CHAPTER 9

UNBALANCED THREE-PHASE THREE-LEVEL RECTIFIER

9.1 Introduction

In recent years, the three-phase ac-dc converters are widely used in industrial applications. The static power converters are nonlinear in nature, and consequently they generate the harmonics into the supply. As a result the power factors of the converters are usually poor and vary with the load. Most electrical systems are designed on the basis of balanced three-phase supply at the fundamental frequency. However, under real operating conditions such as when the input supply is unbalanced or the supply line impedance is unbalanced, the performance of the converter is not necessarily the same as when the converter's performance is balanced [76-80]. In particular, under unbalanced conditions abnormal harmonics are introduced into the system and appear at both the input and output terminals and causes distortions in the waveforms. Therefore converters connected to the unbalanced system have to use large input and output filter to filter out the harmonics. Unbalance in the system may be caused because of short circuit between any two-phases or if any phase of the system opens or due to the unequal impedances in the transformer legs connected to supply the rectifier caused because of different temperature conditions in each leg. Under balanced conditions, using the traditional control techniques in which the control variables are dc quantities, which are obtained by transforming the quantities to the synchronous reference frame, can control the rectifier. Hence the transformation from the abc to synchronous reference frame is necessary. Under unbalance conditions, even in the synchronous reference frame, the control

variables will be time varying signals and hence the suggested control scheme based on synchronous reference frame will be complex and becomes difficult to implement. Hence a control scheme, which will not require these transformations, will be a good choice for controlling. A new control scheme based on the utilization of the natural variables of the system is proposed in this chapter. An attractive advantage of this controller lies in the capacities of working in both balanced and unbalanced conditions, in which the unity power factor can be achieved in balanced condition and a constant input power can be achieved in unbalanced situation.

Objectives of control scheme:

- To regulate the dc bus voltage.
- Bi-directional power flow.
- To draw balanced sinusoidal currents under balanced conditions with unity power factor.
- To transfer constant power even under unbalanced conditions like unbalanced source voltages or unbalanced source impedances.

9.2 Circuit Configuration

The proposed circuit configuration is based on the general three-phase three-leg neutral point clamped converter with unbalanced source and unbalanced input impedances as shown in Figure 9.1. The converter consists of twelve switching devices and six clamping diodes. The input side boost inductors L_a, L_b, and L_c are used to filter out the input harmonic content and provide sinusoidal and have R_a, R_b, and R_c as the

series equivalent resistors. Under unbalanced impedance condition, the impedances are unequal in all the phases.

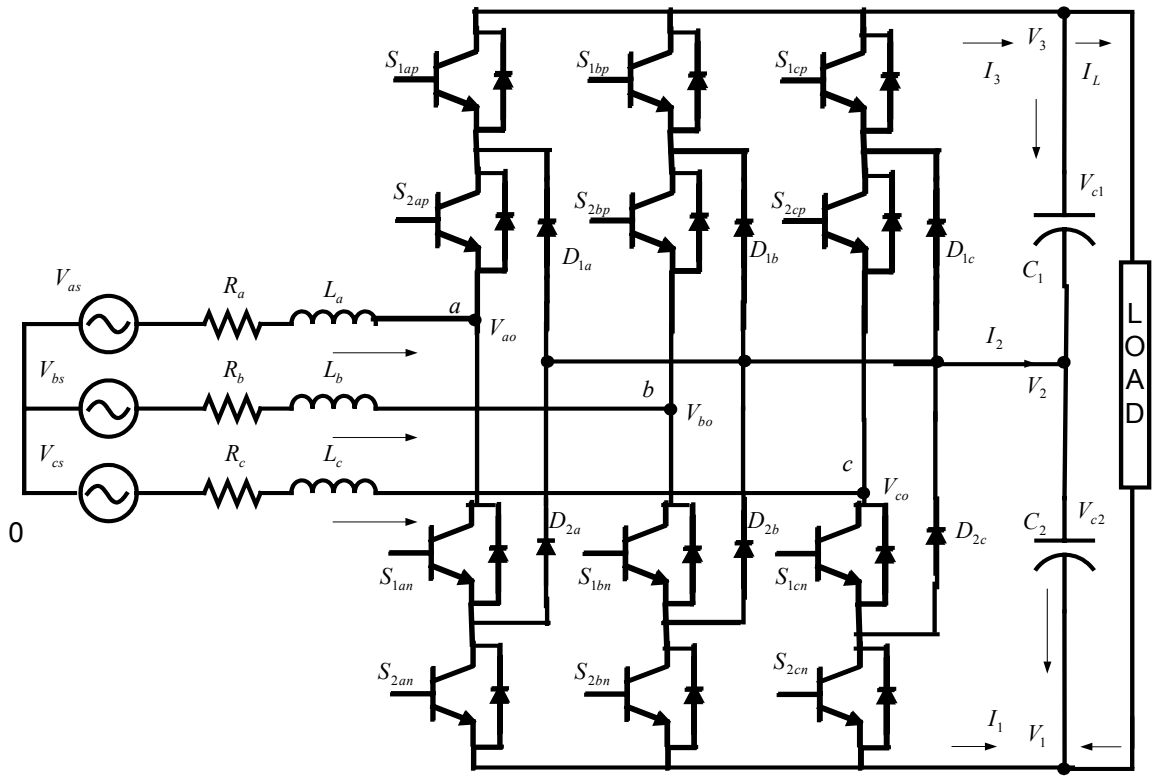

Figure 9.1 Schematic of a three-phase three-level rectifier under unbalanced operation.

9.3 Mathematical Model of the Circuit

Applying the KVL for the input side, write the supply voltage as the sum of the voltage drop across the input side impedance

$$v_a = i_a R_a + L_a p i_a + v_{ao} \tag{9.1}$$

$$v_b = i_b R_b + L_b p i_b + v_{bo} \tag{9.2}$$

$$v_c = i_c R_c + L_c p i_c + v_{co}. \tag{9.3}$$

The voltage V_{ao} is given by

$$v_{ao} = H_{a3} V_{30} + H_{a2} V_{20} + H_{a1} V_{10} \tag{9.4}$$

$$v_{bo} = H_{b3} V_{30} + H_{b2} V_{20} + H_{b1} V_{10} \tag{9.5}$$

$$v_{co} = H_{c3} V_{30} + H_{c2} V_{20} + H_{c1} V_{10} \bullet \tag{9.6}$$

From Chapter 4, similar to the three-level inverter the switching constraint to avoid the shorting of the output capacitor; i.e., at any instant of time only one combination of devices should be on. This leads to the condition as shown below.

$$H_{a3} + H_{a2} + H_{a1} = 1 \tag{9.9}$$

$$H_{b3} + H_{b2} + H_{b1} = 1 \tag{9.8}$$

$$H_{c3} + H_{c2} + H_{c1} = 1 \tag{9.9}$$

Consider phase A.

$$H_{a3} + H_{a2} + H_{a1} = 1$$

$$\Rightarrow H_{a2} = 1 - H_{a3} - H_{a1}$$

By substituting the above in output voltage in Eq. (9.4)

$$v_{ao} = H_{a3}V_{30} + (1 - H_{a3} - H_{a1})V_{20} + H_{a1}V_{10}$$

$$= H_{a3}(V_{30} - V_{20}) + H_{a1}(V_{10} - V_{20}) + V_{20}$$

$$= H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20}$$

where V_{20} is the voltage between the neutral of the supply to the common point of the two capacitors.

Similarly for the other two phases

$$v_{ao} = H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20} \tag{9.10}$$

$$v_{bo} = H_{b3}V_{c1} - H_{b1}V_{c2} + V_{20} \tag{9.11}$$

$$v_{co} = H_{c3}V_{c1} - H_{c1}V_{c2} + V_{20}. \tag{9.12}$$

By substituting the expression from Eqs. (9.10-9.12) in Eqs. (9.1-9.3)

$$v_a = i_a R_a + L_a p i_a + H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20} \tag{9.13}$$

$$v_b = i_b R_b + L_b p i_b + H_{b3}V_{c1} - H_{b1}V_{c2} + V_{20} \tag{9.14}$$

$$v_c = i_c R_c + L_c p i_c + H_{c3}V_{c1} - H_{c1}V_{c2} + V_{20}. \tag{9.15}$$

As explained in Chapter 4, the switching function of the devices is

$$H_{a3} = \left(\frac{2v_{a0}}{V_d} + 1\right)\frac{1}{3} \quad , \; H_{a2} = \frac{1}{3}, \; H_{a1} = \left(-\frac{2v_{a0}}{V_d} + 1\right)\frac{1}{3}. \tag{9.16}$$

The switching pulses can be represented as sum of dc component and fundamental term (cosine or sine varying term) as

$$H_{a3} = (M_{a3} + 1)\frac{1}{3} \tag{9.17}$$

where M_{a3} is called the modulation signal which can be sine or cosine signal.

By equating the switching function H_{a3} and Eq. (9.17)

$$\left(\frac{2v_{a0}}{V_d}+1\right)\frac{1}{3}=\left(M_a+1\right)\frac{1}{3}.$$

Hence the modulation signal for the top devices is

$$M_{a3}=\frac{2v_{a0}}{V_d}. \tag{9.18}$$

Similarly for the other devices, the modulation signal is obtained as

$$M_{a2}=0 \text{ and } M_{a1}=-\frac{2v_{a0}}{V_d}. \tag{9.19}$$

From Eq. (8.29) and (8.30)

$$M_{a3}=-M_{a1}=H_a. \tag{9.20}$$

where H_a is the modulation signal.

Substituting the condition in Eq. (9.20) into Eqs. (9.13 – 9.15)

$$v_a=i_aR_s+L_spi_a+H_aV_{dc}+V_{20} \tag{9.21}$$

$$v_b=i_bR_s+L_spi_b+H_bV_{dc}+V_{20} \tag{9.22}$$

$$v_c=i_cR_s+L_spi_c+H_cV_{dc}+V_{20}. \tag{9.23}$$

The node currents are given by the

$$I_3=H_{a3}i_a+H_{b3}i_b+H_{c3}i_c \tag{9.24}$$

$$I_2=H_{a2}i_a+H_{b2}i_b+H_{c2}i_c \tag{9.25}$$

$$I_1=H_{a1}i_a+H_{b1}i_b+H_{c1}i_c. \tag{9.26}$$

Writing the KCL equation at node 3, i.e., the current flowing through the capacitor C_1 is equal to the difference of the node current I_3 and the load current I_{dc} and the current flowing through the capacitor C_2 is given by the KCL equation at node 1.

$$CpV_{c1} = -I_{dc} + H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{9.27}$$

$$CpV_{c2} = -\left[I_{dc} + H_{a1} i_a + H_{b1} i_b + H_{c1} i_c\right] \tag{9.28}$$

The sum of the two-capacitor voltages after substituting the switching condition is

$$CpV_d = -2I_{dc} + 2\left(H_a i_a + H_b i_b + H_c i_c\right). \tag{9.29}$$

9.4 Control Scheme

The main objective of any control scheme is to regulate the reference quantity under all circumstances whether the system is balanced or unbalanced. In the present control scheme the main objective is to regulate the dc-link voltage and to achieve constant power transfer under all possible conditions and to achieve unity power factor for a balanced case.

Similar to the other control schemes, the natural reference frame controllers are used for controlling the currents and a PI controller is used for dc-link voltage. In the present control scheme three controllers are used to control the line currents.

9.4.1 Control Methodology

Let

$$i_a R_a + L_a p i_a = \sigma_a \tag{9.30}$$

$$i_b R_b + L_b p i_b = \sigma_b \tag{9.31}$$

$$i_c R_c + L_c p i_c = \sigma_c . \tag{9.32}$$

By substituting the above assumption into Eqs. (9.21) – (9.23) and simplifying the expressions for the modulation signals are obtained as

$$H_a = \frac{v_{as} - \sigma_a - V_{2o}}{V_{c1} + V_{c2}} \tag{9.33}$$

$$H_b = \frac{v_{bs} - \sigma_b - V_{2o}}{V_{c1} + V_{c2}} \tag{9.34}$$

$$H_c = \frac{v_{cs} - \sigma_c - V_{2o}}{V_{c1} + V_{c2}}. \tag{9.35}$$

In the present control scheme an assumption is being made that the unbalance in the source voltages is known and is equal to the zero sequence voltage, i.e., the average of the three voltages. Generally the unbalance voltage is equal to the zero sequence voltage. The unbalanced voltages can be made balanced by subtracting the zero sequence voltage from the actual voltages. Hence

$$V_{20} = \frac{1}{3}\left(v_{as} + v_{bs} + v_{cs}\right). \tag{9.36}$$

Let $v_{as}' = v_{as} - V_{20}$, $v_{bs}' = v_{bs} - V_{20}$ and $v_{cs}' = v_{cs} - V_{20}$.

It is clear that the new set of voltages form a balanced set of voltages; i.e.,

$$v_{as}' + v_{bs}' + v_{cs}' = 0.$$

Hence the expressions for the modulation signals become

$$H_a = \frac{v_{as}' - \sigma_a}{V_{c1} + V_{c2}} \tag{9.37}$$

$$H_b = \frac{v_{bs}' - \sigma_b}{V_{c1} + V_{c2}} \tag{9.38}$$

$$H_c = \frac{v_{cs}' - \sigma_c}{V_{c1} + V_{c2}}. \tag{9.39}$$

By substituting the expressions of the modulation signals in Eq. (9.29)

$$CpV_d = -2I_{dc} + 2\left(\left(\frac{v_{as}{}' - \sigma_a}{V_{c1}+V_{c2}}\right)I_a + \left(\frac{v_{bs}{}' - \sigma_b}{V_{c1}+V_{c2}}\right)I_b + \left(\frac{v_{cs}{}' - \sigma_c}{V_{c1}+V_{c2}}\right)I_c\right)$$

$$V_d CpV_d = -2I_{dc}V_d + 2\left(v_{as}{}'i_a + v_{bs}{}'i_b + v_{cs}{}'i_c - \sigma_a i_a - \sigma_b i_b - \sigma_c i_c\right)$$

$$\frac{1}{2}CpV_d{}^2 + 2I_{dc}V_d = 2\left(v_{as}{}'i_a + v_{bs}{}'i_b + v_{cs}{}'i_c - \sigma_a i_a - \sigma_b i_b - \sigma_c i_c\right).$$

Assuming $\frac{1}{2}CpV_d{}^2 = \sigma_v$ as the output of the voltage controller.

$$\sigma_v + 2I_{dc}V_d = 2\left(v_{as}{}'i_a + v_{bs}{}'i_b + v_{cs}{}'i_c - \sigma_a i_a - \sigma_b i_b - \sigma_c i_c\right) \tag{9.40}$$

The sum of the phase currents is equal to zero, hence

$$i_a + i_b + i_c = 0$$

$$\Rightarrow i_c = -i_a - i_b \ .$$

By substituting the above condition in Eq. (9.40) and simplifying

$$\sigma_v + 2I_{dc}V_d = 2[v_{a'c'}i_a + v_{b'c'}i_b - i_a(\sigma_c - \sigma_a) - i_b(\sigma_c - \sigma_b)]. \tag{9.41}$$

The power transfer in a three-phase circuit as

$$P = v_{as}i_a + v_{bs}i_b + v_{cs}i_c$$

$$\Rightarrow$$
$$P = v_{ac}i_a + v_{bc}i_b \ .$$

The main objective of the control scheme is to transfer constant power and hence the differentiation of power with respect to time is zero; i.e.,

$$\frac{\partial P}{\partial t} = 0 \ .$$

Hence

$$0 = I_a pV_{ac} + V_{ac} pI_a + I_b pV_{bc} + V_{bc} pI_b \tag{9.42}$$

where $p = \dfrac{\partial}{\partial t}$.

From Eqs. (9.30) and (9.32)

$$pi_a = \frac{\sigma_a - i_a R_a}{L_a}.$$

$$pi_b = \frac{\sigma_b - i_b R_b}{L_b}.$$

By substituting pi_a, pi_b in Eq. (9.42) and simplifying,

$$i_a\left[L_a L_{\ b} pv_{ac} - L_b R_a v_{ac}\right] + i_b\left[L_a L_{\ b} pv_{bc} - L_a R_b v_{ac}\right] = -\left[L_b v_{ac}\sigma_a + L_a v_{bc}\sigma_b\right]. \tag{9.43}$$

Expressing Eqs. (9.41)-(9.43) in a matrix form

$$\begin{bmatrix} L_a L_{\ b} pv_{ac} - L_b R_a v_{ac} & L_a L_{\ b} pv_{bc} - L_a R_b v_{bc} \\ v_{ac} + \sigma_c - \sigma_a & v_{bc} + \sigma_c - \sigma_b \end{bmatrix} \begin{bmatrix} I_a \\ I_b \end{bmatrix} = \begin{bmatrix} -\left[L_b v_{ac}\sigma_a + L_a v_{bc}\sigma_b\right] \\ \sigma_v + 2I_{dc}\left(V_{c1} + V_{c2}\right) \end{bmatrix}.$$

By solving the above matrix for I_a, I_b

$$i_a = \frac{\left(v_{bc} + \sigma_c - \sigma_b\right)\left(-\left[L_b v_{ac}\sigma_a + L_a v_{bc}\sigma_b\right]\right) - \left(\sigma_v + 2I_{dc}\left(V_{c1} + V_{c2}\right)\right)\left(L_a L_{\ b} pv_{bc} - L_a R_b v_{bc}\right)}{\Delta} \tag{9.44}$$

$$i_b = \frac{\left(L_a L_{\ b} pv_{ac} - L_b R_a v_{ac}\right)\left(\sigma_v + 2I_{dc}\left(V_{c1} + V_{c2}\right)\right) - \left(v_{ac} + \sigma_c - \sigma_a\right)\left(-\left[L_b V_{ac}\sigma_a + L_a v_{bc}\sigma_b\right]\right)}{\Delta} \tag{9.45}$$

where

$$\Delta = \left(L_a L_{\ b} p v_{ac} - L_b R_a v_{ac}\right)\left(v_{bc} + \sigma_c - \sigma_b\right) - \left(L_a L_{\ b} p v_{bc} - L_a R_b v_{bc}\right)\left(v_{ac} + \sigma_c - \sigma_a\right).$$

Hence using the above expressions the reference phase currents can be generated. Phase c current can be obtained using the balance condition for the current.

The schematic of the control scheme adopted for proposed unbalanced rectifier is shown in Figure 9.2. The control structure has two loops, the outer control loop formed by the voltage controller and the inner control loop formed by the current controllers. The bandwidth of the outer controller is selected in such a way that the system takes a shorter time to reach steady state when compared to the inner-loop. The voltage error signal obtained by comparing the reference dc-link voltage with the actual dc-link voltage is passed through a PI controller. The condition for constant power transfer can be obtained using Eq. (9.43). Using constant power equation and the dc-link capacitor equation, the reference currents can be calculated using Eqs. (9.44) and (9.45). The reference currents so generated are compared with the actual phase currents and the error signals are passed though the natural reference frame controllers K_a, K_b, and K_c. The structure of these controllers is explained in the next section. The output of these controllers is assumed as σ_a, σ_b, and σ_c. Using expressions (9.37) - (9.39) the modulation signals can be obtained. These signal when modulated using the carrier based technique generates the switching pulses for the power devices.

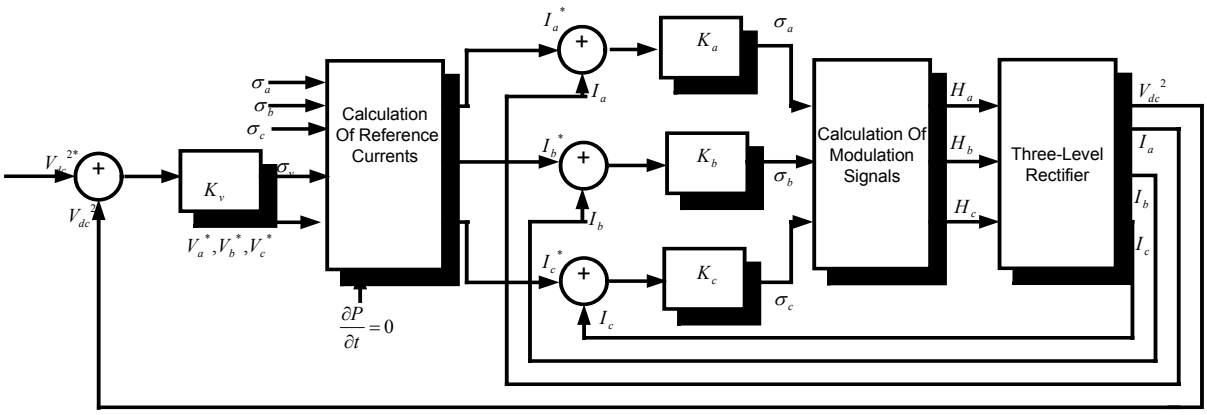

Figure 9.2: Schematic of the control scheme for unbalanced three-phase three-level rectifier.

9.4.2 Controller Structures and Transfer Functions

The current controller whose structure has been discussed in Chapter 9 is shown in Figure (9.3). These kinds of controllers are called as the natural reference frame controllers in which the actual signals are controlled without any transformations. All three controllers have the same structures. Using these kinds of control structures the implementation becomes a lot simpler when compared to controlling the dq quantities.

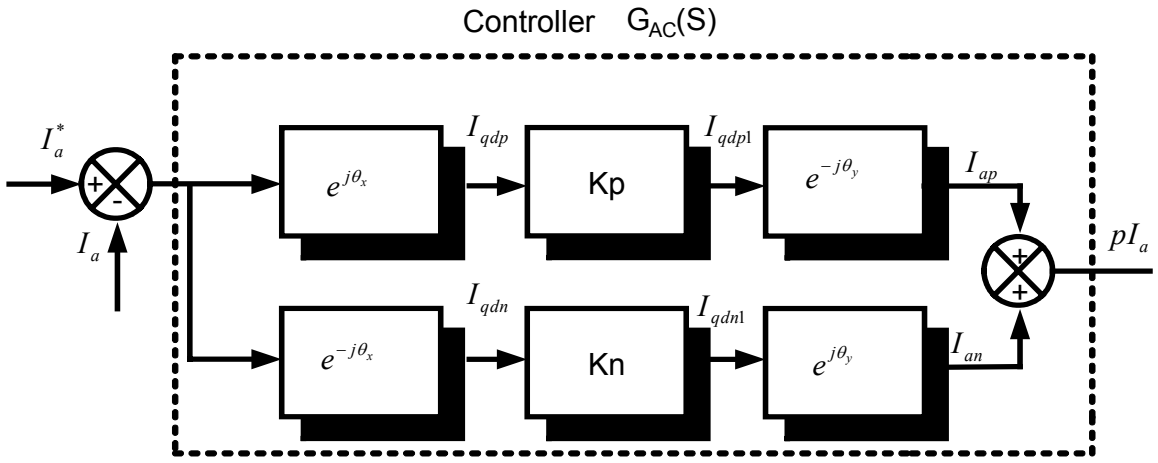

Figure 9.3 Structure of the natural reference frame controller

The procedure for determining the transfer functions of the currents has already been discussed in the previous chapters. Using the same methodology the transfer functions are derived as follows:

$$\frac{i_a}{i_a^*} = \frac{p^2 2K_p Cos\phi_1 + 2pK_i Cos\phi_1 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1}{L_a p^3 + p^2\left[R_a + 2K_p Cos\phi_1\right] + p\left[3\omega_s{}^2 L_a + 2K_i Cos\phi_1\right] + \left[R_a \omega_s{}^2 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1\right]}$$

$$\frac{i_b}{i_b^*} = \frac{p^2 2K_p Cos\phi_1 + 2pK_i Cos\phi_1 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1}{L_b p^3 + p^2\left[R_b + 2K_p Cos\phi_1\right] + p\left[3\omega_s{}^2 L_b + 2K_i Cos\phi_1\right] + \left[R_b \omega_s{}^2 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1\right]}$$

$$\frac{i_c}{i_c^*} = \frac{p^2 2K_p Cos\phi_1 + 2pK_i Cos\phi_1 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1}{L_c p^3 + p^2\left[R_c + 2K_p Cos\phi_1\right] + p\left[3\omega_s{}^2 L_c + 2K_i Cos\phi_1\right] + \left[R_c \omega_s{}^2 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1\right]}.$$

Comparing the denominator of the transfer function with the Butterworth polynomial is one of the useful techniques in choosing the controller parameters. From the transfer functions, it is clear that the system is of a third order system and so its denominator is compared with third order polynomial.

$$p^3 + 2p^2\omega_o + 2p\omega_o{}^2 + \omega_o{}^3 = 0 .$$

Following equations are obtained

$$\frac{R_a + 2K_p Cos\phi_1}{L_a} = 2\omega_o$$

$$\frac{\omega_s{}^2 L_a + 2K_i Cos\phi_1}{L_a} = 2\omega_o{}^2$$

$$\frac{R_a \omega_s{}^2 + 2K_p Cos\phi_1 \omega^2 - 2K_i \omega Sin\phi_1}{L_a} = \omega_o{}^3 .$$

In the similar way, the controller parameters for other controllers can be determined.

9.4.3 Voltage Control

A simple PI controller is being used to control the voltage, as the quantity to be controlled is a dc quantity. The transfer function of the controller is as follows:

$$\frac{V_{dc}{}^2}{V_{dc}{}^{*2}} = \frac{sK_p + K_i}{Cs^2 + 2sK_p + 2K_i} . \tag{9.35}$$

The second order Butterworth polynomial is given by

$$s^2 + \sqrt{2}s\omega_0 + \omega_0{}^2 = 0 . \tag{9.36}$$

By comparing the coefficients of same exponentials

$$K_p = \frac{C\omega_0}{\sqrt{2}} \text{ and } K_i = \frac{C\omega_0{}^2}{2} . \tag{9.37}$$

9.4.4 Circuit Parameters

Unbalanced operation:

Input line resistance $R_a = 0.2\Omega; R_b = 0.4\Omega; R_c = 0.1\Omega$

Input line inductance $L_a = 10mH; L_b = 20mH; L_c = 5mH$

Input Supply Voltage $v_a = 80\cos(\omega t)$

$$v_b = 40\cos(\omega t - 120^0)$$

$$v_c = 50\cos(\omega t + 120^0)$$

Output dc-capacitance $C_1 = C_2 = 2200\mu F$

Load resistance $R_L = 75\Omega$

Balanced operation:

Input line resistance $R_s = 0.2\Omega$

Input line inductance $L_s = 10mH$

Input Supply Voltage $v_a = 80\cos(\omega t)$

$$v_b = 80\cos(\omega t - 120^0)$$

$$v_c = 80\cos(\omega t + 120^0)$$

Output dc-capacitance $C_1 = C_2 = 2200\mu F$

Load resistance $R_L = 75\Omega$

9.5 Simulation Results

The objective of the control scheme is to regulate the dc link voltage, to transfer constant power even under unbalanced conditions, and also to achieve unity power factor under balanced condition. The simulation is done for both balanced and unbalanced conditions. The circuit parameters used for simulating the rectifier are mentioned in section 9.4.4. The reference dc voltage is defined as 200 V; i.e., each capacitor voltage has to settle at 100 V. Figures 9.4 – 9.8 demonstrate the simulation results for unbalanced condition. Initially the converter is simulated such that it operates in the rectifier mode; i.e., the power is being transferred from the source to the load. Figures 9.4 – 9.5 illustrates the results for a rectifier mode of operation. Figure 9.4 (I) (a) shows the modulation signals and it is clear from the figure that the signals are unbalanced. These signals when modulated using the carrier based PWM explained in Chapter 3 generates the switching pulses for the devices. Figures 9.4 (I) (a) (b) illustrate that the two-capacitor voltages settle to the reference voltages with a ripple of 0.5 V each. Figure 9.4 (II) (a) shows the line-line voltage and (II) (b) shows the phase "a" voltage and phase "a" current and it is clear that unity power factor is not achieved, as there is a small phase difference between the phase voltage and phase current. Figure 9.5 (I) show the three phase currents and as expected the peaks of the phase currents will be equal. Figure 9.5 (II) (a) (b) (c) shows the tracking of the currents and also the effectiveness of the controller. After time t = 0.95 sec the load is being changed such that the converter is operated in the regenerative mode; i.e., the power is transferred from the load to the source. Even under this condition the capacitor voltage is well regulated. Figure 9.6 (a) and (b) displays the

power transferred from the supply to the load, (a) which is calculated using the reference currents and (b) which is calculated using the actual currents. As seen from the figure the power, which is calculated, using the actual currents has a ripple of ± 50 W. Figure 9.9 (a) shows the modulation signals that are required to control the converter in the regenerative mode to regulate the dc link voltage. Figure 9.9 (b) (c) gives the regulated capacitor voltages. Hence the control scheme works effectively both in the rectifier mode and the inverter mode. Hence using this scheme bi-directional power flow can be achieved.

In the second case, the control scheme is simulated for a balanced condition and in the particular case, unity power has to be achieved along with the dc regulation and constant power transfer. Figures 9.9 – 9.10 illustrate the effectiveness of the controller. Figure 9.9 (a), (b), and (c) shows the three-phase modulation signals and as observed the modulation signals are balanced. Figure 9.10 (I) (a) shows the line-line voltage and (II) (b) illustrate the unity power factor operation and (c) and (d) show the capacitor voltages which have settled to the reference voltages. Figure 9.10 (II) (a) shows the total dc-link capacitor voltage and there are some glitches which are caused because of the load changes at t = 0.95 sec and t = 1.5 sec. Figure 9.10 (II) (b) gives the power transferred. At t = 0.95 sec the direction of the power is changed; i.e., the load is changed such that it operates in the regenerative mode and at t = 1.5 sec the direction of power is changed again such that power is transferred from the source to the load.

Unbalance Operation:

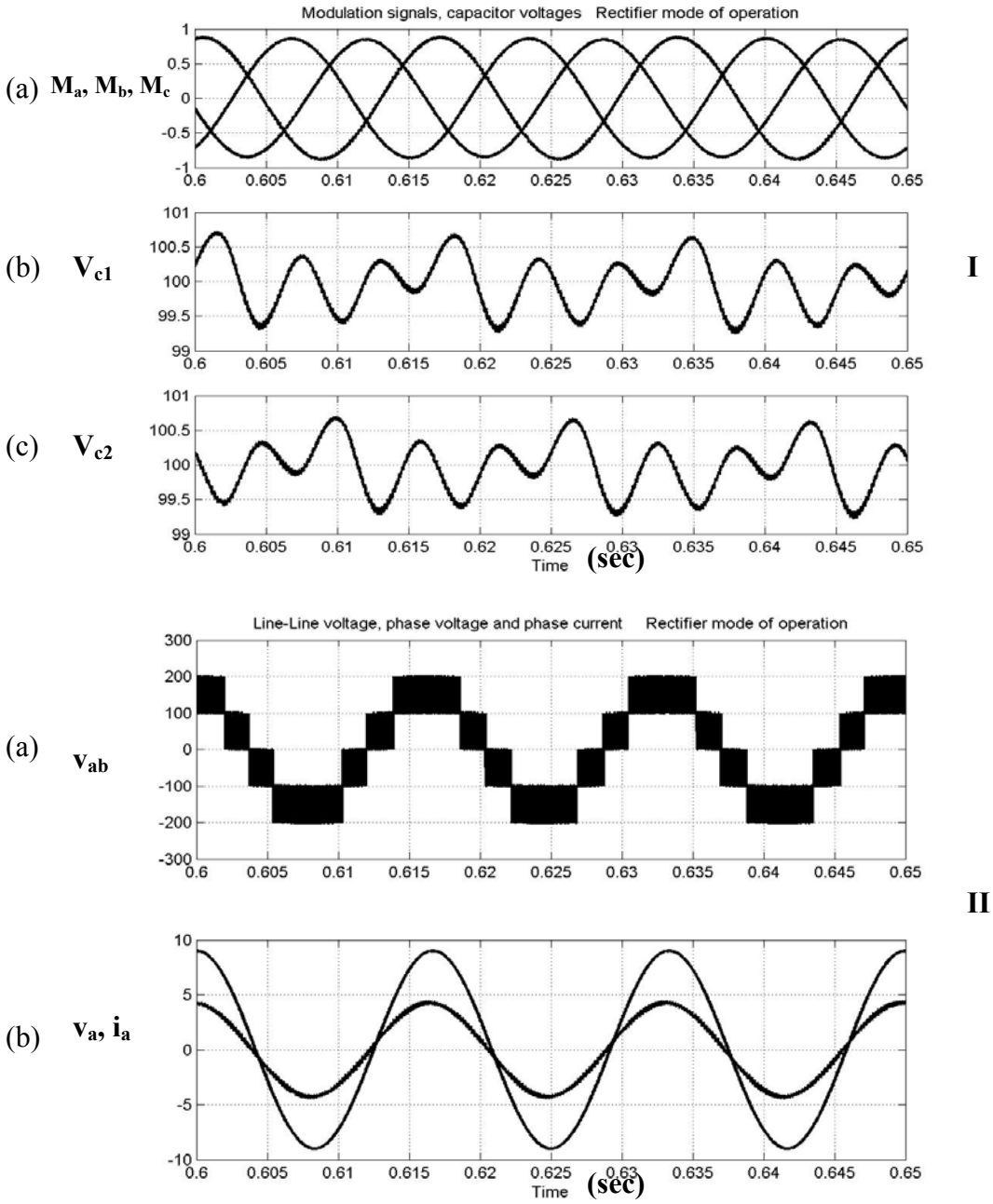

Figure 9.4: Simulation results for control under Unbalance operation, rectifier mode of operation I (a) Three-phase modulation signals (b) (c) Upper and lower capacitor voltages. II (a) Line-line voltage (b) phase "a" voltage (v_a) and phase "a" current (i_a).

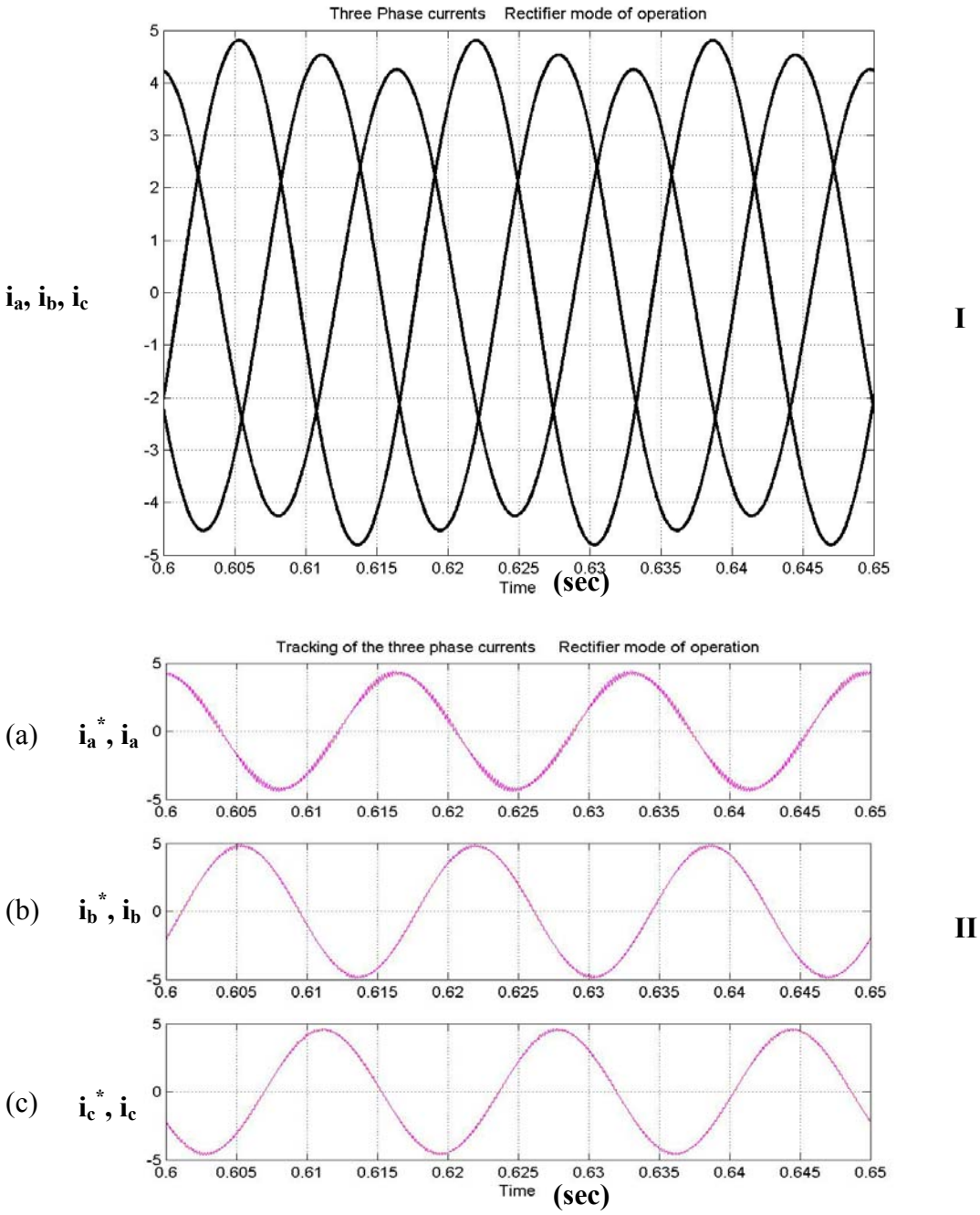

Figure 9.5: Simulation results for control under Unbalance operation, rectifier mode of operation. (I) (a) Three-phase currents (II) (a) (b) (c) Tracking of three phase reference currents.

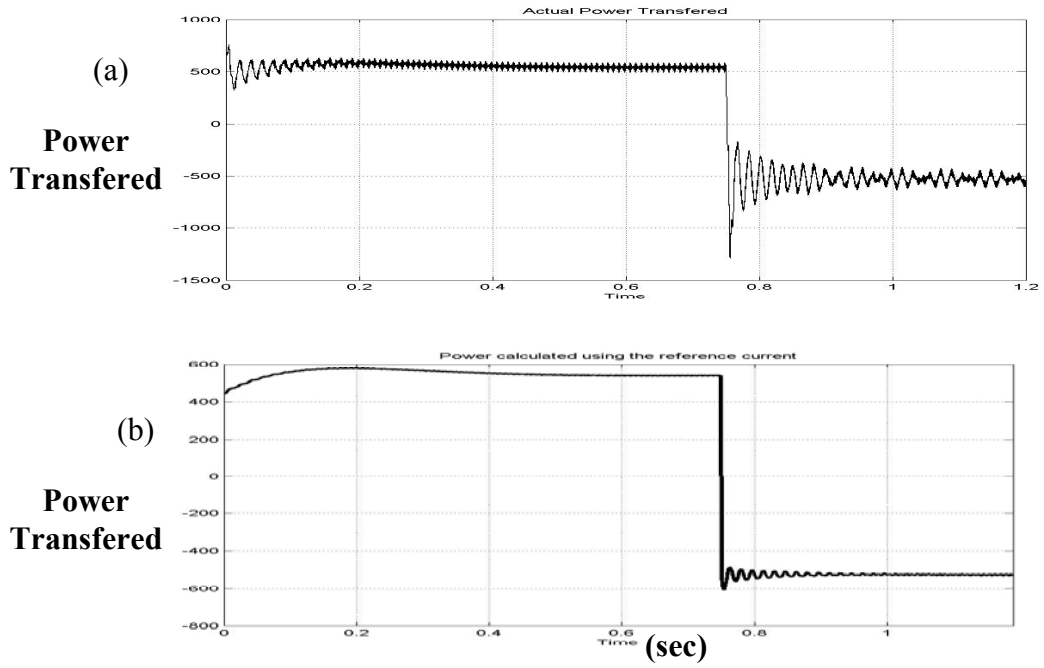

Figure 9.6: Simulation results for control under Unbalance operation (I) Power calculated by using the actual phase currents (II) Power calculated using the reference currents.

Regenerative mode of operation:

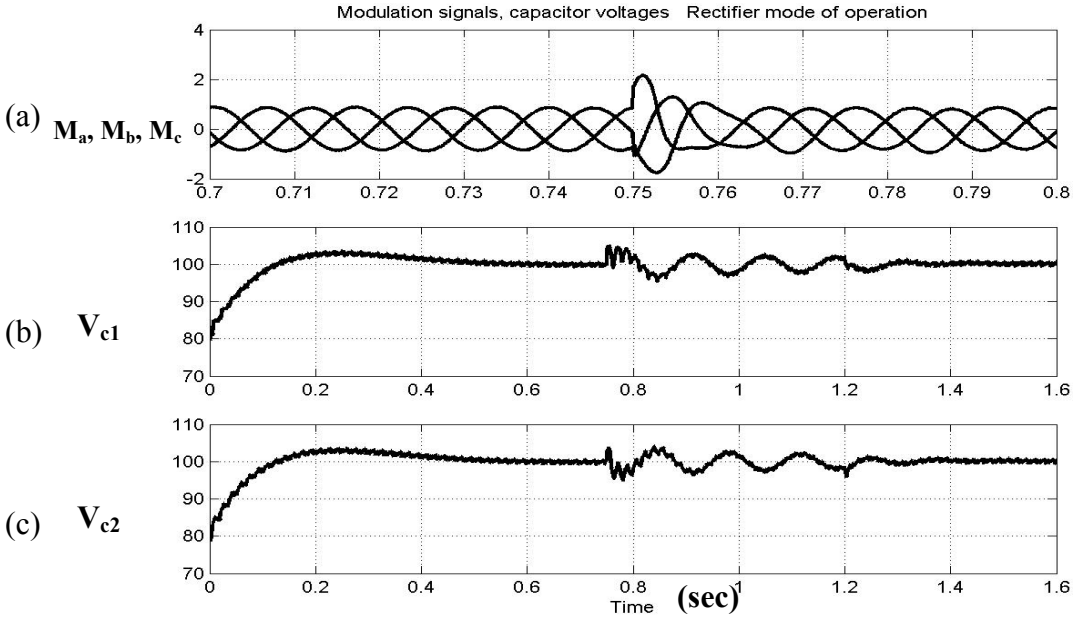

Figure 9.7: Simulation results for control under Unbalance operation, during the load change (a) Three-phase modulation signals, (b) Upper capacitor voltage $V_{c1,}$ (c) lower capacitor voltage V_{c2}.

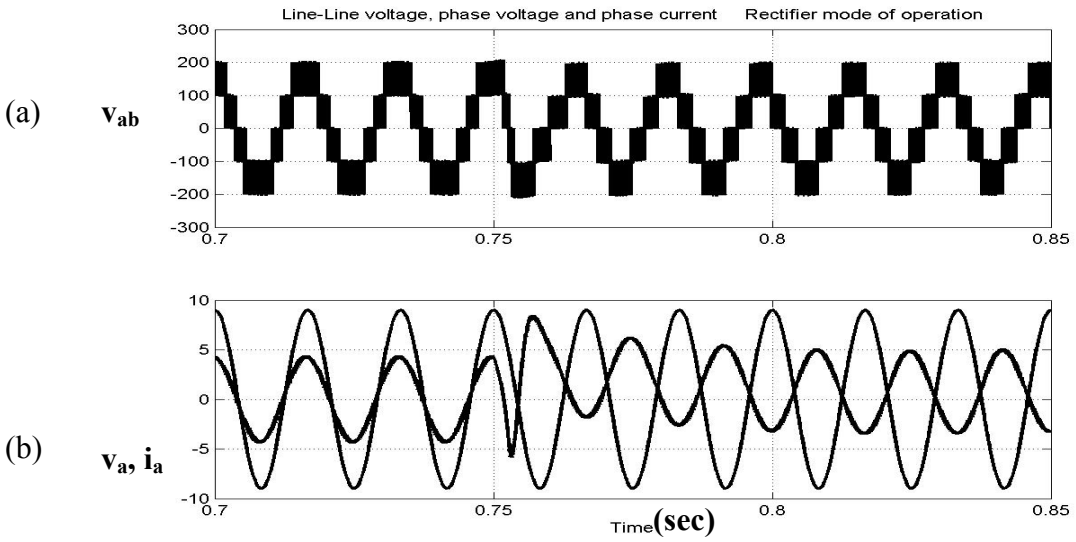

Figure 9.8: Simulation results for control under Unbalance operation, during the load change (a) Line-line voltage (b) phase "a" voltage (v_a) and phase "a" current (i_a).

Balance Operation:

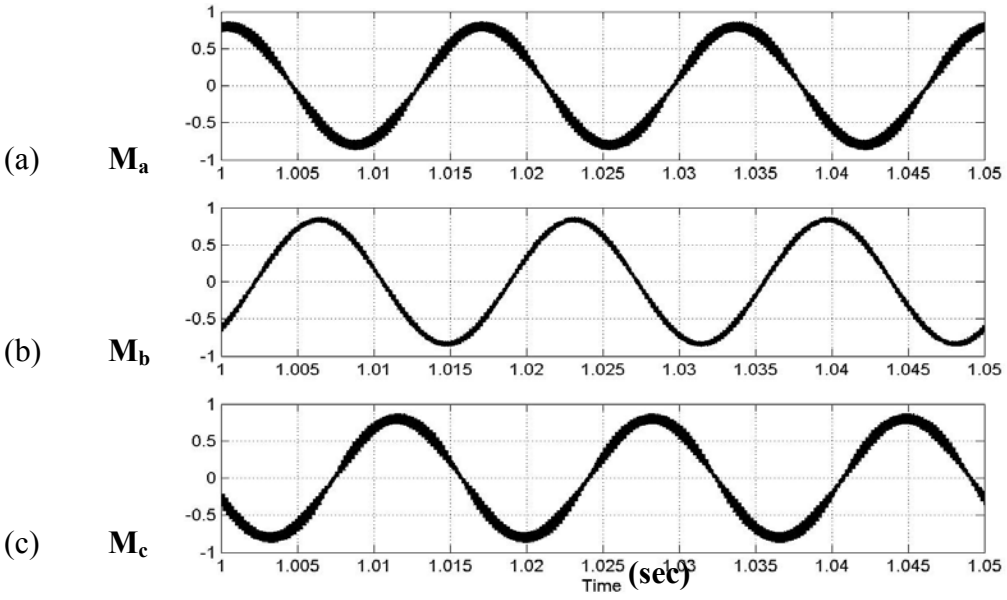

Figure 9.9: Simulation results for control under balance operation, rectifier mode (a), (b), (c) Three-phase modulation signals.

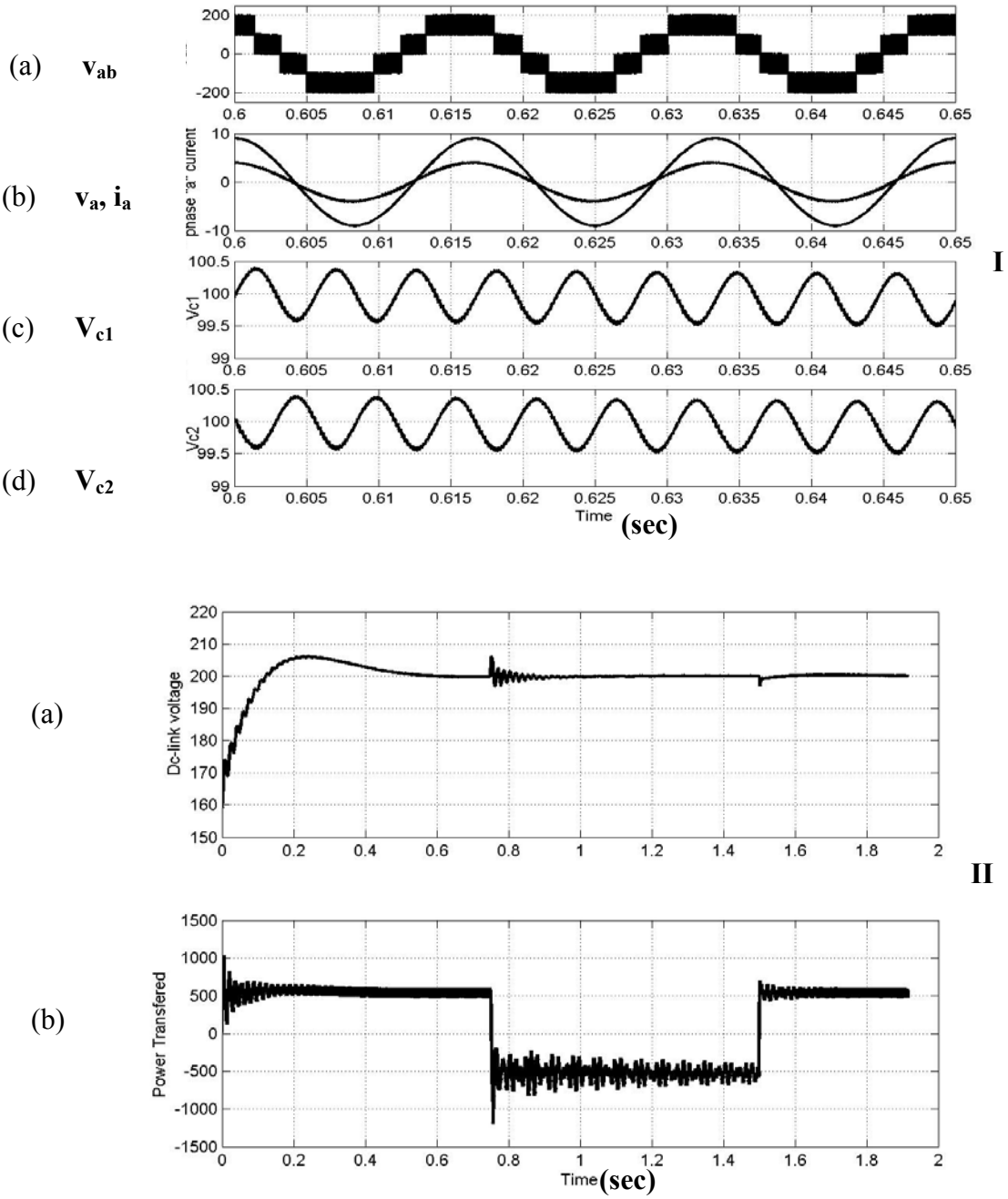

Figure 9.10: Simulation results for control under balance operation, rectifier mode (I) (a) (b) (c) Three-phase modulation signals (II) (a) Line-line voltage (b) Unity power operation, phase "a" voltage (v_a) and phase "a" current (i_a) (c) (d) Upper and lower capacitor voltages (V_{c1}, V_{c2}). (II) (a) Capacitor Voltage ,(b) Power transferred