CHAPTER 7

THREE-PHASE THREE-LEG THREE-LEVEL NEUTRAL POINT CLAMPED RECTIFIER

7.1 Introduction

Many inherent benefits of multilevel converters have led to their increased interest amongst industry utilities. At present, the two most commonly used multilevel topologies are the three-level neutral-point-clamped (NPC) [4-6] and cascaded topologies. Multilevel converters have been attracting attention for medium-voltage and high-power applications. The advantages of the NPC converters are improving the waveform quality and reducing voltage stress on the power devices. The capacitor-clamped converter is an alternate structure to obtain the multilevel waveforms on the ac terminals. The voltage stress on the open power devices is constrained by clamping capacitors. Series connection of full bridge converters was an alternate method to achieve multilevel waveforms because of their modularity and simplicity of control. However, if the voltage levels are more than three levels, the control strategy is complicated to implement. Most three-phase rectifiers use a diode bridge circuit and a bulk storage capacitor but it has poor power factor and high pulsation line current. Passive capacitors and inductors have been used to form passive LC filters for eliminating current harmonics and improving the system power factor. The drawbacks of the two-level converters are the high voltage stress across the devices, large passive components and

hence due to the inherent advantages of the three-level NPC converters were proposed to draw the sinusoidal line currents in phase with mains voltage [57-65].

Objective of the Control Scheme:

- To obtain a constant DC bus voltage.
- To balance the capacitor voltages.
- Bidirectional power flow.
- Low harmonic distortion of line current.
- To draw sinusoidal currents with unity power factor.
- To generate three voltage levels on the AC terminal voltages v_{ac}, v_{bc}, v_{ca}.

7.2 Circuit Configuration

The proposed circuit configuration is based on the three-phase, three-leg neutral point clamped converter shown in Figure 7.1. The converter consists of a boost inductor L_s on the ac side, to filter the input harmonic current and achieve sinusoidal current waveforms. R_s is the series equivalent resistor. Twelve switching devices with rating V_{dc} / 2 and six clamping diodes with the rating of V_{dc} / 2 are used. The diodes are used to clamp the dc-voltage. The converter also consists of two capacitors on the dc terminal. v_a, v_b, v_c represents the phase voltages of the three-phase AC system.

In Figure 7.1 $S_{1ap}, S_{2ap}, S_{1an}, S_{2an}$ are the four switching devices for phase A and similarly phase B and C have four switching devices. $D_{1a}, D_{2a}, D_{1b}, D_{2b}, D_{1c}, D_{2c}$ are the six clamping diodes. $R_{s,} L_s$ are the input side resistance

and the boost inductors, R_L is the load resistance connected across the two capacitors. C_1, C_2 are the output side DC capacitors to hold the dc output voltage. v_a, v_b, v_c are the three input supply voltages, i_a, i_b, i_c are the input phase currents, and I_3, I_2, I_1 are the three output node currents which charge the capacitor.

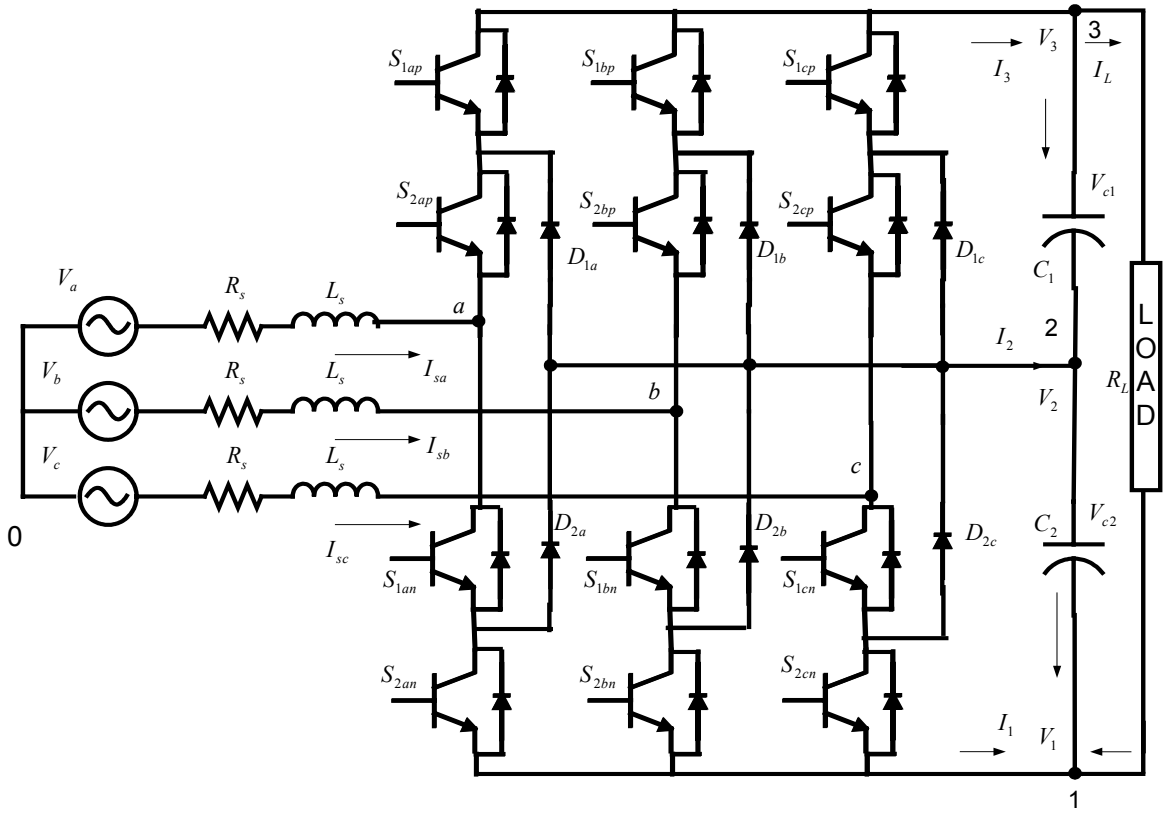


Figure 7.1: Circuit configuration of Three-Phase Three-level Three-Leg Rectifier.

7.3 Modes of Operation

From Chapter 3, in the operation of the multilevel converter combination of switches are used to obtain a stepped waveform, which is close to sinusoidal waveform. The following notations are used for certain combination of devices

$$\begin{aligned} H_{i3} &= S_{1ip} S_{2ip} \\ H_{i2} &= S_{1ip} \overline{S_{2ip}} \\ H_{i1} &= \overline{S_{1ip}}\,\overline{S_{2ip}} \end{aligned} \tag{7.1}$$

$$\overline{S_{1ip}} = 1 - S_{1ip}, \quad \overline{S_{2ip}} = 1 - S_{2ip}$$

where $i = a, b, c$.

Hence in case of a three-level converter there will be three valid operating modes for each phase of the converter as shown in Figures 7.2 –7.4. Consider Phase A as example.

Operation mode 1 $\left(H_{a3} = S_{1ap} S_{2ap}\right)$**:** Figure 7.2 shows the operation mode 1. In this mode of operation, the ac terminal voltage v_{ao} is equal to $V_{dc}/2$ (assuming that $V_{c1} = V_{c2}$). The boost inductor voltage is $V_L = v_a - V_{dc}/2 < 0$ (assuming the voltage drop across the resistor to be negligible). Therefore the line current i_a decreases and the current slope $\frac{di_a}{dt} = \left\{\left(v_a - V_{dc}/2\right)/L\right\}$. The line current i_a will charge or discharge the dc bus capacitor C_1 if the ac system voltage v_a is positive or negative, respectively.

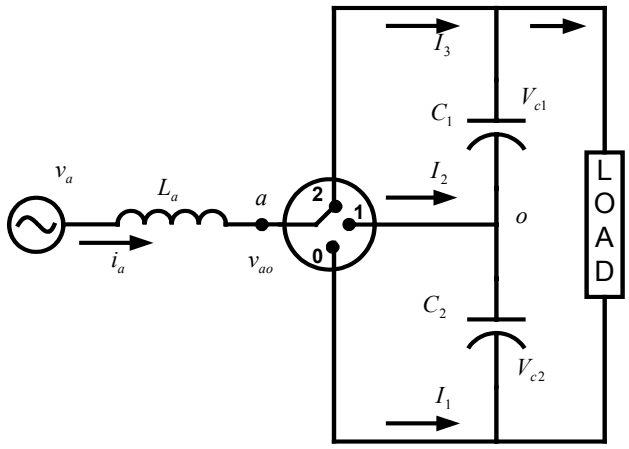


Figure 7.2: Operational modes of the rectifier: Operation Mode 1.

Operation mode 2 $\left(H_{a2} = \overline{S_{1ap}} S_{2ap}\right)$**:** Figure 7.3 shows the operation mode 2. The ac terminal voltage V_{ao} is equal to zero (assuming that $V_{c1} = V_{c2}$). The boost inductor voltage is $V_L = V_a$. Therefore the line current I_a increases or decreases during the positive or negative cycles of the input supply voltage, respectively**.** The line current I_a will not charge or discharge the dc bus capacitors in this mode of operation.

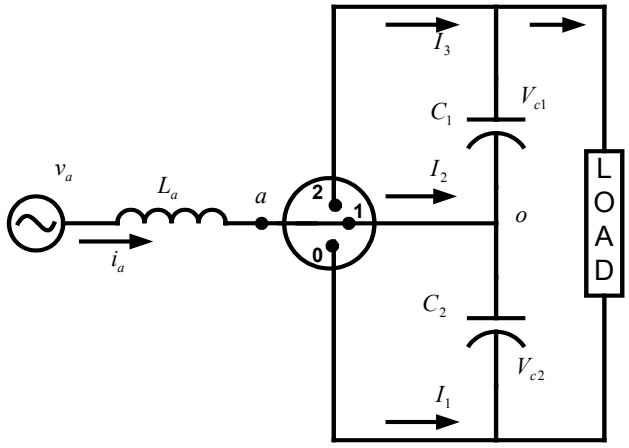


Figure 7.3: Operational modes of the rectifier: Operation Mode 2.

Operation mode 3 $\left(H_{a1} = \overline{S_{1ap}}\,\overline{S_{2ap}}\right)$**:** Figure 7.4 shows the operation mode 3. In this mode of operation, the ac terminal voltage v_{ao} is equal to $-V_{dc}/2$. The boost inductor voltage is $V_L = V_a + V_{dc}/2 > 0$. Therefore the line current i_a increases and the current slope is $\frac{di_a}{dt} = \{(V_a + V_{dc}/2)/L\}$**.** The line current i_a will charge or discharge the dc bus capacitor C_2 if the ac system voltage v_a is positive or negative half cycles of the supply voltage, respectively.

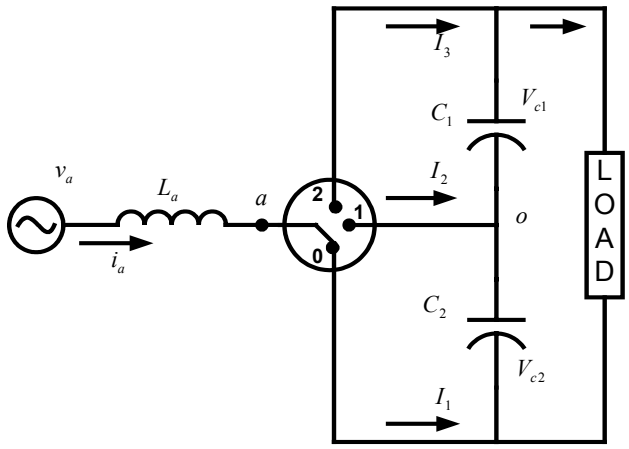


Figure 7.4: Operational modes of the rectifier: Mode 3 operation.

7.4 Mathematical Model of the Circuit

Applying Kirchoff's voltage law (KVL) for the input side, the supply voltage can be written as the sum of the voltage drop across the input side impedance and

$$v_a = i_a R_s + L_s p i_a + v_{ao} \tag{7.2}$$

$$v_b = i_b R_s + L_s p i_b + v_{bo} \tag{7.3}$$

$$v_c = i_c R_s + L_s p i_c + v_{co}. \tag{7.4}$$

The positive node voltage appears at point 'a' when the upper two switching combination occurs i.e., when S_{1ap}, S_{2ap} are on. Hence the effective voltage that appears at point 'a' in a cycle is $H_{a3}V_{30}$. Similarly the other two node voltages appear when the other switching combination occurs i.e., H_{a2} and H_{a1}. Hence the voltage v_{ao} is given by the sum of the three effective voltages

$$v_{ao} = H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10} \tag{7.5}$$

$$v_{bo} = H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10} \tag{7.6}$$

$$v_{co} = H_{c3}V_{30} + H_{c2}V_{20} + H_{c1}V_{10}. \tag{7.7}$$

From Chapter 4, similar to the three-level inverter, the switching constraint to avoid the shorting of the output capacitor; i.e., at any instant of time only one combination of devices should be on. This leads to the condition in Eqs. (7.8-7.10)

$$H_{a3} + H_{a2} + H_{a1} = 1 \tag{7.8}$$

$$H_{b3} + H_{b2} + H_{b1} = 1 \tag{7.9}$$

$$H_{c3} + H_{c2} + H_{c1} = 1. \tag{7.10}$$

Consider phase "a";

$$H_{a3} + H_{a2} + H_{a1} = 1$$

$$\Rightarrow H_{a2} = 1 - H_{a3} - H_{a1}.$$

By substituting the above equation in output voltage Eq. (7.7)

$$v_{ao} = H_{a3}V_{30} + (1 - H_{a3} - H_{a1})V_{20} + H_{a1}V_{10}$$

$$= H_{a3}(V_{30} - V_{20}) + H_{a1}(V_{10} - V_{20}) + V_{20}$$

$$= H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20}$$

where V_{20} is the voltage between the neutral of the supply to the common point of the two capacitors.

Similarly for the other two phases

$$v_{ao} = H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20} \tag{7.11}$$

$$v_{bo} = H_{b3}V_{c1} - H_{b1}V_{c2} + V_{20} \tag{7.12}$$

$$v_{co} = H_{c3}V_{c1} - H_{c1}V_{c2} + V_{20}. \tag{7.13}$$

By substituting the expression in Eqs. (7.11-7.13) into Eqs. (7.2-7.4)

$$v_a = i_a R_s + L_s p i_a + H_{a3}V_{c1} - H_{a1}V_{c2} + V_{20} \tag{7.14}$$

$$v_b = i_b R_s + L_s p i_b + H_{b3}V_{c1} - H_{b1}V_{c2} + V_{20} \tag{7.15}$$

$$v_c = i_c R_s + L_s p i_c + H_{c3}V_{c1} - H_{c1}V_{c2} + V_{20}. \tag{7.16}$$

Hence under balanced condition,

$$V_{20} = -\frac{1}{3}[V_{c1}(H_{a3} + H_{b3} + H_{c3}) + V_{c2}(H_{a1} + H_{b1} + H_{c1})].$$

From Chapter 4, the individual device switching functions are obtained as

$$H_{a3} = \left(\frac{2V_{a0}}{V_d} + 1\right)\frac{1}{3} \quad , \; H_{a2} = \frac{1}{3}, \; H_{a1} = \left(-\frac{2V_{a0}}{V_d} + 1\right)\frac{1}{3}. \tag{7.17}$$

The switching functions of the devices can be approximated using the Fourier series. Since the switching pulses are periodic function of time and they repeat after every cycle of modulation signal and hence the periodic signals can be represented using the Fourier series as a sum of dc component and sine and cosine time varying terms.

$$H_{a3} = \left(M_{a3} + 1\right)\frac{1}{3} \tag{7.18}$$

$$H_{a2} = \left(M_{a2} + 1\right)\frac{1}{3} \tag{7.19}$$

$$H_{a1} = \left(M_{a1} + 1\right)\frac{1}{3} \tag{7.20}$$

where M_{a3}, M_{a2}, M_{a1} are called the modulation signal.

By equating the switching functions and Eq. (7.18)

$$\left(\frac{2v_{a0}}{V_d} + 1\right)\frac{1}{3} = \left(M_a + 1\right)\frac{1}{3}.$$

Hence the modulation signal for the top devices is

$$M_{a3} = \frac{2v_{a0}}{V_d}. \tag{7.21}$$

Similarly for the other devices, the modulation signal is obtained as

$$M_{a2} = 0 \text{ and } M_{a1} = -\frac{2v_{a0}}{V_d}. \tag{7.22}$$

From Eq. (7.21) and (7.22)

$$M_{a3} = -M_{a1} = H_a. \tag{7.23}$$

where H_a is the modulation signal.

Substituting the modulation signals in Eqs. (7.14 – 7.17)

$$v_a = i_a R_s + L_s p i_a + H_a\left(V_{c1} + V_{c2}\right) + V_{20} \tag{7.24}$$

$$v_b = i_b R_s + L_s p i_b + H_b\left(V_{c1} + V_{c2}\right) + V_{20} \tag{7.25}$$

$$v_c = i_c R_s + L_s p i_c + H_c\left(V_{c1} + V_{c2}\right) + V_{20}. \tag{7.26}$$

The node currents are given by

$$I_3 = H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{7.27}$$

$$I_2 = H_{a2} i_a + H_{b2} i_b + H_{c2} i_c \tag{7.28}$$

$$I_1 = H_{a1} i_a + H_{b1} i_b + H_{c1} i_c. \tag{7.29}$$

Writing the Kirchoff's Current Law (KCL) at node 3; i.e., the current flowing through the capacitor C_1 is equal to the difference of the node current I_3 and the load current I_{dc}. The current flowing through the capacitor C_2 is given by the KCL at node 1.

$$CpV_{c1} = -I_{dc} + H_{a3} i_a + H_{b3} i_b + H_{c3} i_c \tag{7.30}$$

$$CpV_{c2} = -\left[I_{dc} + H_{a1} i_a + H_{b1} i_b + H_{c1} i_c\right] \tag{7.31}$$

7.5 Modeling of the Converter

Writing Eqs. (7.14-7.16) in the matrix form

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L_s & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & L_s \end{bmatrix} \begin{bmatrix} pi_a \\ pi_b \\ pi_c \end{bmatrix} + \begin{bmatrix} H_{a3} \\ H_{b3} \\ H_{c3} \end{bmatrix} V_{c1} - \begin{bmatrix} H_{a1} \\ H_{b1} \\ H_{c1} \end{bmatrix} V_{c2} + V_{20}.$$

Transforming the above equation to synchronous reference frame by using transformation matrix $T(\theta)$, where

$$T(\theta)=\begin{bmatrix}\cos(\theta) & \cos(\theta-\beta) & \cos(\theta+\beta)\\ \sin(\theta) & \sin(\theta-\beta) & \sin(\theta+\beta)\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix} \quad \beta=\frac{2\pi}{3}$$

$\theta=\int \omega_e dt+\theta_0$; θ_0 - Initial reference angle.

The qd equations are obtained as

$$V_q^{\ e}=R_s I_q^{\ e}+L_s pI_q^{\ e}+\omega_e L_s I_d^{\ e}+V_{c1}H_{q3}-V_{c2}H_{q1} \tag{7.32}$$

$$V_d^{\ e}=R_s I_d^{\ e}+L_s pI_d^{\ e}-\omega_e L_s I_q^{\ e}+V_{c1}H_{d3}-V_{c2}H_{d1} \tag{7.33}$$

$$V_0^{\ e}=R_s I_0^{\ e}+L_s pI_0^{\ e}+V_{c1}H_{03}-V_{c2}H_{01} \tag{7.34}$$

$$C_1 pV_{c1}=-I_{dc}+\frac{3}{2}\left[H_{q3}I_q^{\ e}+H_{d3}I_d^{\ e}+H_{03}I_0^{\ e}\right] \tag{7.35}$$

$$C_2 pV_{c2}=-\left[I_{dc}+\frac{3}{2}\left[H_{q1}I_q^{\ e}+H_{d1}I_d^{\ e}+H_{01}I_0^{\ e}\right]\right] \tag{7.36}$$

where

$$H_{q3}=\frac{2}{3}\left[H_{a3}\cos(\theta)+H_{b3}\cos(\theta-\beta)+H_{c3}\cos(\theta+\beta)\right]$$

$$H_{d3}=\frac{2}{3}\left[H_{a3}\sin(\theta)+H_{b3}\sin(\theta-\beta)+H_{c3}\sin(\theta+\beta)\right]$$

$$H_{03}=\frac{1}{3}\left[H_{a3}+H_{b3}+H_{c3}\right].$$

Similarly

$$H_{q1}=\frac{2}{3}\left[H_{a1}\cos(\theta)+H_{b1}\cos(\theta-\beta)+H_{c1}\cos(\theta+\beta)\right]$$

$$H_{d1}=\frac{2}{3}\left[H_{a1}\sin(\theta)+H_{b1}\sin(\theta-\beta)+H_{c1}\sin(\theta+\beta)\right]$$

$$H_{01} = \frac{1}{3}\left[H_{a1} + H_{b1} + H_{c1}\right].$$

Assuming

$$H_{q3} = \alpha H_q \; ; \; H_{d3} = \alpha H_d$$

$$H_{q1} = -\beta H_q \; ; \; H_{d1} = -\beta H_d \, .$$

By substituting the above expressions in Eqs. (7.32 - 7.36)

$$V_q^{\,e} = R_s I_q^{\,e} + L_s p I_q^{\,e} + \omega_e L_s I_d^{\,e} + \left(\alpha V_{c1} + \beta V_{c2}\right) H_q \tag{7.37}$$

$$V_d^{\,e} = R_s I_d^{\,e} + L_s p I_d^{\,e} - \omega_e L_s I_q^{\,e} + \left(\alpha V_{c1} + \beta V_{c2}\right) H_d \tag{7.38}$$

$$C_1 p V_{c1} = -I_{dc} + \frac{3}{2}\left[\alpha\left(H_q I_q^{\,e} + H_d I_d^{\,e}\right)\right] \tag{7.39}$$

$$C_2 p V_{c2} = -\left[I_{dc} - \frac{3}{2}\left[\beta\left(H_q I_q^{\,e} + H_d I_d^{\,e}\right)\right]\right] \, . \tag{7.40}$$

From the steady state analysis using Eq. (7.39) and (7.40) it can be shown that $\alpha = \beta$.

Substituting the above condition in Eqs. (7.37-7.38)

$$V_q^{\,e} = R_s I_q^{\,e} + L_s p I_q^{\,e} + \omega_e L_s I_d^{\,e} + \left(V_{dc}\right) H_q \tag{7.41}$$

$$V_d^{\,e} = R_s I_d^{\,e} + L_s p I_d^{\,e} - \omega_e L_s I_q^{\,e} + \left(V_{dc}\right) H_d \tag{7.42}$$

$$C_1 p V_{c1} = -I_{dc} + \frac{3}{2}\left[\left(H_q I_q^{\,e} + H_d I_d^{\,e}\right)\right] \tag{7.43}$$

$$C_2 p V_{c2} = -\left[I_{dc} - \frac{3}{2}\left[\left(H_q I_q^{\,e} + H_d I_d^{\,e}\right)\right]\right] \, . \tag{7.44}$$

7.6 Steady-State Analysis

The active and reactive power for a three-phase system is given by

$$P = \frac{3}{2}\left(V_q I_q + V_d I_d\right) \tag{7.45}$$

$$Q = \frac{3}{2}\left(V_d I_q - V_q I_d\right). \tag{7.46}$$

For unity power factor, the reactive power is zero. The condition for unity power is obtained by equating the reactive power to zero.

In synchronous reference frame, choose initial reference angle such that $V_q = V$ and $V_d = 0$. By substituting the qd voltages in Eq. (7.46),

$$Q = \frac{3}{2}\left(V_d I_q - V_q I_d\right) = 0$$

$$\Rightarrow V_q I_d = 0 \ .$$

But $V_q \neq 0$ and hence $I_d = 0$.

The steady state analysis is done for unity power factor condition; i.e., the d-axis component of the input current is zero $I_d = 0$ and also in the steady state analysis the derivative terms are made zero. Hence by applying the above conditions to Eqs. (7.41-7.44), the steady state equations are obtained as

$$V_q = R_s I_q + H_q V_{dc} \tag{7.47}$$

$$V_d = -\omega_e L_s I_q + H_d V_{dc} \tag{7.48}$$

$$0 = -I_{dc} + \frac{3}{2}\alpha H_q I_q \tag{7.49}$$

$$0 = -\left[I_{dc} - \frac{3}{2}\beta H_q I_q \right]. \tag{7.50}$$

By equating the above two equations, it is observed that $\alpha = \beta$.

By substituting the above condition and solving for unknown I_q, H_q, H_d

$$H_q = \frac{3R_L V_q - \sqrt{3}\left[-R_L\left(-3R_L {V_q}^2 + 8R_s {V_{dc}}^2\right)\right]^{1/2}}{6R_L V_{dc}}, \frac{3R_L V_q + \sqrt{3}\left[-R_L\left(-3R_L {V_q}^2 + 8R_s {V_{dc}}^2\right)\right]^{1/2}}{6R_L V_{dc}}$$

$$H_d = \frac{6V_{dc}R_L R_s + 3\omega_e L_s R_L V_q + \omega_e L_s \sqrt{3}\left[-R_L\left(-3R_L {V_q}^2 + 8R_s {V_{dc}}^2\right)\right]^{1/2}}{6R_L R_s V_{dc}},$$
$$\frac{6V_{dc}R_L R_s + 3\omega_e L_s R_L V_q - \omega_e L_s \sqrt{3}\left[-R_L\left(-3R_L {V_q}^2 + 8R_s {V_{dc}}^2\right)\right]^{1/2}}{6R_L R_s V_{dc}}$$

$$I_q = \frac{3R_L V_q + \sqrt{3}\left[-R_L\left(-3R_L {V_q}^2 + 8R_s {V_{dc}}^2\right)\right]^{1/2}}{6R_L R_s}, \frac{3R_L V_q - \sqrt{3}\left[-R_L\left(-3R_L {V_q}^2 + 8R_s {V_{dc}}^2\right)\right]^{1/2}}{6R_L R_s}.$$

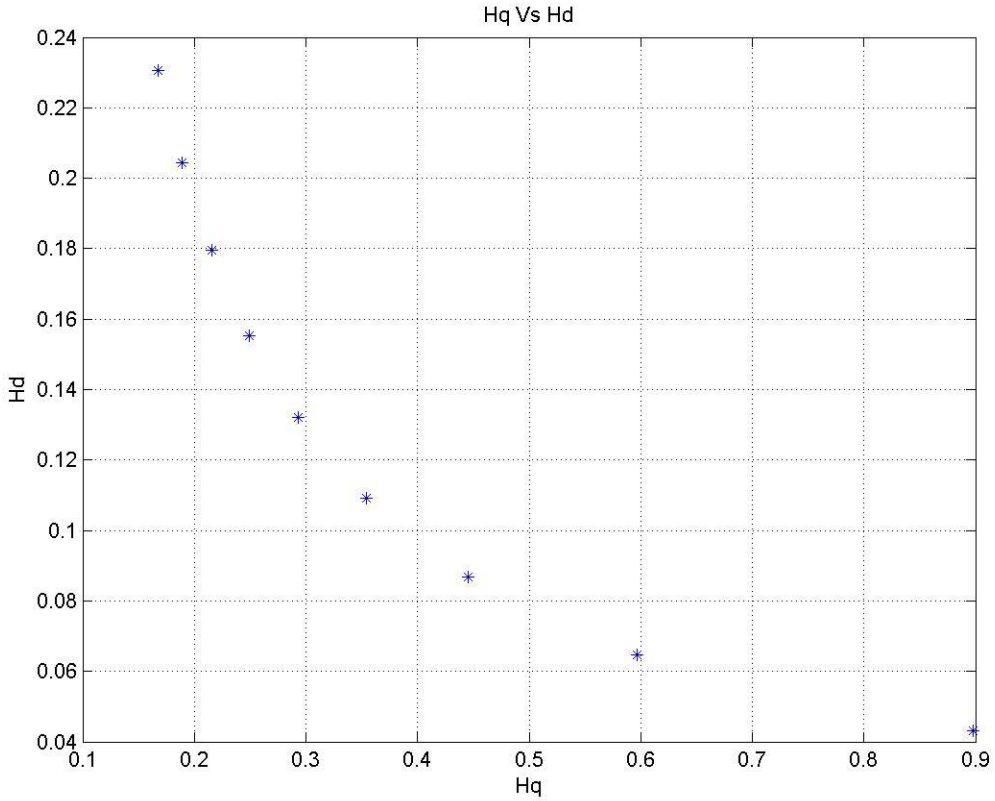


Figure 7.5: Plot of q-axis modulation against d-axis modulation for various dc voltages for unity power factor operation.

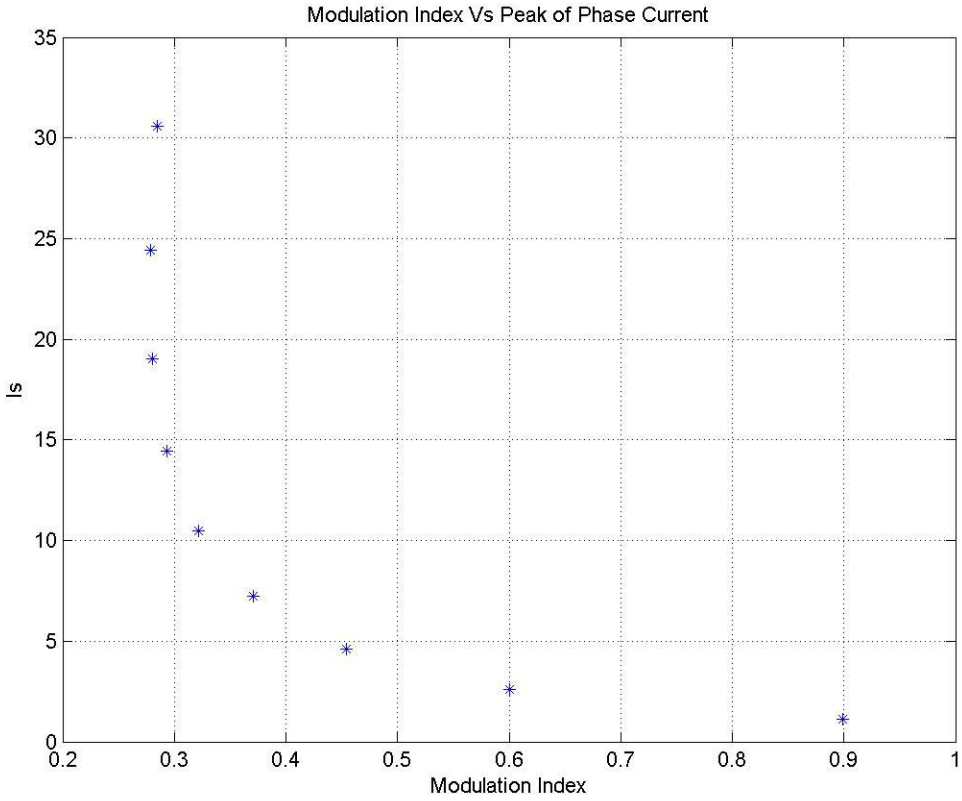


Figure 7.6: Plot of modulation index against peak of the phase current for various dc voltages for unity power factor operation.

Figures 7.5 and 7.6 are obtained using the steady state analysis. The plots are obtained by using the expressions for H_q, H_d, I_q. By varying the dc voltage from 70V to 700 V and each point of voltage increment, the expressions are evaluated and plotted. Figure 7.5 shows the plot of variation of the q-axis modulation index against the d-axis modulation index. Figure 7.6 shows the plot of the modulation index against the peak of the phase current. The plots are for unity power factor operation.

7.7 Open-loop Simulation of the Rectifier

From the steady-state analysis, choose a particular value of modulation index from the plot for H_q, H_d. Using the circuit parameters given below and using the modulation index, the converter is simulated.

7.7.1 Circuit Parameters

Input line resistance $R_s = 0.2\Omega$

Input line inductance $L_s = 10mH$

Input Supply Voltage $v_a = 80\cos(\omega t)$

$$v_b = 80\cos(\omega t - 120^0)$$

$$v_c = 80\cos(\omega t + 120^0)$$

Output dc-capacitance $C_1 = C_2 = 2200\mu F$

Load resistance $R_L = 75\Omega$

In the simulation, firstly the dq modulation signals are transformed to abc reference frame and these modulation signals are compared with the two triangles to obtain the switching; the PWM scheme is explained in Chapter 3 and using the equations mentioned above, the modulation scheme is implemented for unity power factor conditions and for two different values of the dc voltages.

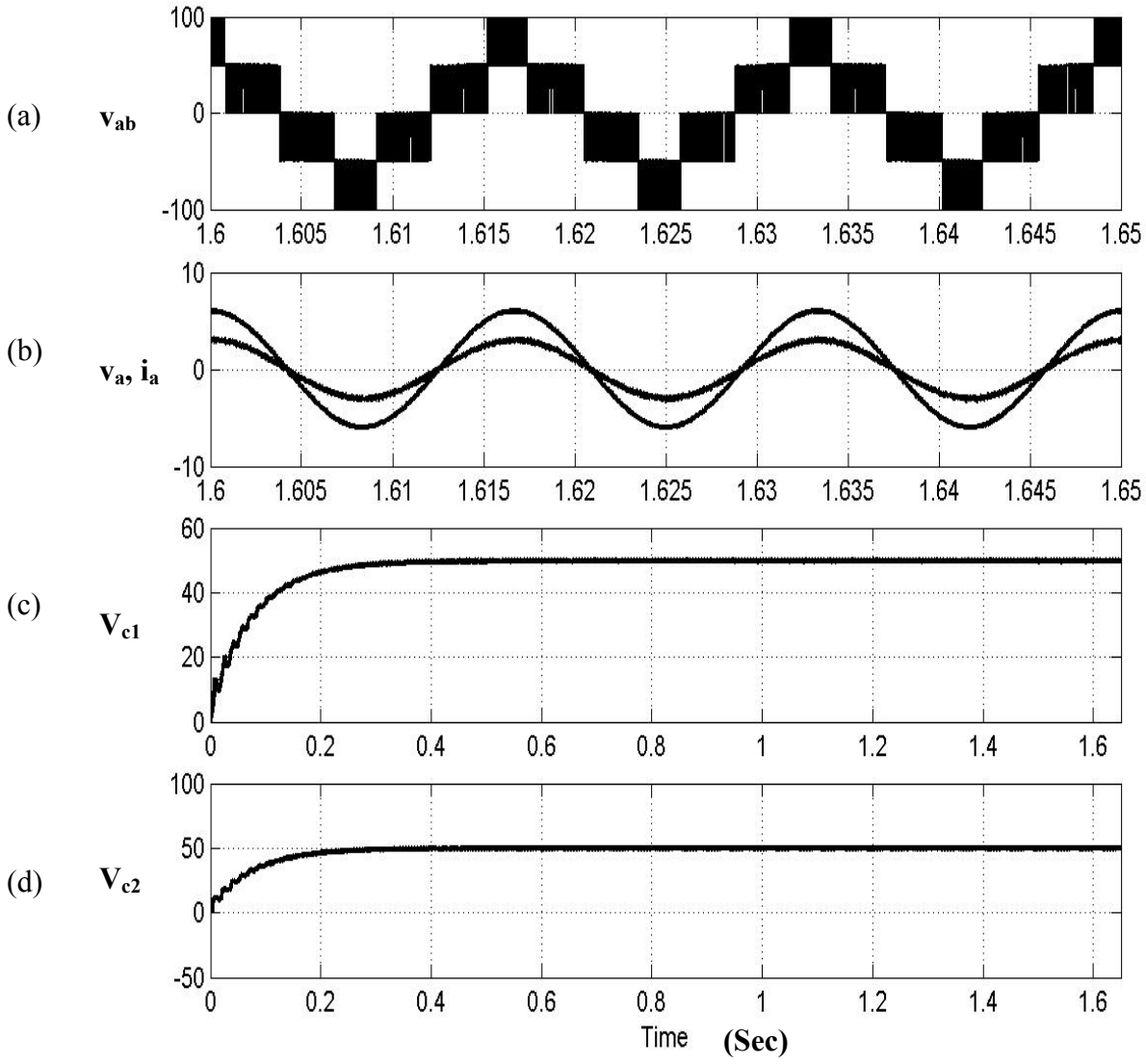


Figure 7.7: Open loop simulation of the rectifier: Operating Condition 1: $V_{dc} = 100V$. (a) Line-line voltage v_{ab} (b) Input phase voltage v_a and input phase current i_a showing the unity power factor operation (c), (d) Output Capacitor Voltages (V_{c1}, V_{c2}).

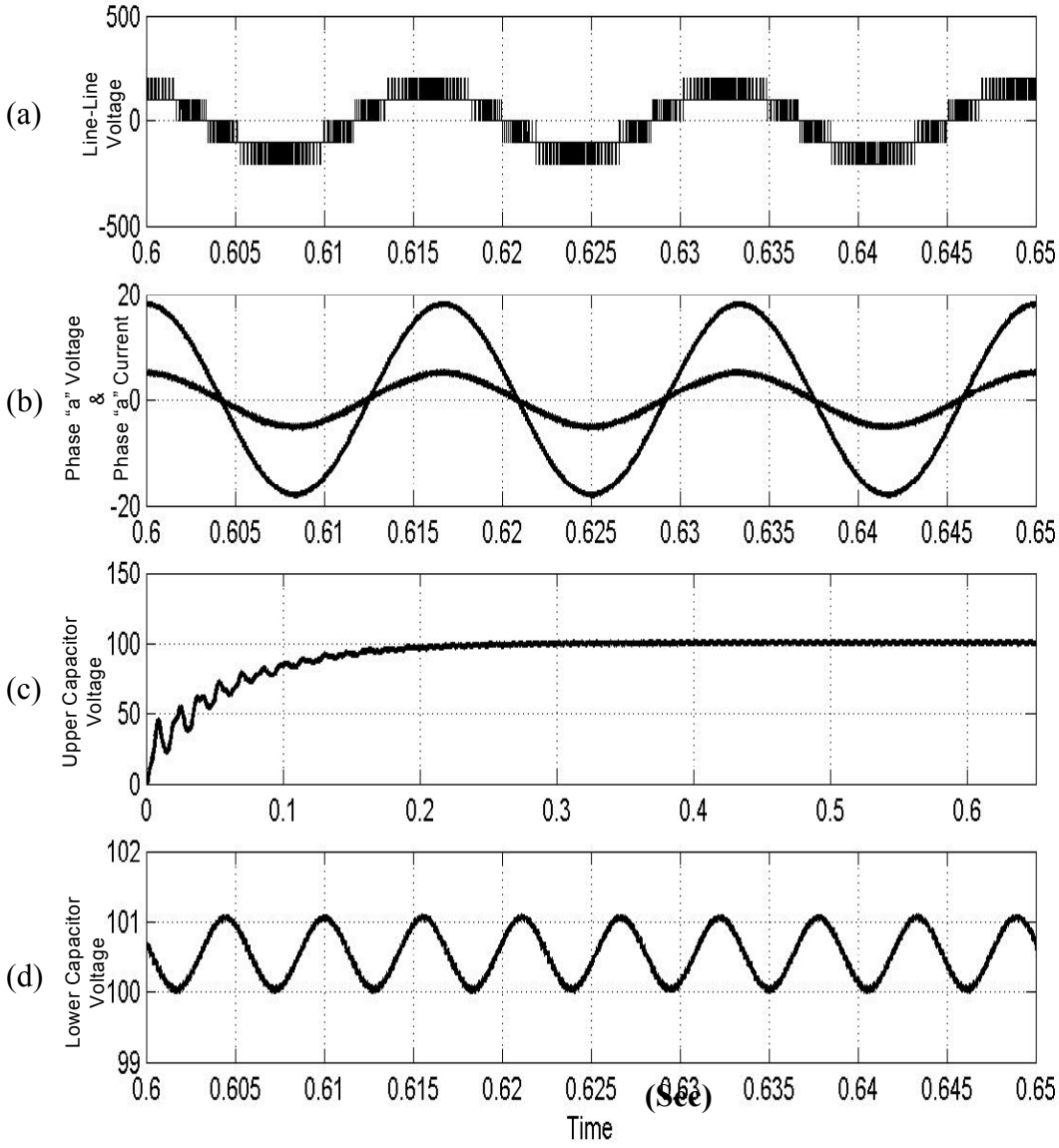


Figure 7.8: Open-loop simulation of the rectifier: Operating Condition 2: $V_{dc} = 200V$. (a) Line-line voltage v_{ab} (b) Input phase voltage v_a and input phase current i_a showing the unity power factor operation (c), (d) Output Capacitor Voltages (V_{c1}, V_{c2}).

Figure 7.7 and Figure 7.8 show the open loop simulation results for unity power factor operation for two operating conditions. Figure 7.7 shows the simulation results for an operating dc voltage of 100 V. Figure 7.7 (a) shows the line-to-line voltage and it shows the steps in the voltage waveform. Figure 7.7 (b) shows the unity power factor operation. Figure 7.7 (c) and (d) shows the two capacitor voltages and as can be seen that the neutral point voltage is very low, in the range of 1 V. Figure 7.8 gives the simulation results for other operating condition of V_{dc} = 200 V.

7.8 Control of Three-Leg Three Phase Three-Level Rectifier

The main objective of any control scheme is to regulate the actual quantity with the reference quantity. The proposed control scheme is intended to achieve the dc-link voltage constant, and to obtain unity power factor at the input side. Any quantity of the system can be set as the output of the controller provided a relation as to how the controlled quantity effects the variable taken as the output can be given, but this is usually a tedious job.

In the control of the rectifier two methods have been proposed. Both the control schemes are intended for the same objectives but the approach and the controllers used are different in the two cases.

7.8.1 Control Scheme A

In this particular scheme, the analysis and the control is done in a dq reference frame; i.e., all the quantities such as the voltages, currents, etc., are transformed to

another reference frame so as to make the time varying quantities to be time invariant quantities. Controlling the time invariant quantities is simple and can be achieved using a PI, PD, or PID controller. In the following control scheme a cascaded control structure is being used, i.e., the output of one controller is used to calculate the reference of the other controller. Hence the time response of the controllers becomes a main criterion in designing the control parameters.

From the dq analysis, Eq. (7.41) can be written as

$$R_s I_q^{\,e} + L_s p I_q^{\,e} = V_q^{\,e} - \omega_e L_s I_d^{\,e} - V_{dc} H_q .$$

Assuming $R_s I_q^{\,e} + L_s p I_q^{\,e} = \sigma_q$

$$\sigma_q = \frac{V_q^{\,e}}{L_s} - \omega_e I_d^{\,e} - \frac{V_{dc}}{L_s} H_q . \tag{7.51}$$

Similarly

$$R_s I_d^{\,e} + L_s p I_d^{\,e} = V_d^{\,e} + \omega_e L_s I_d^{\,e} - V_{dc} H_d .$$

Assuming $R_s I_d^{\,e} + L_s p I_d^{\,e} = \sigma_d$

$$\sigma_d = \frac{V_d^{\,e}}{L_s} + \omega_e I_q^{\,e} - \frac{V_{dc}}{L_s} H_d . \tag{7.52}$$

Adding the two capacitor equations Eq. (7.43) and Eq. (7.44)

$$Cp\left(V_{c1} + V_{c2}\right) = -I_{dc} + \frac{3}{2}\left[H_q I_q^{\,e} + H_d I_d^{\,e} + H_o I_o^{\,e}\right] - I_{dc} + \frac{3}{2}\left[H_q I_q^{\,e} + H_d I_d^{\,e} + H_o I_o^{\,e}\right]. \tag{7.53}$$

Under balanced conditions $I_o = 0$.

Writing Eq. (7.53) in a more simplified form as

$$Cp\left(V_{dc}\right) = -2I_{dc} + 3\ [H_q I_q^{\,e} + H_d I_d^{\,e}]. \tag{7.54}$$

From Eqs. (7.51)-(7.52) the expression for modulation signals in qd can be obtained

$$H_q = \frac{-\sigma_q L_s - \omega_e {I_d}^e L_s + {V_q}^e}{V_{dc}} \tag{7.55}$$

$$H_d = \frac{-\sigma_d L_s + \omega_e {I_q}^e L_s + {V_d}^e}{V_{dc}}. \tag{7.56}$$

Substituting these expression in the capacitor equation

$$Cp(V_{dc}) = -2I_{dc} + 3\left[\left(\frac{-\sigma_q L_s - \omega_e {I_d}^e L_s + {V_q}^e}{V_{dc}}\right){I_q}^e + \left(\frac{-\sigma_d L_s + \omega_e {I_q}^e L_s + {V_d}^e}{V_{dc}}\right){I_d}^e\right]$$

$$\Rightarrow V_{dc} Cp(V_{dc}) = -2I_{dc} + 3\left[\left(-\sigma_q L_s - \omega_e {I_d}^e L_s + {V_q}^e\right){I_q}^e + \left(-\sigma_d L_s + \omega_e {I_q}^e L_s + {V_d}^e\right){I_d}^e\right].$$

Assuming $\frac{1}{2} Cp {V_{dc}}^2 = \delta_v$.

Now arranging the terms in the above equation and simplifying

$$\frac{3}{2}\left[{V_q}^e {I_q}^e + {V_d}^e {I_d}^e\right] = \frac{\delta_v}{2} + \frac{3}{2}\left[{I_q}^e \sigma_q L_s + {I_d}^e \sigma_d L_s\right] + V_{dc} I_{dc}$$

where $P^* = \frac{3}{2}\left[{V_q}^e {I_q}^e + {V_d}^e {I_d}^e\right]$.

Hence

$$P^* = \frac{\delta_v}{2} + \frac{3}{2}\left[{I_q}^e \sigma_q L_s + {I_d}^e \sigma_d L_s\right] + V_{dc} I_{dc} \tag{7.57}$$

where P^* is the required power to meet the load.

For unity power factor operation, reactive power is zero, i.e., $Q^* = 0$;

The active and reactive power for a three-phase balanced system is

$$P^* = \frac{3}{2}\left({V_q}^e {I_q}^e + {V_d}^e {I_d}^e\right) \tag{7.58}$$

$$Q^* = \frac{3}{2}\left({V_d}^e {I_q}^e - {V_q}^e {I_d}^e\right). \tag{7.59}$$

By solving P^* and Q^* for ${I_q}^e$ and ${I_d}^e$

$$I_q^{\ e} = \frac{2}{3\Delta}\left[P^* V_q^{\ e} + Q^* V_d^{\ e}\right] \tag{7.60}$$

$$I_d^{\ e} = \frac{2}{3\Delta}\left[P^* V_d^{\ e} - Q^* V_q^{\ e}\right] \tag{7.61}$$

where $\Delta = P^{*2} + Q^{*2}$.

Figure 7.9 shows the schematic of the control scheme A. The voltage control is called the outer control loop and the current controllers are the inner control loop. Hence the time response of the current controllers has to be faster than that the voltage controller by at least 10 times. In the control scheme the square of the actual dc voltage $V_{dc}^{\ 2}$ is compared with the reference dc voltage $V_{dc}^{\ *2}$. The error signal is passed through a PI controller K_v whose structure is explained in the next section. The output of this controller is assumed as σ_v. Using expressions (7.60) and (7.61) the reference qd currents $I_q^{\ *}$ and $I_d^{\ *}$ can be calculated. These reference currents are compared with the actual qd currents. The errors are passed through the two current controllers K_q and K_d. The outputs of these controllers are assumed as σ_q and σ_d. Using expressions (7.55) and (7.56) the qd modulation signals can be obtained. These qd signals can be transformed back to the abc reference frame to obtain the actual modulation signals. The carrier based PWM is used to obtain the gating signals for the devices as explained in Chapter 3. These modulation signals when compared with the two triangles, the switching functions for the devices can be obtained.

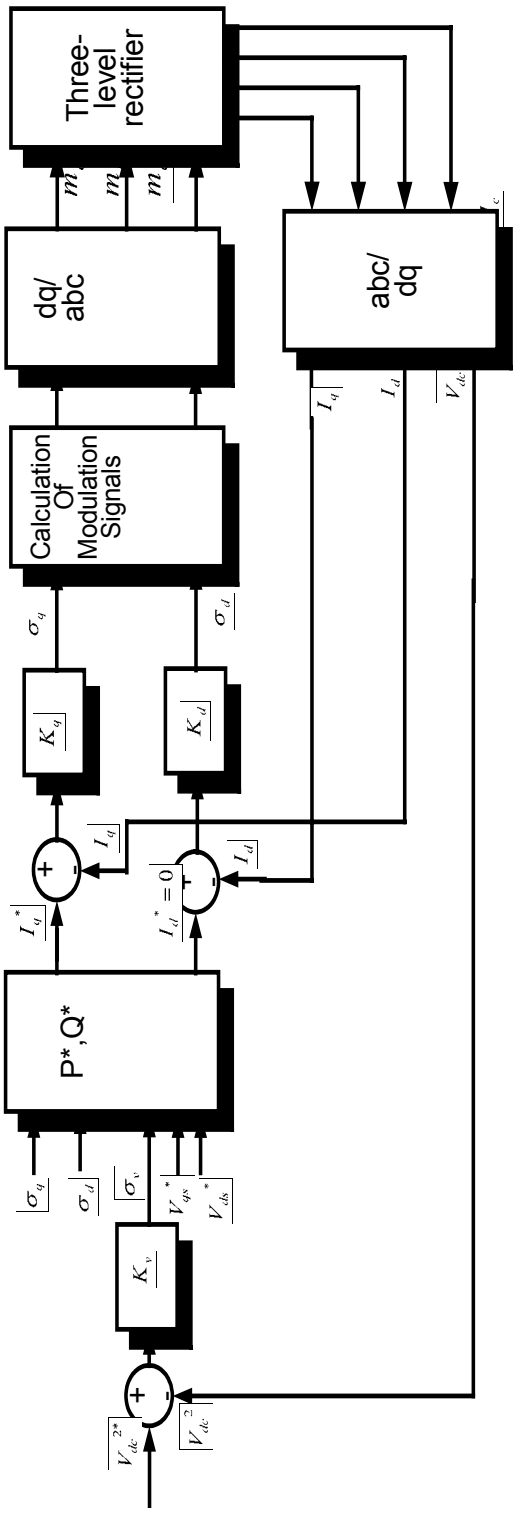


Figure 7.9 Block diagram of the control scheme A

7.8.2 Controller Structure and Design

It is clear from the analysis that the controllable quantities are dc signals. To control a dc quantity a simple PI, PD, or PID can be used. In the present case a PI control structure is being used.

7.8.3.Voltage Controller

From Figure 7.10

$$\left(V_{dc}^{*2} - V_{dc}^{2}\right)K_v = \frac{1}{2}CpV_{dc}^{2}$$

$$\Rightarrow \frac{1}{2}CsV_{dc}^{2} + K_vV_{dc}^{2} = K_vV_{dc}^{*2}$$

$$\Rightarrow \left(\frac{1}{2}Cs + K_v\right)V_{dc}^{2} = K_vV_{dc}^{*2}$$

$$\Rightarrow \frac{V_{dc}^{2}}{V_{dc}^{*2}} = \frac{K_v}{K_v + \frac{Cs}{2}} \quad .$$

Assuming the structure of the controller K_v as $K_p + \frac{K_i}{s}$ and by substituting this in to the above transfer function

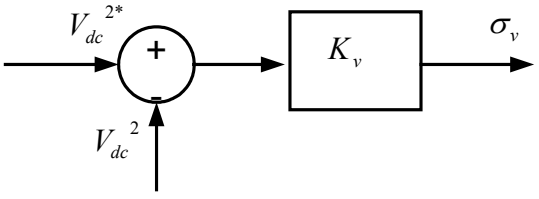


Figure 7.10: Structure of the voltage controller.

$$\frac{V_{dc}^{\ 2}}{V_{dc}^{\ *2}} = \frac{K_p + \frac{K_i}{s}}{K_p + \frac{K_i}{s} + \frac{Cs}{2}}$$
$$= \frac{sK_p + K_i}{Cs^2 + 2sK_p + 2K_i} \quad .$$

One method of obtaining the controller parameters is by comparing the denominator of the transfer function with Butter-Worth polynomial. The order of the polynomial is same as the order of the system. The Butter-worth method locates the Eigen values of the transfer function uniformly in the left half of the s-plane, on a circle of radius ω_0, with its center at the origin. Hence in the present case the transfer function is of second order system and hence the denominator is compared with the second order Butterworth polynomial.

The second order Butter Worth polynomial is given by

$$s^2 + \sqrt{2}s\omega_0 + \omega_0^{\ 2} = 0 \,. \tag{7.62}$$

Hence by comparing the coefficients of same exponentials

$$K_p = \frac{C\omega_0}{\sqrt{2}} \text{ and } K_i = \frac{C\omega_0^{\ 2}}{2} \,. \tag{7.63}$$

7.8.4 Current Controller

Using similar analysis the transfer function of the q-axis current can be obtained as follows:

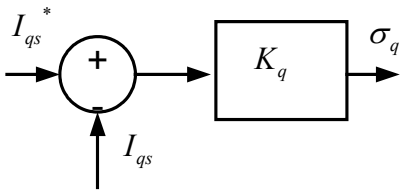


Figure 7.11: Structure of the current controller

$$\frac{I_q}{I_q^*} = \frac{sK_p + K_i}{s^2 + s\left(\frac{R_s}{L_s} + K_p\right) + K_i}. \tag{7.64}$$

Again the controller parameters can be obtained by comparing the denominator with the Butterworth polynomial as

$$K_p = \sqrt{2}\omega_0 - \frac{R_s}{L_s} \text{ and } K_i = {\omega_0}^2. \tag{7.65}$$

As explained above the speed of the controller depends on ω_0. ω_0 of current controller should be at least ten times greater than that of the voltage controller. The d-axis current controller has the similar kind of structure. The transfer function of the d-axis current is

$$\frac{I_d}{I_d^*} = \frac{sK_p + K_i}{s^2 + s\left(\frac{R_s}{L_s} + K_p\right) + K_i}. \tag{7.66}$$

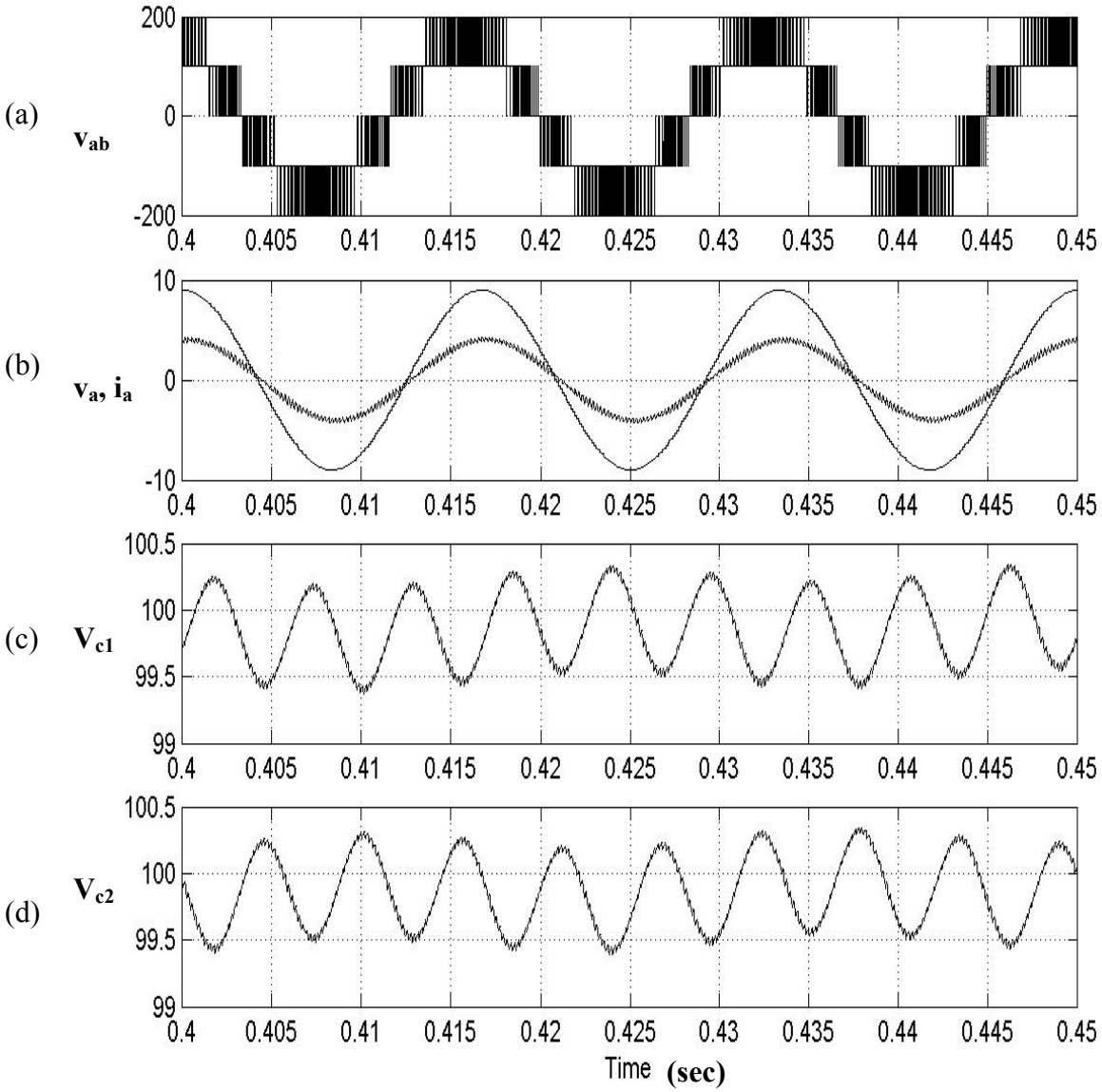


Figure 7.12: Simulation results of control scheme A: Rectifier mode of operation with a load resistance of 75**Ω**. : (a) Line-line voltage v_{ab} (b) Input phase voltage v_a and input phase current i_a showing the unity power factor operation (c), (d) Output Capacitor Voltages (V_{c1}, V_{c2}).

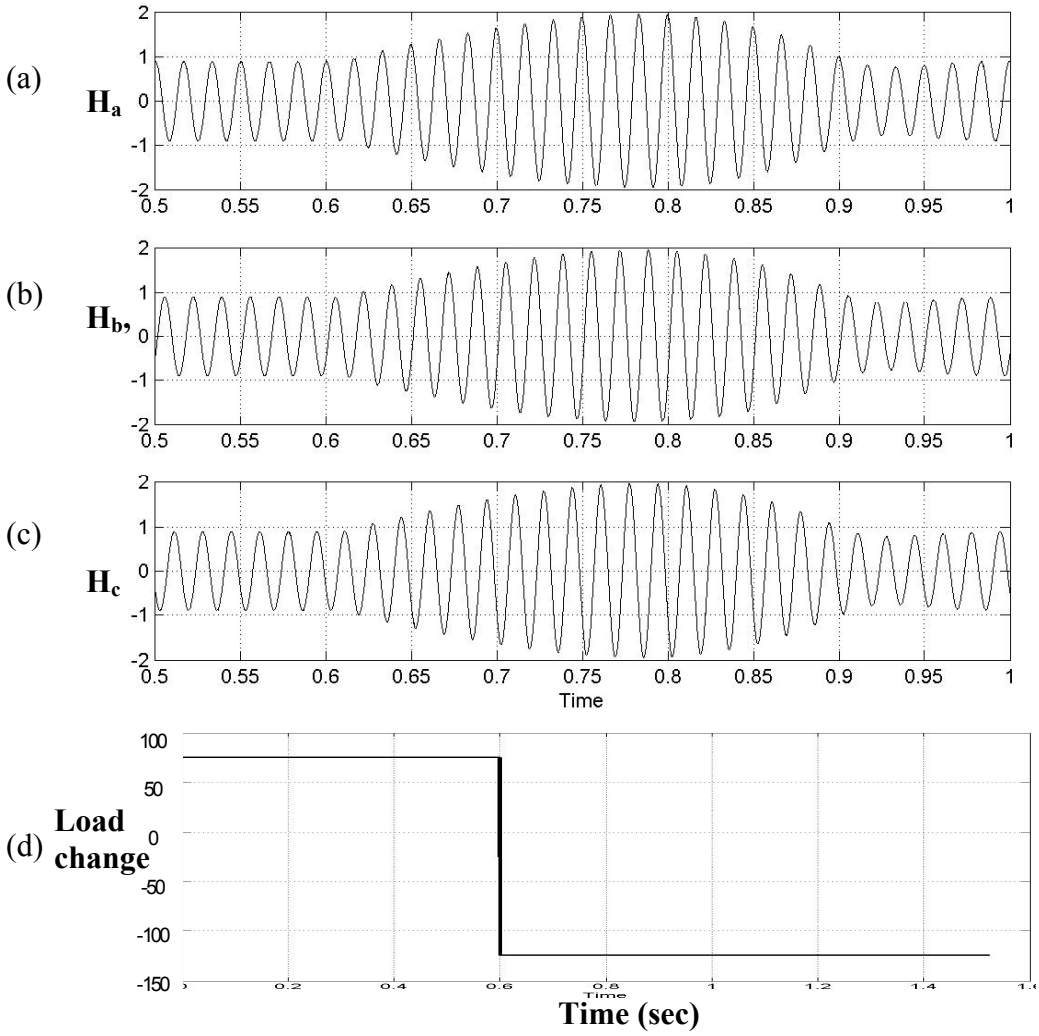


Figure 7.13: Modulation signals during the transition from rectifier mode of operation to inverter mode of operation. (a) Phase a modulation signal (H_a) (b) Phase b modulation signal (H_b) and (c) Phase c modulation signal (H_c). (d) Plot showing change in load i.e., from the rectifier mode of operation to inverter mode of operation at t = 0.6 sec.

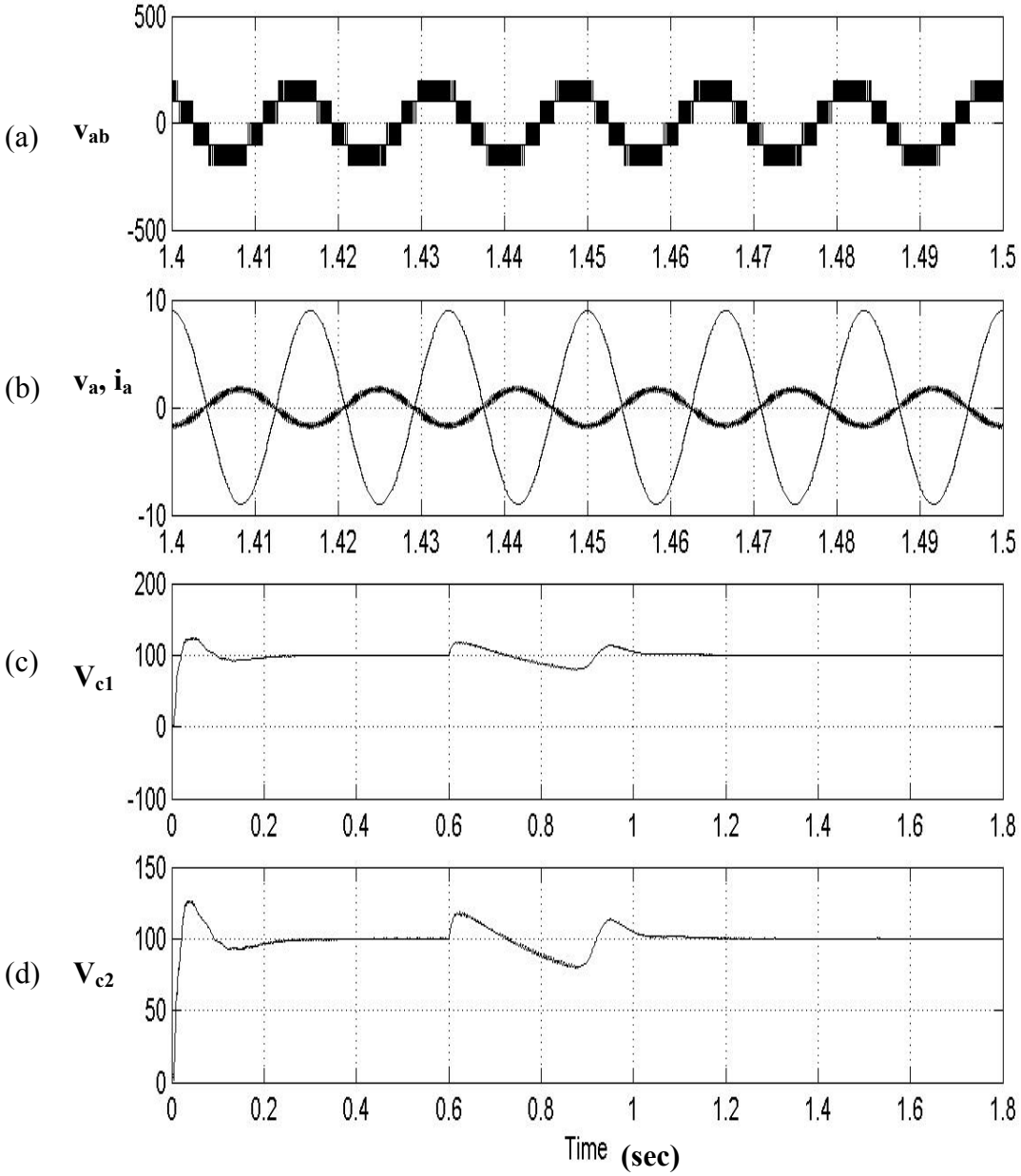


Figure 7.14: Simulation results of control scheme A: Inverter mode of operation, , load change at time t = 0.6sec $V_{dc} = 200V$. (a) Line-line voltage v_{ab} (b) Input phase voltage v_a and input phase current i_a showing the unity power factor operation (c), (d) Output Capacitor Voltages (V_{c1}, V_{c2}).

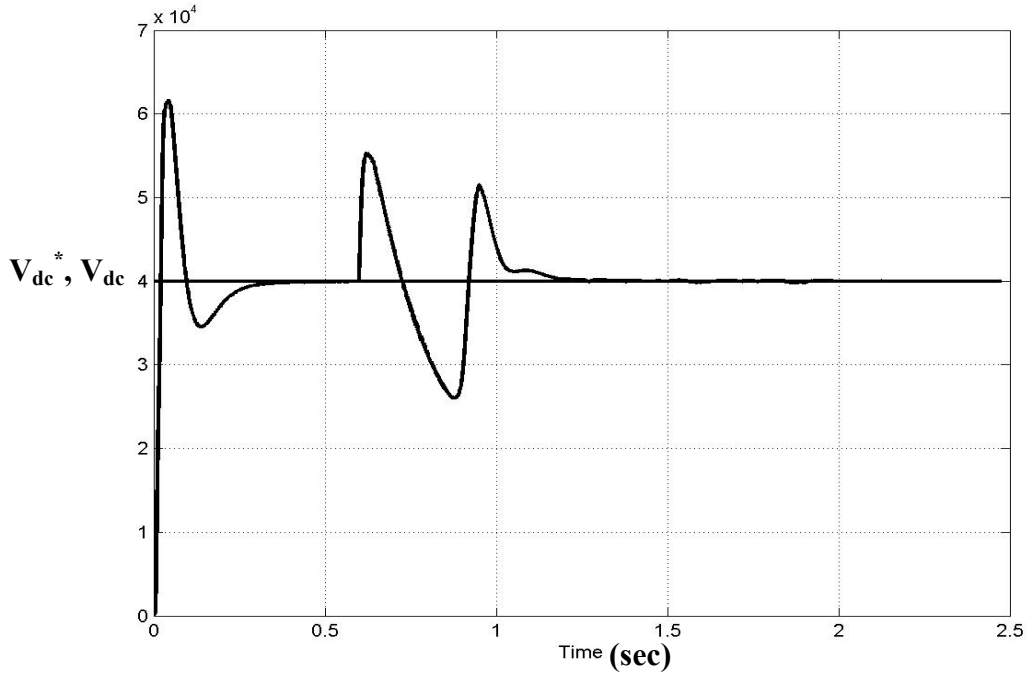


Figure 7.15: Control scheme A: Reference dc voltage and the actual dc voltage. V_{dc}^{*2} & V_{dc}^{2}

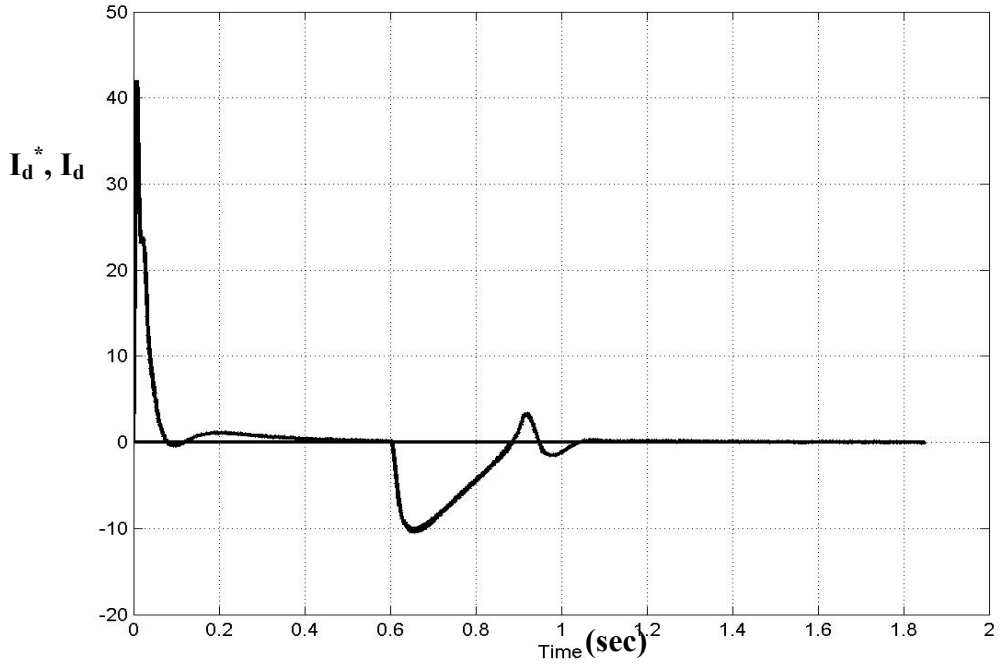


Figure 7.16: Control scheme A: Reference d-axis current and the actual d-axis current

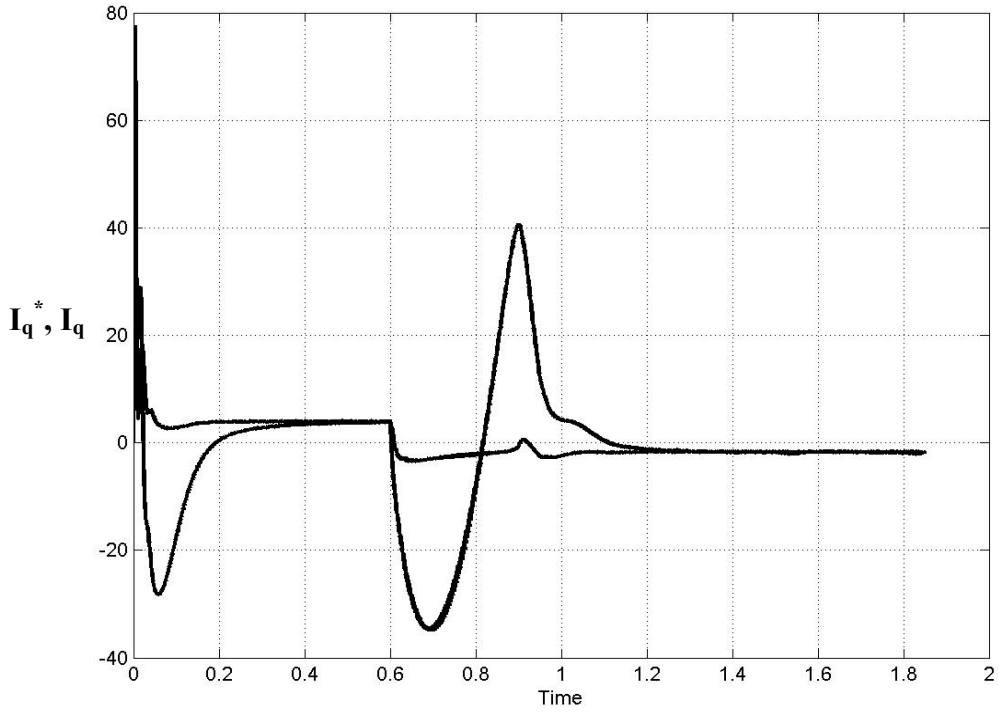


Figure 7.17: Control scheme A: Reference q-axis current and the actual q-axis current.

Figures 7.12 to 7.17 show the simulation results for control scheme A. Figure 7.12 shows the steady state plots after the capacitor voltages have settled. The reference capacitor voltage in the present case is taken as 200 V and hence the steady state values of the capacitors should be 100 V each. Figure 7.12 (a) shows the line-line voltage V_{ab}; Figure 7.12 (b) shows the unity power factor operation; Figure 7.12 (c) and (d) shows the two capacitor voltages and can be seen that the voltages settle to the reference voltages. Figure 7.13 (d) shows the change of load; i.e., change of operation from rectifier to inverter mode. Figure 7.13 shows the modulation signals during the change of load. Figure 7.14 shows the steady state plots in the inverter mode of operation. The load is changed from 75 Ω to –100 Ω. Negative load indicates inverter mode of operation; i.e.,

the power is fed back to the supply. As seen from the results, the control scheme works effectively even in the inverter mode of operation as it achieves the capacitor voltage control and also the unity power factor operation even in the inverter mode. Figure 7.15 shows the tracking of the capacitor voltages. It can be seen that there are some dips because of the load change and also initially it took some time to settle to the reference voltage. Figure 7.16 shows the tracking of the d-axis current. For unity power factor operation d-axis component has to be zero and it is clear from the plot that d-axis current is tracked well. Figure 7.17 shows the tracking active component of the current or the q-axis current.

7.8.5 Control Scheme B

In the previous control scheme A, the analysis is in qd reference frame; i.e., all the quantities are transformed to synchronous reference frame so as to make the quantities time invariant. The control structure is simple in case of the dc quantities, but when it comes to implementation it becomes complex. Because all the quantities should be transformed to synchronous reference frame and after that again the modulation signals have to be transformed back to abc reference. Hence a new control scheme is being formulated using the natural variables; i.e., control the actual signals without any transformation. Hence the control becomes simple.

$$v_a = i_a R_s + L_s p i_a + H_a V_{dc} + V_{20} \tag{7.67}$$

$$v_b = i_b R_s + L_s p i_b + H_b V_{dc} + V_{20} \tag{7.68}$$

$$v_c = i_c R_s + L_s p i_c + H_c V_{dc} + V_{20}. \tag{7.69}$$

For a balanced case, $i_c = -(i_a + i_b)$.

By substituting I_c in Eq. (7.69)

$$v_c = -(i_a + i_b)R_s - L_s p(i_a + i_b) + H_c V_{dc} + V_{20}.$$

To eliminate the term V_{20}, subtract Eqs. (7.67), (7.69) and Eqs. (7.67), (7.69)

$$v_{ac} = 2i_a R_s + 2L_s p i_a + i_b R_s + L_s p i_b + H_{ac} V_{dc} \tag{7.70}$$

$$v_{bc} = 2i_b R_s + 2L_s p i_b + i_a R_s + L_s p i_a + H_{bc} V_{dc}. \tag{7.71}$$

Solving for $L_s p I_a$ and $L_s p I_b$

$$L_s p i_a = \frac{-v_{bc} + 2v_{ac} + H_{bc} v_{dc} - 2H_{ac} V_{dc}}{3} - I_a R_s.$$

Rearranging the terms and simplifying

$$3(i_a R_s + L_s p i_a) = -v_{bc} + 2v_{ac} + H_{bc} V_{dc} - 2H_{ac} V_{dc}.$$

Assuming $\sigma_a = 3(i_a R_s + L_s p i_a)$.

Hence

$$\sigma_a = -v_{bc} + 2v_{ac} + H_{bc} V_{dc} - 2H_{ac} V_{dc}. \tag{7.72}$$

Similarly

$$\sigma_b = -v_{ac} + 2v_{bc} + H_{ac} V_{dc} - 2H_{bc} V_{dc}. \tag{7.73}$$

From the above Eqs. (7.72) and (7.73), solving for H_{ac}, H_{bc}

$$H_{ac} = \frac{3v_{ac} - \sigma_b - 2\sigma_a}{3V_{dc}} \tag{7.74}$$

$$H_{bc} = \frac{3v_{bc} - \sigma_a - 2\sigma_b}{3V_{dc}}. \tag{7.75}$$

The capacitor equation is

$$CpV_{dc} = -2I_{dc} + 2H_a i_a + 2H_b i_b + 2H_c i_c . \tag{7.76}$$

Again substituting for I_c

$$CpV_{dc} = -2I_{dc} + 2H_{ac} i_a + 2H_{bc} i_b . \tag{7.77}$$

By substituting the expressions for H_{ac}, H_{bc} from Eqs. (7.74)-(7.75)

$$CpV_{dc} = -2I_{dc} + 2\left(\frac{3v_{ac} - \sigma_b - 2\sigma_a}{3V_{dc}}\right) i_a + 2\left(\frac{3v_{bc} - \sigma_a - 2\sigma_b}{3V_{dc}}\right) i_b . \tag{7.78}$$

By simplifying the equation and writing in terms of the phase voltages

$$\frac{3}{2} CpV_{dc}{}^2 = -6I_{dc}V_{dc} + 6I_a\left(v_a - v_c\right) + 6i_b\left(v_b - v_c\right) - 2i_a\sigma_b - 4i_a\sigma_a - 2i_b\sigma_a - 4i_b\sigma_b . \tag{7.79}$$

For unity power factor operation

$i_a = Kv_a$ and $i_b = Kv_b$.

Hence substituting the above condition in Eq. (7.79) and simplifying

$$\frac{3}{2} CpV_{dc}{}^2 = -6I_{dc}V_{dc} + K\left[6\left(v_a{}^2 + v_b{}^2 + v_c{}^2\right) - 2\sigma_a v_{ac} - 2\sigma_b v_{bc}\right].$$

Assuming $\frac{3}{2} CpV_{dc}{}^2 = \sigma_v$ and solving for value of K

$$K = \frac{\sigma_v + 6I_{dc}V_{dc}}{\Delta} . \tag{7.80}$$

where $\Delta = \left[6\left(v_a{}^2 + v_b{}^2 + v_c{}^2\right) - 2\sigma_a v_{ac} - 2\sigma_b v_{bc}\right].$

Hence the reference frame currents can be calculated as

$$i_a{}^* = Kv_a$$
$$i_b{}^* = Kv_b \ .$$

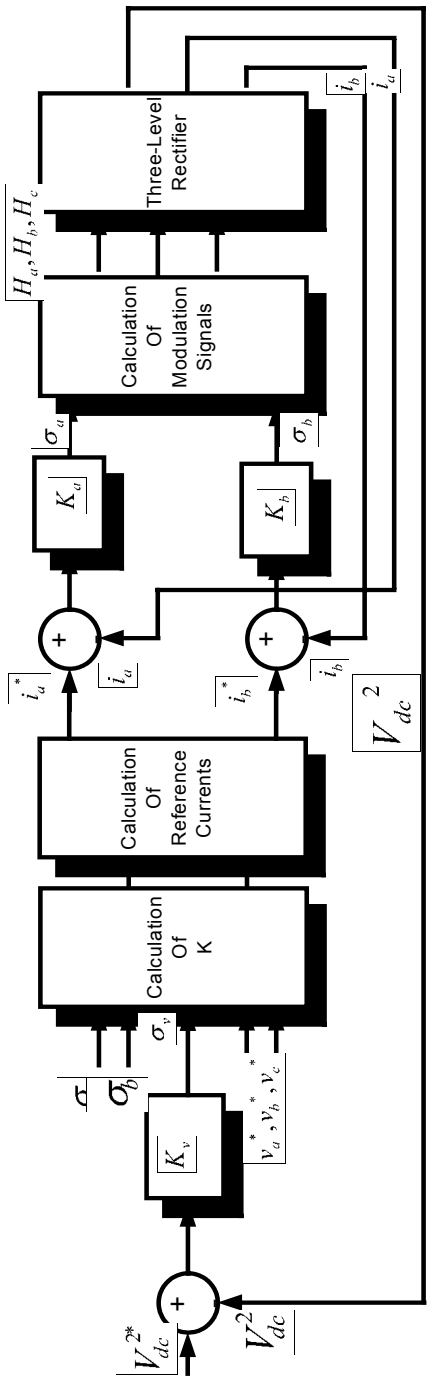


Figure 7.18: Block diagram of the control scheme B

Figure 7.18 shows the schematic of the control scheme B. Similar to control scheme A, scheme B also has the voltage control called the outer control loop and the current controllers as the inner control loop. Hence the time response of the current controllers has to be faster than the voltage controller at least by 10 times. In the control scheme the square of the actual dc voltage $V_{dc}^{\ 2}$ is compared with the reference dc voltage $V_{dc}^{\ *2}$. The error signal is passed through a PI controller K_v whose structure is explained in the next section. The output of this controller is assumed as σ_v. Using expression (7.80) the value of K is calculated and thereby the reference currents $i_a^{\ *}$ and $i_b^{\ *}$ can be calculated. These reference currents are compared with the actual currents. The errors are passed through the two current controllers K_a and K_b. The output of these controllers is assumed as σ_a and σ_b. Using expressions (7.74) and (7.75) the modulation signals can be obtained.

7.8.6 Controller Structure and Design

It is clear that the controllable quantities are dc signal in case of voltage and ac signals in case of currents. Hence in the control of ac quantity a simple PI, PD, or PID cannot be used. Hence a new controller called natural reference frame controller is being used.

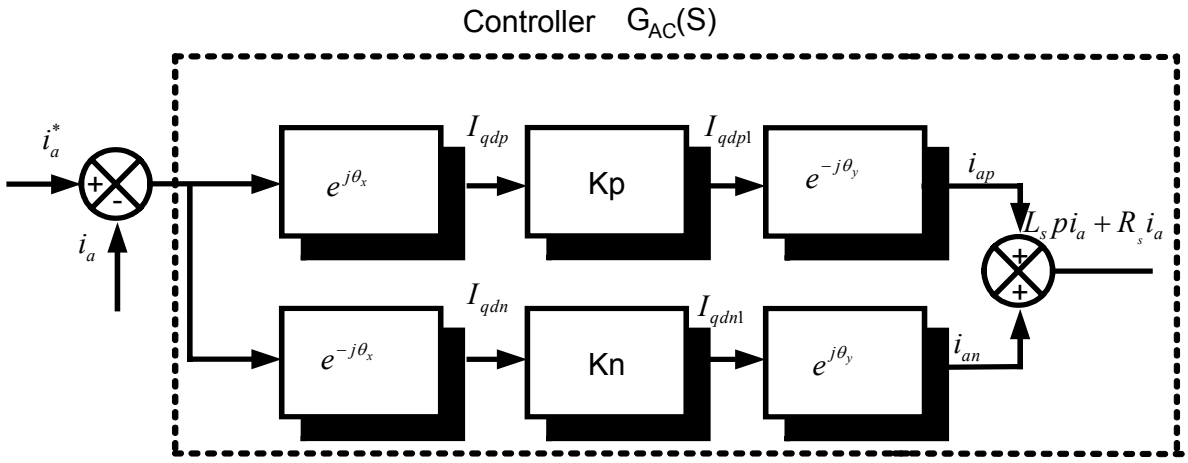


Figure 7.19: Structure of the controller

7.8.7 Natural Reference Frame Controller

The block diagram of the controller is outlined in Figure 7.19. In this scheme currents are being controlled and hence the inverter currents are used as the feedback signals. The currents i_a, i_b are taken from the inverter and are compared with the reference current signals i_a^*, i_b^*.

The errors of the currents are firstly transformed to positive and negative synchronous reference frames; i.e., θ_x and $-\theta_x$. Hence the output of the transformation block is

$$I_{qdp} = (i_a^* - i_a)e^{i\theta_x} \tag{7.67}$$

$$I_{qdn} = (i_a^* - i_a)e^{-i\theta_x} \tag{7.68}$$

where $\theta_x = \omega_e t + \theta_{x0}$; θ_{x0} - Initial reference angle.

After transformation the output signals are dc quantities. The signals are passed through these controllers whose transfer function is given by K_p (p) and K_n (p). Hence the output of the regulators is

$$I_{qdp1} = (i_a^* - i_a)e^{i\theta_x} K_p(p) \tag{7.69}$$

$$I_{qdn} = (i_a^* - i_a)e^{-i\theta_x} K_n(p)\,. \tag{7.70}$$

Now these signals are again transformed back to the abc reference frame with some delay angle ϕ_1 ; i.e., $\theta_y = \omega_e t + \theta_{x0} - \phi_1, \theta_y = -\omega_e t + \theta_{x0} - \phi_1$. Hence the resulting signals from these transformation blocks are

$$i_{ap} = (i_a^* - i_a)e^{i(\theta_x - \theta_y)} K_p(p - j\omega)\,. \tag{7.70}$$

$$i_{an} = (i_a^* - i_a)e^{-i(\theta_x - \theta_y)} K_n(p + j\omega)\,. \tag{7.71}$$

Let $\theta_x - \theta_y = \phi_1$; then

$$i_{ap} = (i_a^* - i_a)e^{i\phi_1} K_p(p - j\omega) \tag{7.72}$$

$$i_{an} = (i_a^* - i_a)e^{-i\phi_1} K_n(p + j\omega)\,. \tag{7.73}$$

Now take the sum of the two signals i_{ap}, i_{an} to get the output of the controller, which is equal to $3\left(R_s i_a + L_s p i_a\right)$.

$$3\left(R_s i_a + L_s p i_a\right) = (i_a^* - i_a)e^{i\phi_1} K_p(p - j\omega) + (i_a^* - i_a)e^{-i\phi_1} K_n(p + j\omega)$$

$$= (i_a^* - i_a)[e^{i\phi_1} K_p(p - j\omega) + e^{-i\phi_1} K_n(p + j\omega)]$$

By simplifying the above equation the transfer function of the system is obtained as

$$\frac{i_a}{i_a^*} = \frac{e^{i\phi_1} K_p(p - j\omega) + e^{-i\phi_1} K_n(p + j\omega)}{3R_s + 3L_s p + e^{i\phi_1} K_p(p - j\omega) + e^{-i\phi_1} K_n(p + j\omega)}\,. \tag{7.74}$$

In this particular case assume the controller to be a PI controller whose transfer function is given as

$$K_p(p) = k_p + \frac{k_{ip}}{p}$$
$$K_n(p) = k_n + \frac{k_{in}}{p} \quad . \tag{7.75}$$

Hence, by substituting the above transfer functions in (7.67) and simplifying,

$$\frac{i_a}{i_a^*} = \frac{e^{i\phi_1}(p+j\omega)[k_p(p-j\omega)+k_{ip}] + e^{-i\phi_1}(p-j\omega)[k_n(p+j\omega)+k_{in}]}{(3R_s+3L_sp)(p^2+\omega^2) + e^{i\phi_1}(p+j\omega)[k_p(p-j\omega)+k_{ip}] + e^{-i\phi_1}(p-j\omega)[k_n(p+j\omega)+k_{in}]}.$$

For simplicity, if $k_{ip} = k_{in} = k_i; k_n = k_p = k_p$, then

$$\frac{i_a}{i_a^*} = \frac{p^2 2k_p\cos\phi_1 + p2k_i\cos\phi_1 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}{3L_sp^3 + p^2\left[2k_p\cos\phi_1 + 3R_s\right] + p[2k_i\cos\phi_1 + 3\omega^2 L_s] + 3R_s\omega^2 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}.$$

Similar analysis can be done for the phase B current and transfer function is obtained as

$$\frac{i_b}{i_b^*} = \frac{p^2 2k_p\cos\phi_1 + p2k_i\cos\phi_1 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}{3L_sp^3 + p^2\left[2k_p\cos\phi_1 + 3R_s\right] + p[2k_i\cos\phi_1 + 3\omega^2 L_s] + 3R_s\omega^2 + 2\cos\phi_1\omega^2 k_p - 2k_i\omega\sin\phi_1}.$$

In designing the parameters of the controller, compare the denominator of the transfer function with Butterworth Polynomial. The Butter-worth polynomial for the third order is as follows:

$$p^3 + 2p^2 w_0 + 2pw_0^2 + w_0^3 = 0\,. \tag{7.76}$$

Hence by comparing the denominator of the transfer function with above polynomial

$$\frac{3R_s + 2\cos\phi_1 k_p}{3L_s} = 2\omega_0 \tag{7.77}$$

$$\frac{3\omega^2 L_s + 2\cos\phi_1 k_i}{3L_s} = 2{\omega_0}^2 \tag{7.78}$$

$$\frac{3R_s\omega^2 + 2\cos\phi_1 k_p\omega^2 - 2k_i\omega\sin\phi_1}{3L_s} = {\omega_0}^3 . \tag{7.79}$$

Hence by solving the above three equations for the three unknowns k_i, k_p, ω_0 and by varying the delay angle ϕ_1 the controller parameters can be calculated.

7.8.8 Voltage Controller

The voltage control structure is same as discussed in control scheme A. Hence the transfer function of the controller is as follows:

$$\frac{{V_{dc}}^2}{{V_{dc}}^{*2}} = \frac{sK_p + K_i}{Cs^2 + 2sK_p + 2K_i} .$$

The second order Butter Worth polynomial is given by

$$s^2 + \sqrt{2}s\omega_0 + {\omega_0}^2 = 0 . \tag{7.80}$$

Hence by comparing the coefficients of same exponentials

$$K_p = \frac{C\omega_0}{\sqrt{2}} \text{ and } K_i = \frac{C{\omega_0}^2}{2} . \tag{7.81}$$

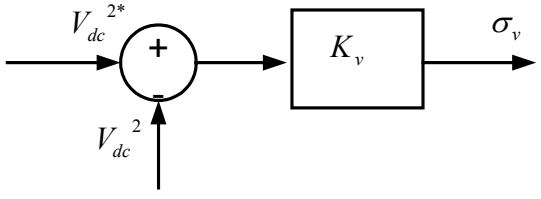


Figure 7.20: Structure of the Voltage controller

In this case ω_0 value depends on the value of ω_0 which is obtained from the current controller. The value ω_0 of the voltage controller has to be at least 10 times lesser than that of the current controller so as to make the response time of the voltage controller slower than that of the current controller.

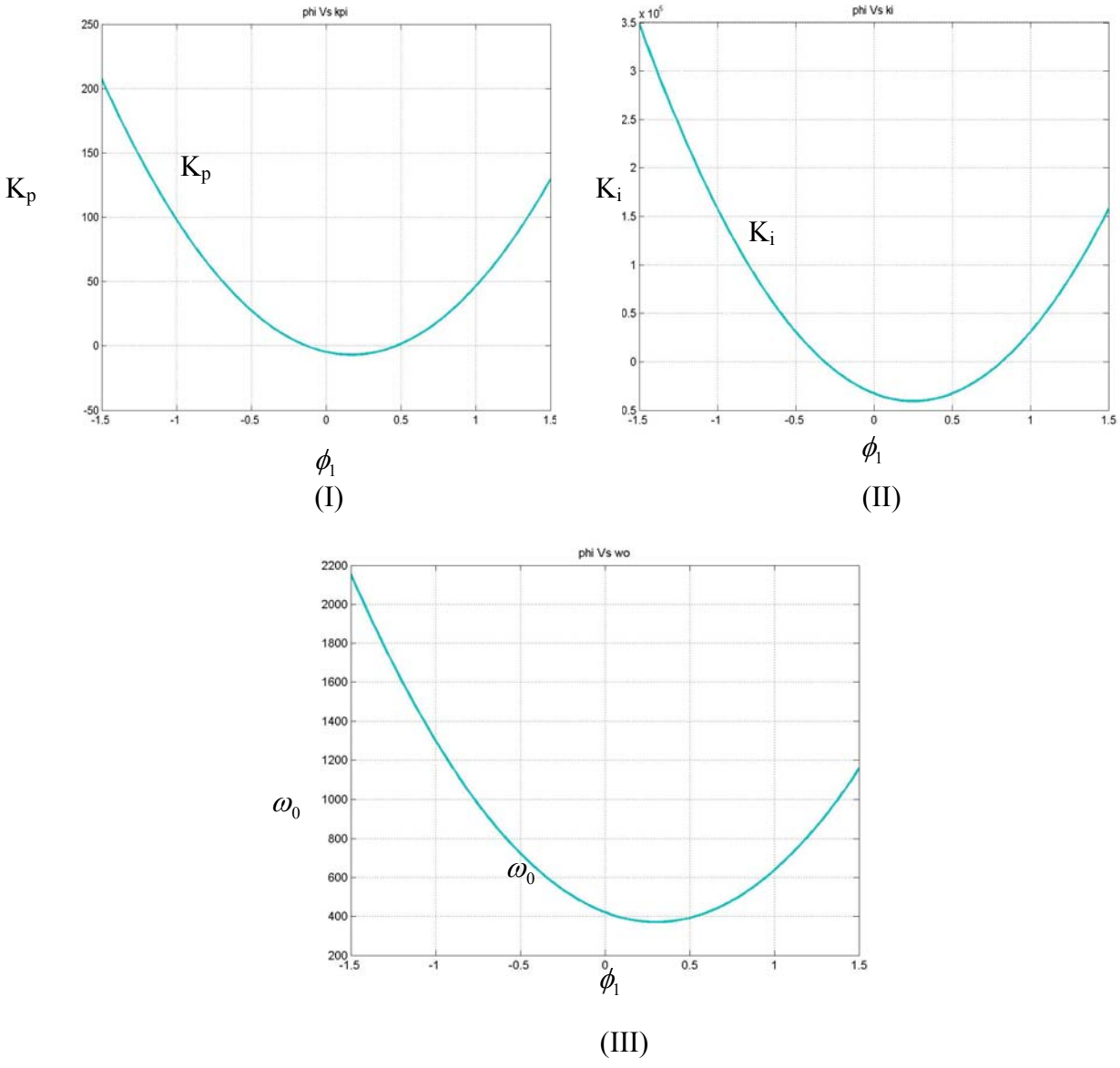


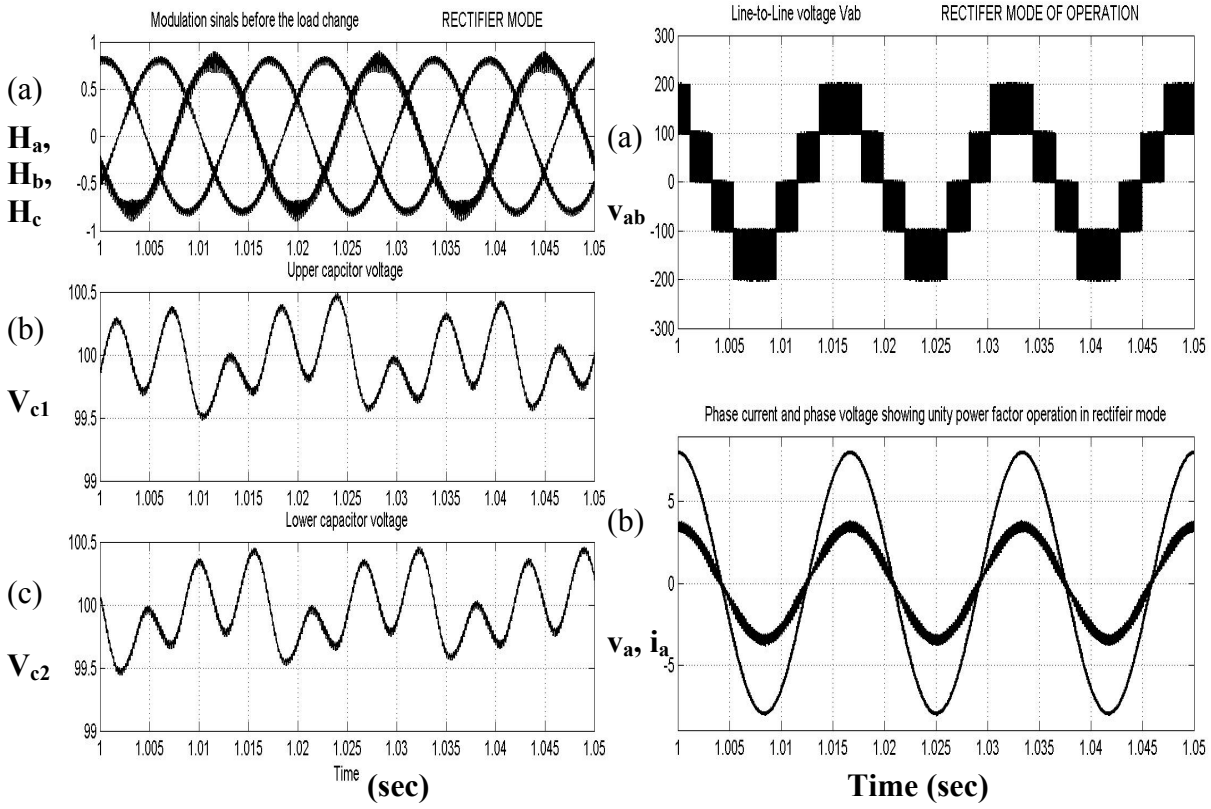
Figure 7.21: Variation of the control parameters of the current controller with the variation of the delay angle ϕ_l .(I) K_p ,(II) K_i ,(III) ω_0.

Figure 7.21 shows the variation of the control parameters of the current and the voltage controller with the variation of the delay angle. The delay angle is varied from – pi/2 to +pi/2 and the expression k_p, k_i, ω_0 obtained by solving the expression (7.77-7.79) are evaluated and plotted against the delay angle. After getting ω_0 from the current controller the voltage control parameters are obtained using expressions (7.81).

7.9 Simulation Results

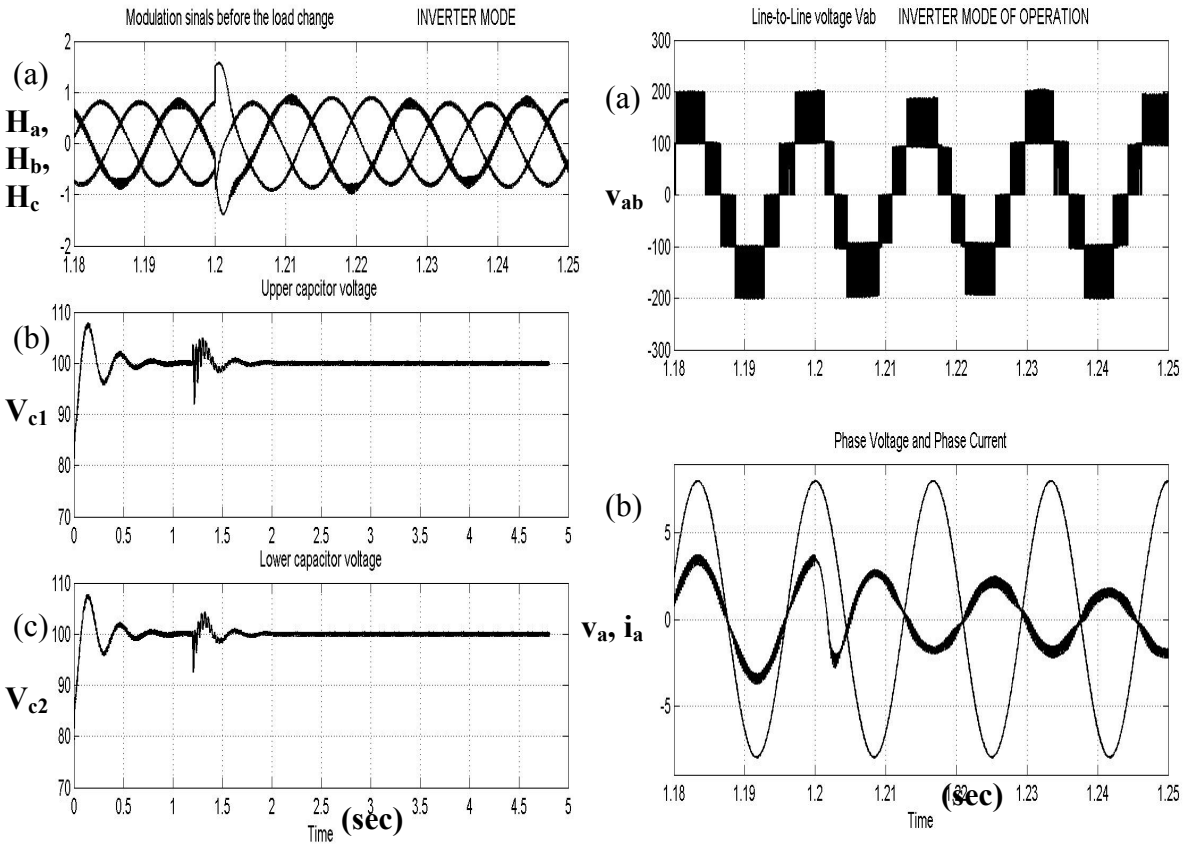
Figures 7.22 to 7.24 show the simulation results for control scheme B. As seen from the plot that even the control scheme B works effectively. Even scheme B is simulated for both the rectifier and inverter modes of operation. The reference capacitor voltage in the present case is taken as 200 V and hence the steady state values of the capacitors should be 100 V each. Figure 7.22 show the steady state plots after the capacitor voltages have settled in the rectifier mode of operation i.e., the power is being fed to the load from the source. Figure 7.22 (I) (a) illustrates the modulation signals during the rectifier mode of operation. Figure 7.22 (I) (b) and (c) shows the capacitor voltage and it can be seen that the capacitor voltages have settled to the reference values of 100 V each with a ripple of 0.7 V. Figure 7.22 II (a) shows the line-line voltage and (b) shows the unity power factor condition. After the capacitors have settled and when the system in steady state, the effectiveness of the controller is checked by operating the rectifier in the regenerative mode i.e., the power is now fed back to the source from the load (for example, incase of a dc motor when the motor runs in the reverse direction). The change is made at time t = 1.2 sec. Figure 7.23 shows the dynamics of the system during the transition. Figure (7.23)

I (a) shows the modulation signals, (b) the capacitor voltages and as seen the capacitor voltages are settled to the reference voltages. Figure (7.23) II (a) the line-to-line voltage and again the unity power factor condition is being maintained even in the regenerative mode. Hence the results show the validity and the effectiveness of the control scheme.



I II

Figure 7.22: Simulation results of control scheme B: Rectifier mode of operation with a load resistance of 75**Ω**. (I) (a) Modulation signals (b) upper capacitor voltage V_{c1} (c) bottom capacitor voltage V_{c2} (II) (a) Line-line source voltage v_{ab}, (b) Input phase voltage (v_a) and source phase current (i_a).



I II

Figure 7.23: Simulation results of control scheme B: Inverter mode of regenerative operation, load change at time t = 1.2sec (I) (a) Modulation signals (H_a, H_b, H_c) (b) upper capacitor voltage V_{c1} (c) bottom capacitor voltage V_{c2} (II) (a) Line-line voltage v_{ab}, (b) phase voltage (v_a) and phase current (i_a).

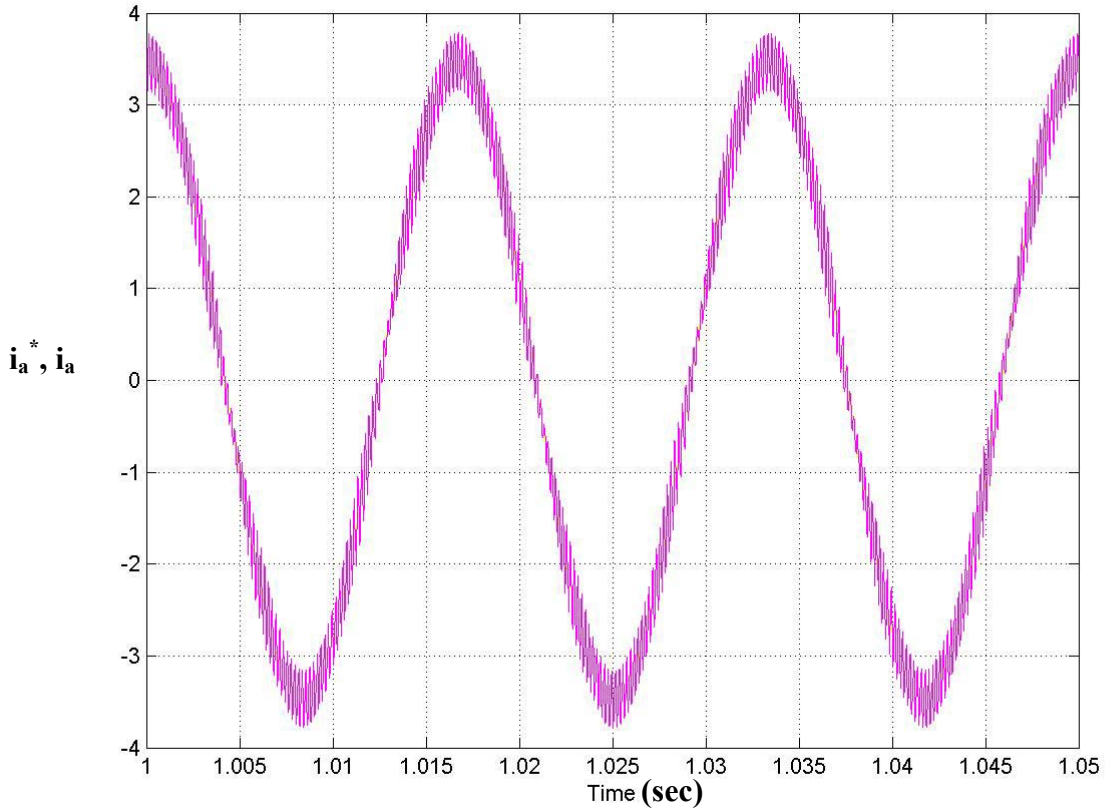


Figure 7.24: Tracking of the phase currents. Reference phase current and the actual phase current.