CHAPTER 3

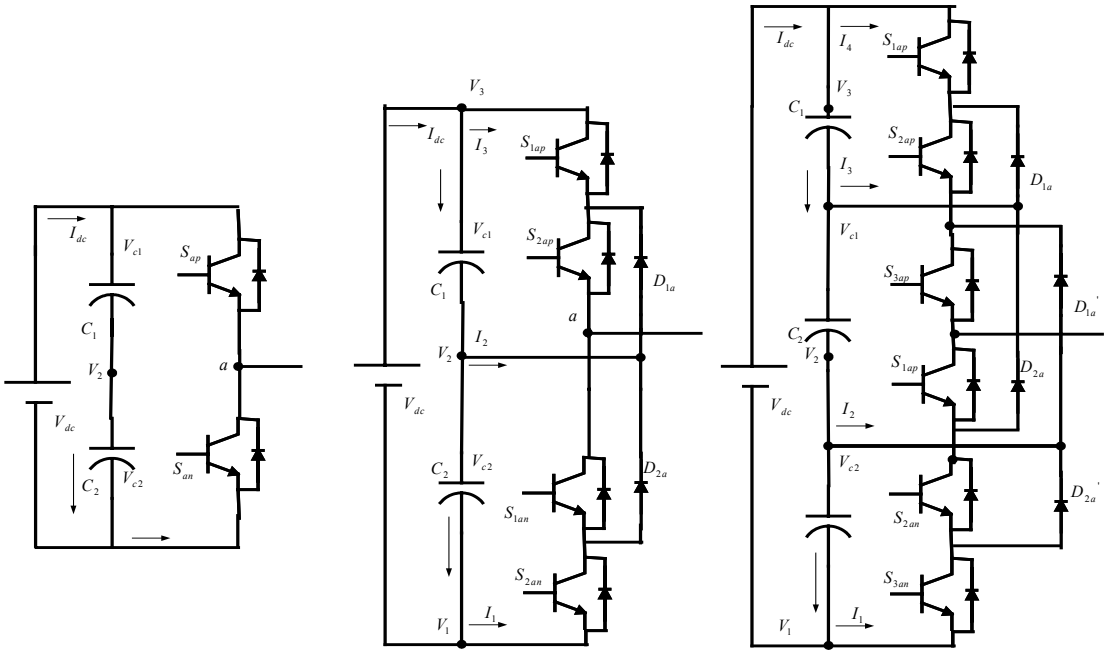
OPERATION AND TOPOLOGIES OF MULTILEVEL CONVERTERS

3.1 Diode-Clamped Multilevel Inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. Figure 3.1 shows the circuit for a diode clamped inverter for a three-level and a four-level inverter. The key difference between the two-level inverter and the three-level inverter are the diodes D_{1a} and D_{2a}. These two devices clamp the switch voltage to half the level of the dc-bus voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is $V_{dc} / n-1$. Although each active switching device is only required to block $V_{dc} / n-1$, the clamping devices have different ratings. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels [4] where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced [4]. However, with an even number of voltage

levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied [5]. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been limited to the three level. Because of industrial developments over the past several years, the three level inverter is now used extensively in industry applications. Although most applications are medium-voltage, a three-level inverter for 480V is on the market.

In general for a N level diode clamped inverter, for each leg 2 (N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge.



(I) (II) (III)

Figure 3.1: Topology of the diode-clamped inverter (I) two-level inverter, (II) three-level inverter, (III) four-level inverter.

Though the structure is more complicated than the two-level inverter, the operation is straightforward and well known [5]. In summary, each phase node (*a*, *b*, or *c*) can be connected to any node in the capacitor bank (V_3, V_2, V_1). Connection of the a-phase to positive node, V_3 occurs when S_{1ap} and S_{2ap} are turned on and to the neutral point voltage, when S_{2ap} and S_{1an} are turned on and the negative node V_1 is connected when S_{1an} and S_{2an} are turned on. There are some complementary switches and in a practical implementation, some dead time is inserted between the gating signals and their complements meaning that both switches in a complementary pair may be switched off for a small amount of time during a transition. However, for the discussion herein, the dead time will be ignored. From Figure 3.1 (II), it can be seen that, with this switching state, the *a*-phase current I_a will flow into the junction through diode D_{1a} if the current is negative or out of the junction through diode D_{2a} if the current is positive. The dc currents I_3, I_2, and I_1 are the node currents of the inverter.

Extending the diode-clamped concept to four levels results in the topology shown in Figure 3.1 (III). A pair of diodes is added in each phase for each of the two junctions. The operation is similar to the three-level. For practical implementation, the switching state needs to be converted into transistor signals. Once the transistor signals are established, general expressions for the *a*-phase line-to-ground voltage and the *a*-phase component of the dc currents can be written as

$$V_{ao} = H_{aN}V_{N0} + H_{aN-1}V_{N-10} + \ldots + H_{a1}V_{10} \tag{3.1}$$

$$V_{bo} = H_{bN}V_{N0} + H_{bN-1}V_{N-10} + \ldots + H_{b1}V_{10} \tag{3.2}$$

$$V_{co} = H_{cN}V_{N0} + H_{cN-1}V_{N-10} + \ldots + H_{c1}V_{10}\,. \tag{3.3}$$

The node currents for the N level inverter are given by

$$I_N = H_{aN} I_a + H_{bN} I_b + H_{cN} I_c$$

$$I_{N-1} = H_{aN-1} I_a + H_{bN-1} I_b + H_{cN-1} I_c$$

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$$I_1 = H_{a1} I_a + H_{b1} I_b + H_{c1} I_c .$$

The above relationships may be programmed into a simulation software to form a block that simulates one phase of a diode-clamped inverter. A number of blocks can be connected together for a multiphase system. For more simulation details, the transistor and diode KVL and KCL equations may be implemented. This allows inclusion of the device voltage drops (as well as conduction losses) and also the individual device voltages and currents. To express this relationship, consider the general N-level diode-clamped structure. Therein, only the upper half of the inverter is considered since the lower half contains complementary transistors and may be analyzed in a similar way. Through the clamping action of the diodes, the blocking voltage of each transistor is the corresponding capacitor voltage in the series bank.

The inner diodes of the multilevel inverter must block a higher voltage. For example, in the four-level topology the inner diodes must block two-thirds of the dc voltage while the outer diodes block one-third. This is a well-known disadvantage of the diode-clamped topology. For this reason, some authors represent the higher voltage diodes with lower voltage diodes in series [6] or alter the structure of the topology so that each diode blocks the same voltage [7].

Finally, the capacitor junction currents may be expressed as the difference of two clamping diode currents. In case of a three-level inverter, the expression reduces to

$$C_1 pV_{c1} = -I_{dc} + H_{a3} I_a + H_{b3} I_b + H_{c3} I_c \tag{3.5}$$

$$C_2 pV_{c2} = -\left(I_{dc} + H_{a1} I_a + H_{b1} I_b + H_{c1} I_c\right). \tag{3.6}$$

3.2 Flying Capacitor Structure

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Meynard and Foch. This is one of the alternative topology for the diode clamped inverter. The flying capacitor involves series connection of capacitor clamped switching cells [8]. Figure 3.2 shows the three-level and the four level capacitor clamped inverter. This topology has several unique and attractive features when compared to the diode-clamped inverter. One feature is that added clamping diodes are not needed. Furthermore, the flying capacitor inverter has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed. Figure 3.2 shows the three-level flying capacitor inverter. The general concept of operation is that each flying capacitor is charged to one-half of the dc voltage and can be connected in series with the phase to add or to subtract this voltage. The major advantage is that the required number of voltage levels can be achieved without the use of the transformer. This assists in reducing the cost of the converter and again reduces power loss. Unlike the diode clamped structure where the series string of capacitors share the

same voltage, in the capacitor-clamped voltage source converter the capacitors within a phase leg are charged to different voltage levels. To synthesize the phase voltage waveforms the various switches within the phase leg are switched on to combine the various capacitor voltage levels with the constraint that no capacitor is short-circuited and current continuity with the DC link is maintained for each capacitor.

Similar to the diode clamped inverter, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, a N level converter will require a total of (N-1) * (N-2) / 2 clamping capacitors per phase in addition to the N-1 main dc bus capacitors.

The topology also has several disadvantages that have limited its use. First one being the converter initialization i.e., before the converter can be modulated by any modulation scheme the capacitors must be set up with the required voltage level as the initial charge. This complicates the modulation process and becomes a hindrance to the operation of the converter. The capacitor voltages must also be regulated under normal operation in a similar way to the capacitors of a diode clamped converter. Another major drawback of the topology is the rating of the capacitors, since the capacitors have large fractions of the dc bus voltage across them.

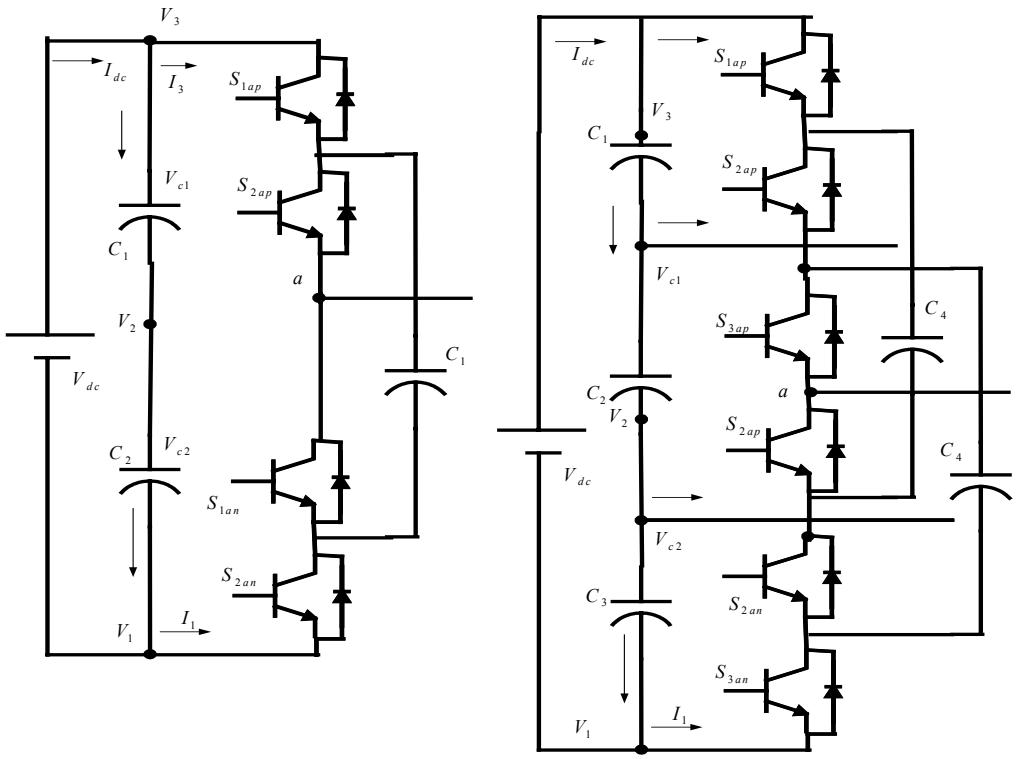

Figure 3.2: Schematic of Capacitor Clamped inverter (I) three-level inverter (II) four-level inverter.

In the operation of the converter, each phase node (*a*, *b*, or *c*) can be connected to any node in the capacitor bank (V_3, V_2, V_1*)*. Connection of the a-phase to positive node V_3 occurs when S_{1ap} and S_{2ap} are turned on and to the neutral point voltage when S_{2ap} and S_{1an} are turned and the negative node V_1 is connected when S_{1an} and S_{2an} are turned on. The clamped capacitor C_1 is charged when S_{1ap} and S_{1an} are turned on and is discharged when S_{2ap} and S_{2an} are turned on. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V_3. Considering the direction of the *a*-phase flying capacitor current I_a for

the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states so that both capacitors can be regulated to their ideal voltages.

3.3 Series H-Bridge Multilevel Inverter

One more alternative for a multilevel inverter is the Series H-bridge inverter. The series H-bridge inverter appeared in 1975 [7], but several recent patents have been obtained for this topology as well. A series of single-phase full bridges makes up a phase for the inverter. Each full bridge can switch between $+V_{dc}$, 0, $-V_{dc}$. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. An apparent disadvantage of this topology is the large number of isolated voltages required to supply each cell. However, phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

There are several advantages for this topology that have made the application of the converter interesting. The main advantage is the regulation of the DC buses described, while the other is concerning the modularity of control that can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately. Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.

A two-cell series H-bridge inverter is as shown in Figure 3.3. The inverter consists of familiar H-bridge (sometimes referred to as full-bridge) cells in a cascade connection. Since each cell can provide three voltage levels (zero, positive dc voltage, and negative dc voltage), the cells are themselves multilevel inverters. Since the H-bridge cells can supply both positive and negative voltages contributing to the line-to-ground voltage, a switching state is defined for H-bridge cells that have negative values.

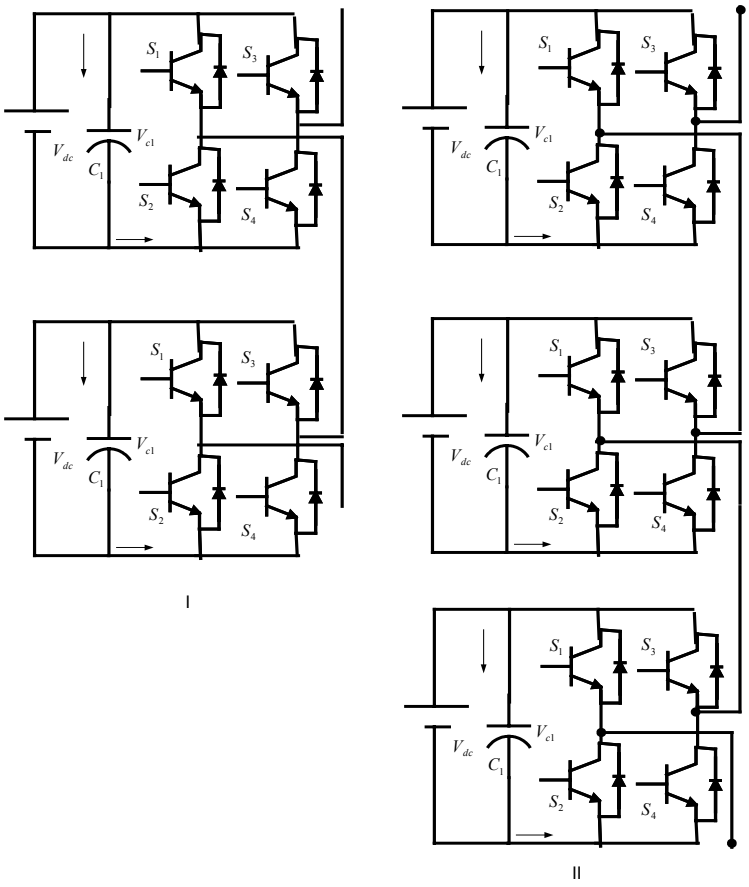

Figure 3.3: Schematic of series H-bridge inverter.

3.4 Parallel Phase Topology

Since nearly all multilevel inverters involve effective series connection of transistor devices, parallel connection of inverter poles through inter-phase reactors is sometimes overlooked or not recognized as a multilevel solution. However, researchers noted the features and redundancies of multilevel some time ago [9]. One advantage of parallel connection is that the devices share current and this topology is good for high current loads. It is also reasonable to perform parallel combinations of diode-clamped

poles so that the transistor voltage and current ratings are reduced [10]. This structure has the advantage of providing a high number of voltage levels while reducing the voltage and current stress on the individual transistors. Figure 3.4 shows a three-phase three-level inverter made from parallel two-level poles. The inter-phase reactor is similar to a typical transformer with the exception that an air-gap exists in the core to ensure linearity and the windings are such that the resistance and leakage inductances are small. With these assumptions, the reactor will have equal voltages on each of the two-level poles i.e., the line-to-ground voltage is the average of that of each of the two-level poles.

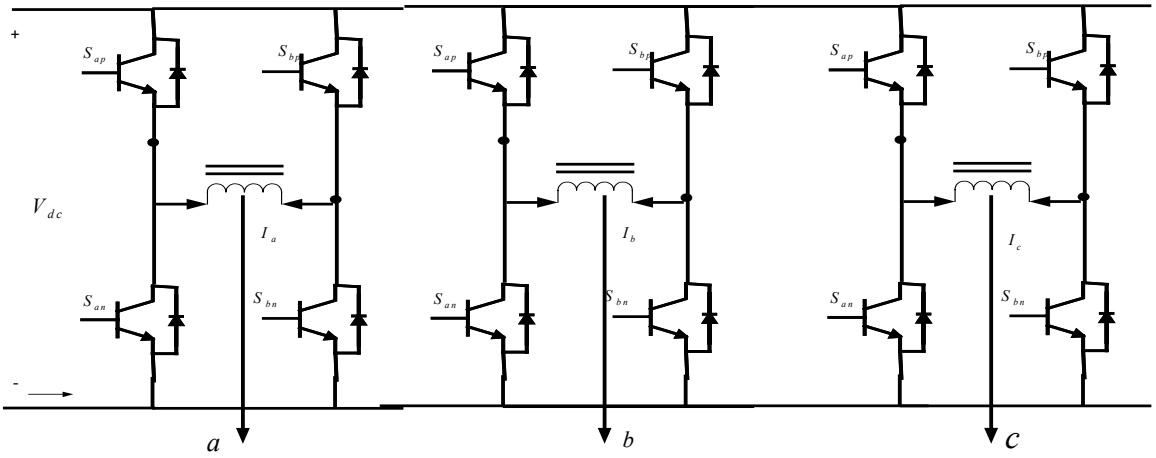

Figure 3.4: Schematic of the parallel phase topology.

3.5 Mixed-Level Hybrid Multilevel Cells

The hybrid converter topology was proposed by Manjrekar. For high-voltage high-power applications, it is possible to adopt multilevel diode-clamped or capacitor-clamped inverters to replace the full-bridge cell in a cascade inverter. The reason for

doing so is to reduce the amount of separate dc sources. The cascade inverter requires more number of dc sources than the mixed hybrid inverter to achieve the same number of levels.

Figure 3.5 shows the structure of a seven level hybrid inverter, in which it can be seen that each phase leg is constructed from a high-voltage (HV) stage and a low-voltage (LV) stage. The simplest configuration comprises two series connected dingle-phase inverters per phase, with their dc voltages in the ration of 2:1. In terms of the operation, the hybrid converter uses the HV stage to achieve the bulk power transfer and uses the LV stage as a means to improve the spectral performance of the overall converter. The levels obtained using the configuration in Figure 3.5 are $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$. Also note that the HV stage is shown to be constructed using devices that have high-voltage blocking characteristics but not necessarily fast switching characteristics like integrated gate controlled thyristors (IGCT) while the LV stage is constructed using devices that have fast switching characteristics but not necessarily high-voltage blocking characteristics like insulated gate bipolar transistor (IGBT).

The hybrid system again uses the transformer to produce the isolated dc supplies for each full-bridge inverter, and the control of the converter are more complex than the standard cascaded structure. However the control is still modular in that the LV stage and HV stage have their own reference waveforms, but the LV stage reference must be created from the HV reference. One of the problems with the converter is that during the middle ranges of the modulation index the HV stage will be supplying more power to the load when compared to the LV stage. Under these operating conditions the LV stage will be required to operate in a rectification mode, which means that the DC link must be

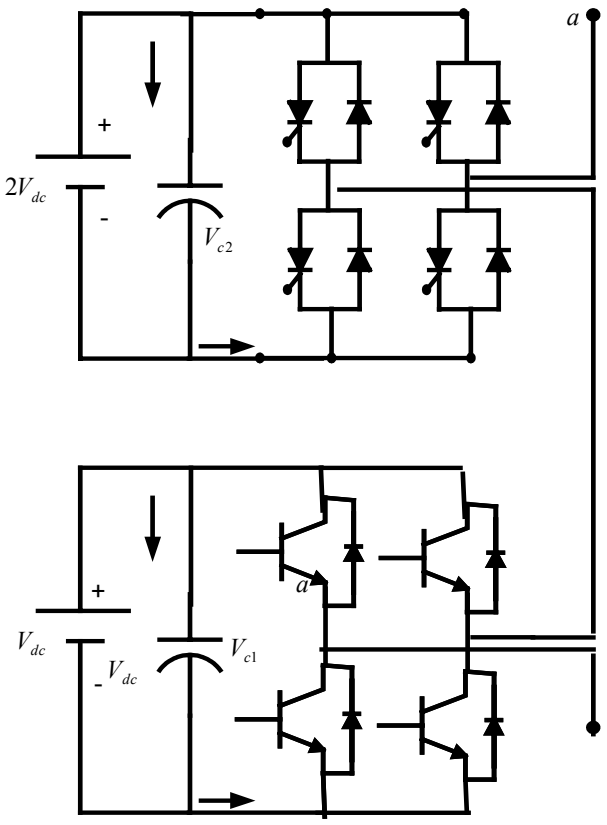

Figure 3.5: Schematic of a seven-level hybrid voltage source inverter.

capable of bidirectional power flow. However, the reduced switch count and more effective use of the power electronics devices that comprises the hybrid system make it a particularly attractive system at medium to high power levels.

3.6 Asymmetric Hybrid Multilevel Cells

In the previous sections, the voltage levels of the cascade inverter cells equal each other. However, it is possible to have different voltage levels among the cells, and the circuit can be called as asymmetric hybrid multilevel inverter. Figure 3.6 shows an

example of having two separate dc-bus levels, one with V_{dc}, and the other with V_{dc} / 2. Depending on the availability of dc sources, the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage, and thus reduces the harmonic contents with less number of cascaded cells required. The operation is similar to that of hybrid level converter except that this topology uses IGBT devices in both the bridges. The levels obtained using the configuration in Figure 3.6 are $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$.

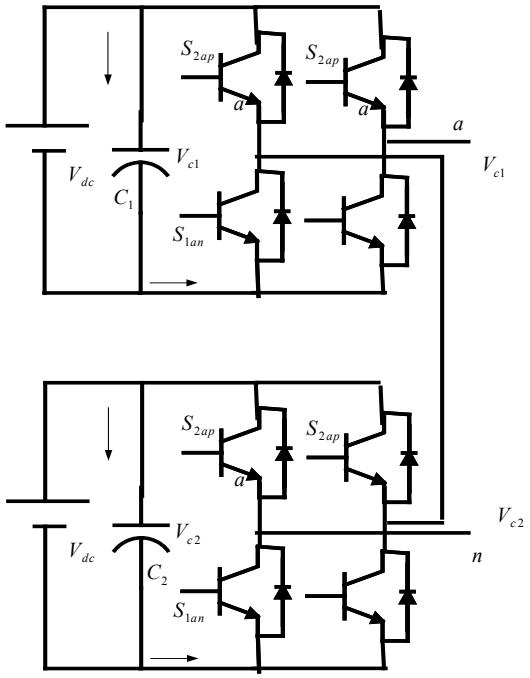

Figure 3.6: Schematic of asymmetric hybrid cascaded inverter cell arrangement with different voltage levels.

3.7 Soft Switching Multilevel Inverters

Soft switching topologies are popular in case of the two-level converters; applying the same principles, to reduce the switching losses that are produced because of the switching of the devices, soft switching techniques are used to switch the devices to reduce the switching losses and hence increase the efficiency of the multilevel inverter. In case of the cascaded inverter, the implementation of the soft switching is similar to that of the conventional two-level inverter. For diode or capacitor clamped inverters, however, the choices of soft-switching circuit can be found with different circuit combinations. Although zero-current switching is possible, mostly zero-voltage switching is used in most of the converter.

The auxiliary switch S_{x2}, S_{x3}, D_{x2}, and D_{x3} are used to assist the inner main switches S_{2ap} and S_{1an} to achieve the soft switching. With L_{r23} as the coupled inductor, the bridge type circuit formed by S_{x2}, S_{x3}, S_{2ap}, and S_{1an} forms a two-level coupled-inductor ZVT. For the outer main switches, the soft switching relies on S_{1ap} and S_{2an}, S_{x1}, S_{x4}, D_{x1}, D_{x4} coupled with inductor L_{r14}, and split-capacitor pair C_2 to form an auxiliary resonant commutated pole (ARCP) type soft switching.

When the load current is positive, diodes which are in the bottom devices are conducting the load current I_L; during this interval, the main switches S_{1an} and S_{2an} are turned off and their snubber capacitor voltages are charged to $V_{dc} / 2$. After the auxiliary switch S_{x1} turns on, the inductor current I_{Lr14} increases linearly until it reaches the load current. As this time, the current in D_4 starts to decrease slowly to zero. When the

inductor current I_{Lr14} exceeds the load current, the diode current passing in S_{2an} device turns off naturally. During this interval, the main switch S_{2an} is turned on. After S_{2an} turns off, the resonant inductor and capacitor starts to resonate to discharge the capacitor voltage of S_{1ap}. After the resonant period, the stored inductor current slowly starts to decrease through the resonant tank. During this interval, negative voltage is applied to the resonant inductor. When the resonant current falls below the load current, the commutation will naturally occur from the diode of S_{2an} to S_{1ap} under zero voltage condition. After some time, the diode D_{x1} will be turned off at zero-current condition and the device S_{1ap} quickly reaches the load current. Conducting the D_{x1} stabilizes the circulating path of the magnetizing current through the coupled inductor and after the elimination of this magnetizing current, the auxiliary switch S_{x1} is turned off at zero current condition.

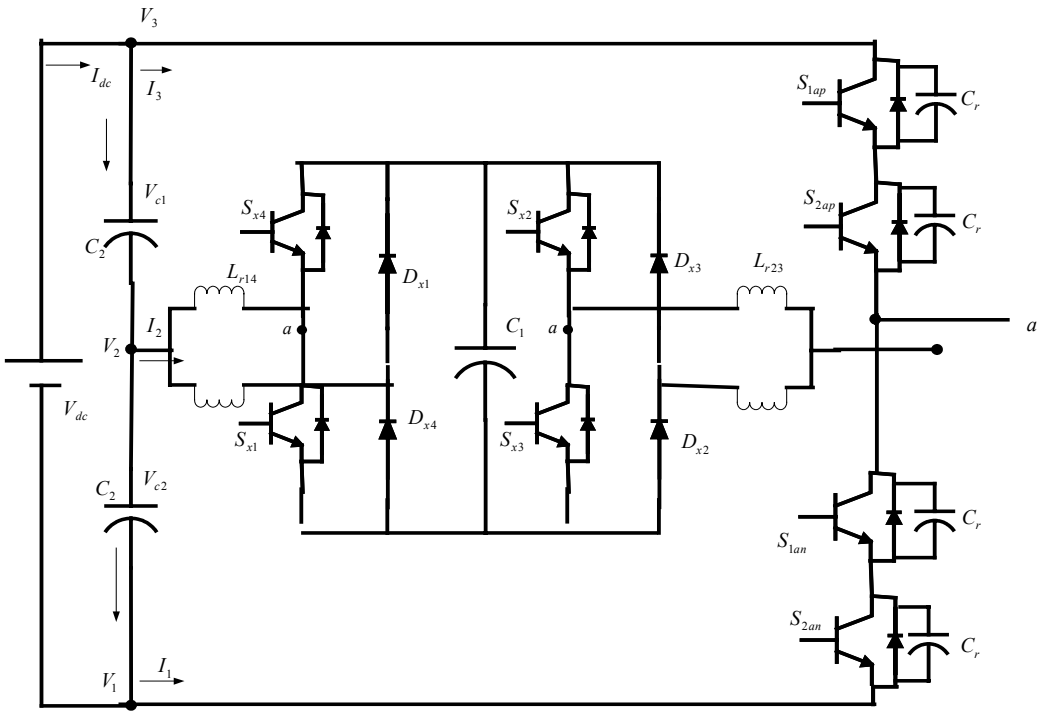

Figure 3.7: Schematic of zero-voltage-switching capacitor clamped inverter circuit.

3.8 Carrier-Based PWM Scheme

This section of the chapter extends the principles of carrier-based PWM that are used for multilevel inverter. One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. There are three alternative PWM strategies with differing phase relationships:

- Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbor carrier by 180^0.
- Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.
- Phase disposition (PD)- All carrier waveforms are in phase.

3.8.1 Alternate Phase Disposition (APOD)

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180^0. Since APOD and POD schemes in case of three-level inverter are the same, a five level inverter is considered to discuss about the APOD scheme.

The rules for APOD method, when the number of level N = 5, are

- The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180^0.

- The converter switches to + V_{dc} / 2 when the reference is greater than all the carrier waveforms.
- The converter switches to V_{dc} / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.
- The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.
- The converter switches to - V_{dc} / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.
- The converter switches to -V_{dc} / 2 when the reference is lesser than all the carrier waveforms.

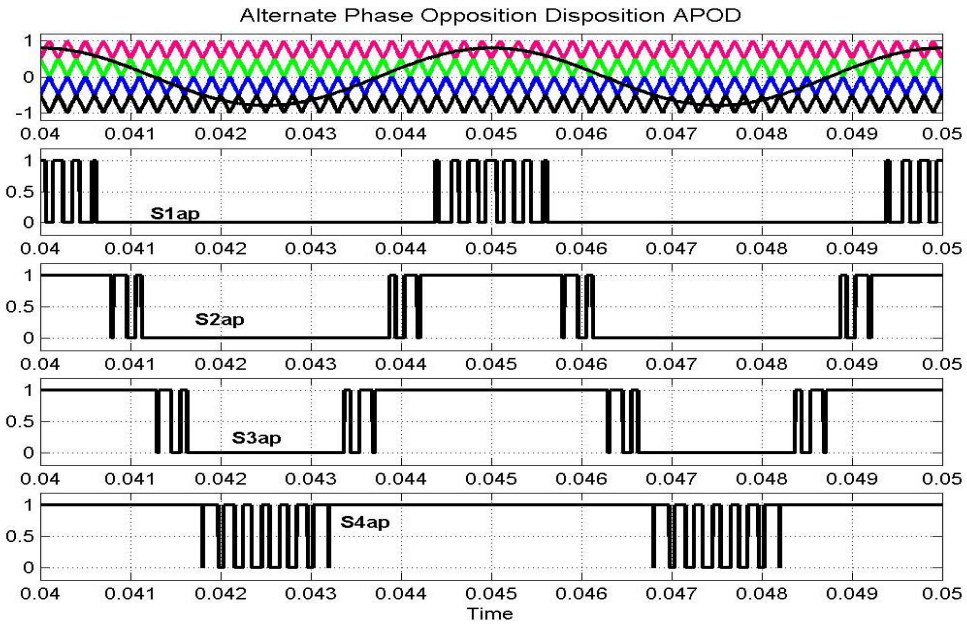

Figure 3.8: Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter: (a) Four triangles and the modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{3ap} (e) S_{4ap}.

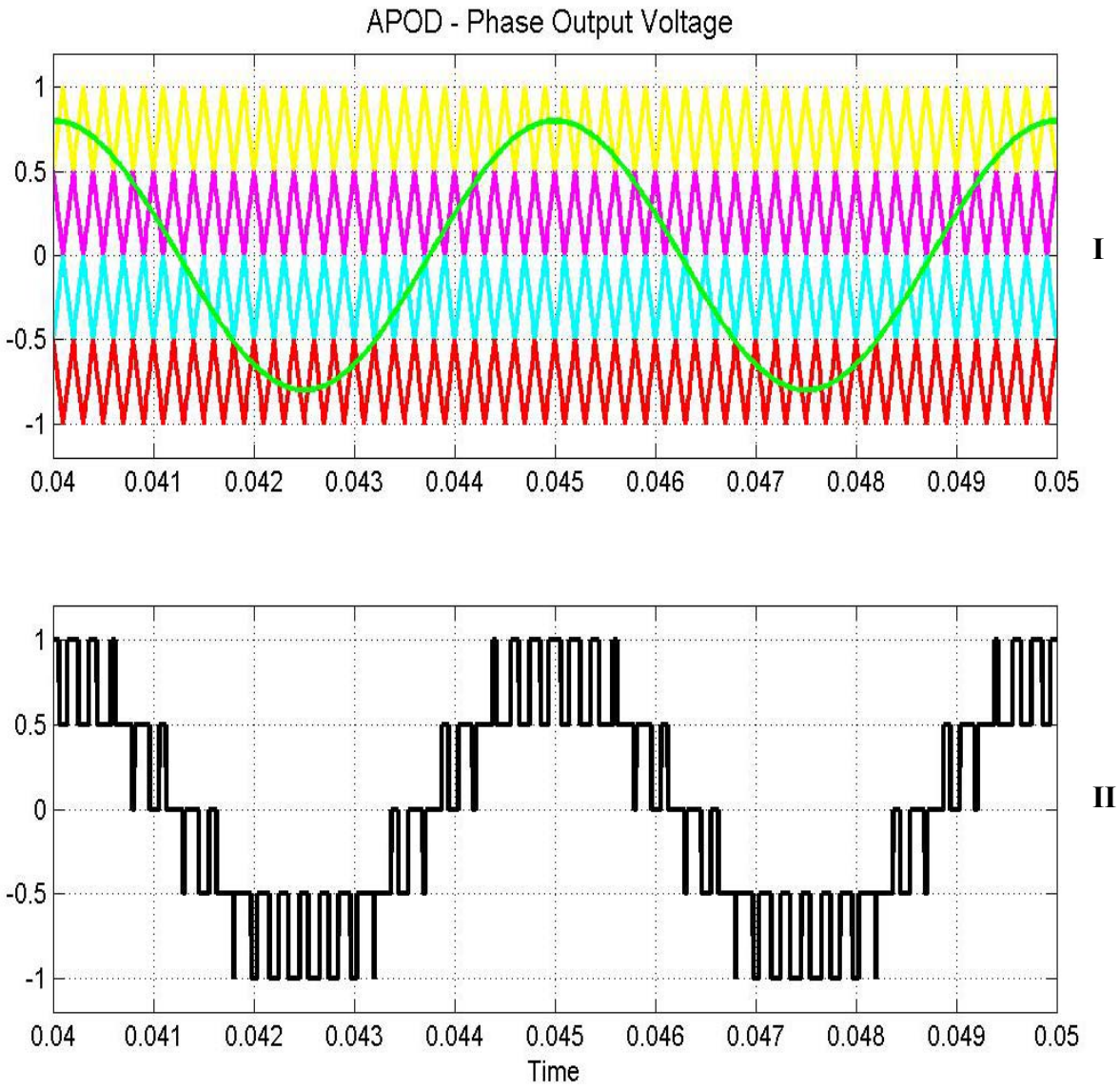

Figure 3.9: Simulation of carrier-based PWM scheme using APOD for a five-level inverter. I. Modulation signal and carrier waveforms (II) Phase "a" output voltage.

Figure 3.8 demonstrates the APOD scheme for a five-level inverter. The figure displays the switching pattern generated by the comparison of the modulation signals with the four carrier waveforms. Figure 3.9 shows the output voltage waveform of phase "a" and it is clear the waveform has five steps.

3.8.2 Phase Opposition Disposition (POD)

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.

The rules for the phase opposition disposition method, when the number of level N = 3 are

- The N –1 = 2 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180^0 out of phase with those below zero.
- The converter is switched to + V_{dc} / 2 when the reference is greater than both carrier waveforms.
- The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
- The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

As seen from Figure 3.10, the figure illustrates the switching functions produced by POD carrier-based PWM scheme. In the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the lower triangle from 0 to –1 and these two triangle waveforms are in out of phase. When the modulation signal is greater than both the carrier waveforms, S_{1ap} and S_{2ap} are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S_{2ap} and S_{1an} are turned on and the converter switches to neutral point.

When the reference is lower than both carrier waveforms, S_{1an} and S_{2an} are turned on and the converter switches to negative node voltage.

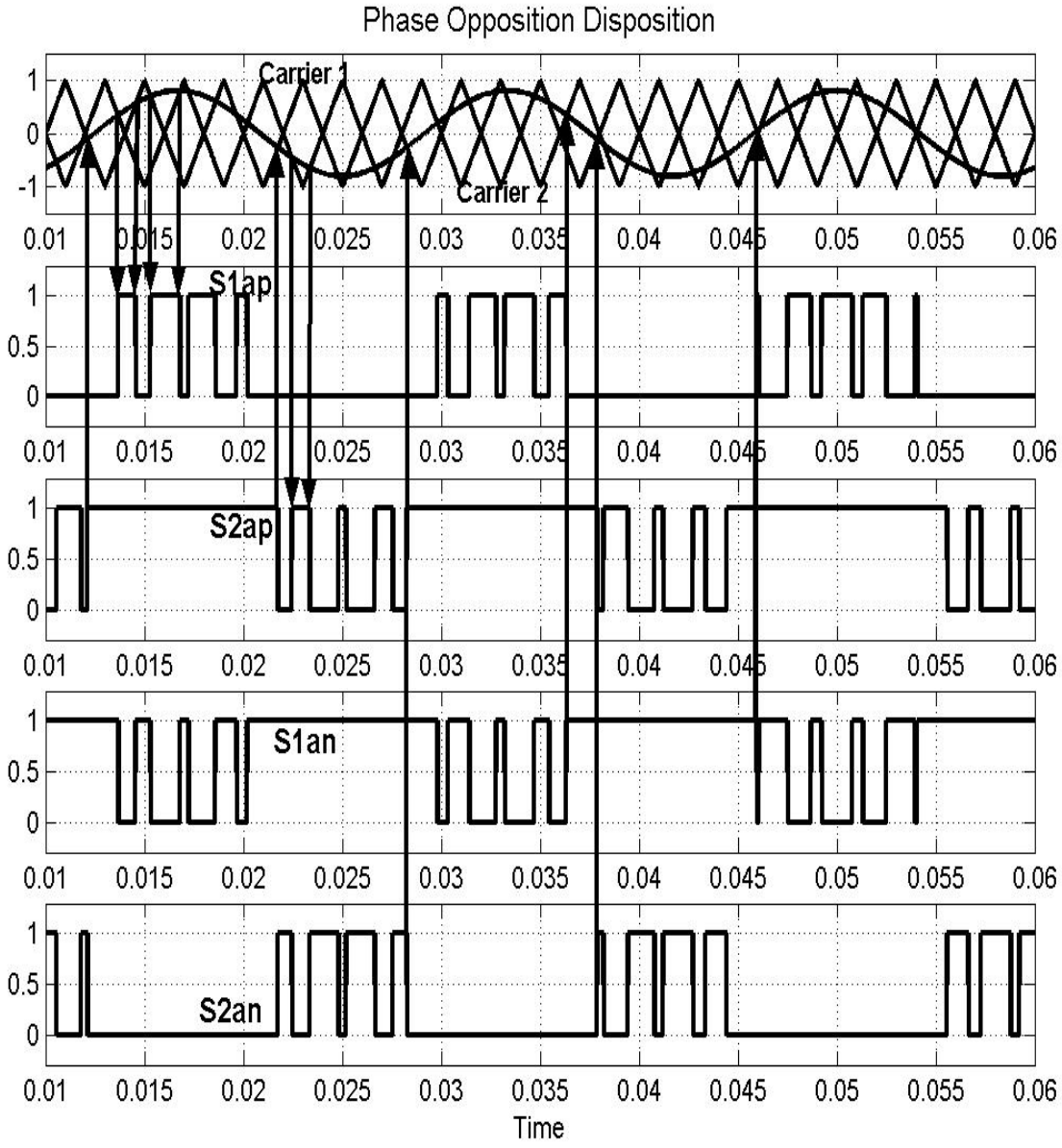

Figure 3.10: Switching pattern produced using the POD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{1an} (e) S_{2an}.

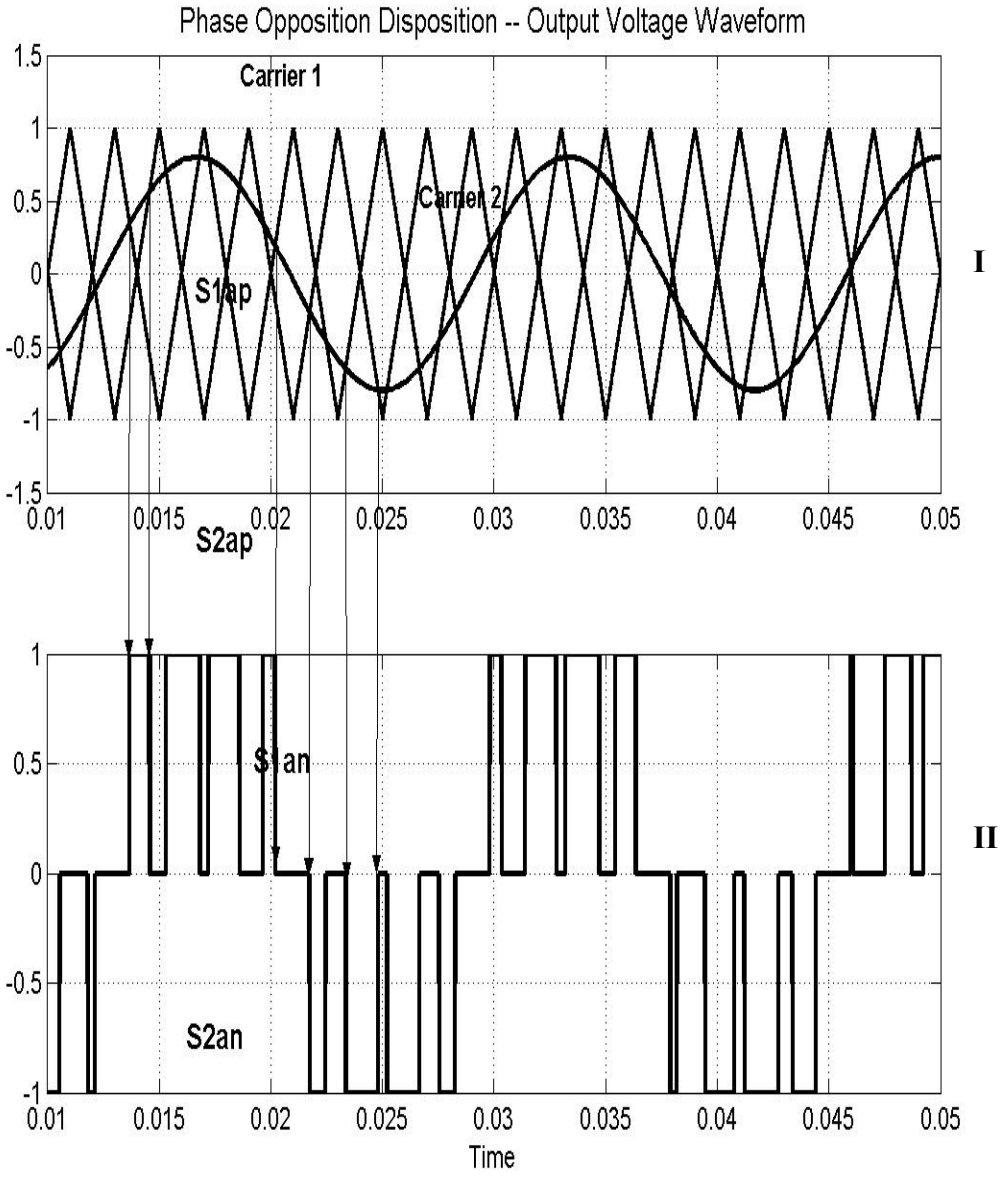

Figure 3.11: Simulation of carrier-based PWM scheme using POD. I. Modulation signal and out of phase carrier waveforms (II) Phase "a" output voltage.

Figure 3.11 shows the implementation of the phase disposition (PD) scheme. Figure 3.11 (I) shows the two carriers waveforms are displaced out of phase and compared with the sinusoidal modulation signal. Figure 3.11 (II) shows the phase "a" output voltage waveform.

3.8.3 Phase Disposition (PD)

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Figure 3.8 demonstrates the sine-triangle method for a three-level inverter. Therein, the *a*-phase modulation signal is compared with two (*n*-1 in general) triangle waveforms.

The rules for the phase disposition method, when the number of level N = 3, are

- The N –1 = 2 carrier waveforms are arranged so that every carrier is in phase.
- The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.
- The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.
- The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

In the carrier-based implementation at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the definition of the switching pulses is generated.

As seen from Figure 3.8, the figure illustrates the switching pattern produced by the carrier-based PWM scheme. In the PWM scheme there are two triangles, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. In the similar way for an N –level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/(N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/(N-1)), second

carrier waveform from (1-4/(N-1)), and the bottom most triangle varies from (2-2/(N-1)) to –1.The switching function for the devices is given by

$$H_a > Triangle - 1 \;\; \&$$
$$> Triangle - 2; \;\; H_{a3} = 1; otherwise \quad H_{a3} = 0$$

$$H_a < Triangle - 1 \;\; \&$$
$$> Triangle - 2; \;\; H_{a2} = 1; otherwise \quad H_{a2} = 0$$

$$H_a < Triangle - 1 \;\; \&$$
$$< Triangle - 2; \;\; H_{a1} = 1; otherwise \quad H_{a1} = 0.$$

In Figure 3.12, the switching pattern of each device can be seen. It is clear from the figure that during the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S_{1ap} and S_{2ap} are turned on and also during the positive cycle S_{2ap} is completely turned on. When S_{1ap} and S_{2ap} are turned on the converter switches to the + V_{dc} / 2 and when S_{1an} and S_{2ap} are on, the converter switches to zero and hence during the positive cycle S_{2ap} is completely turned on and S_{1ap} and S_{1an} will be turning on and off and hence the converter switches from + V_{dc} / 2 – 0. During the negative half cycle of the modulation signal the converter switches from 0 - - V_{dc} / 2. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage $V_{30} = \frac{V_{dc}}{2}, \; V_{20} = 0, \; V_{10} = -\frac{V_{dc}}{2}$.

$$V_{ao} = H_{a3}V_{30} + H_{a2}V_{20} + H_{a1}V_{10}$$

$$V_{bo} = H_{b3}V_{30} + H_{b2}V_{20} + H_{b1}V_{10}$$

$$V_{co} = H_{c3}V_{30} + H_{c2}V_{20} + H_{c1}V_{10}$$

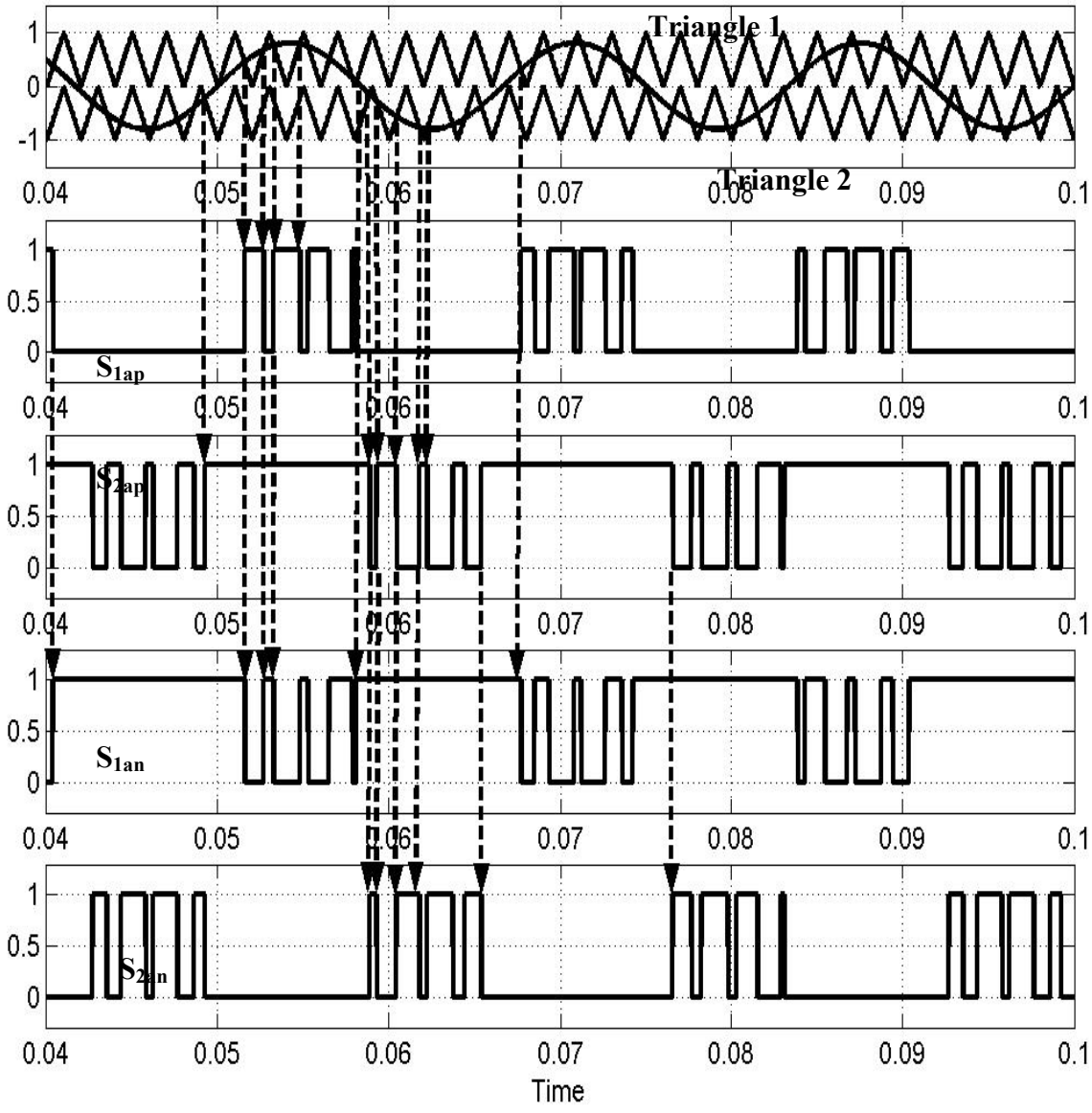

Figure 3.12: Switching pattern produced using the PD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{1an} (e) S_{2an}.

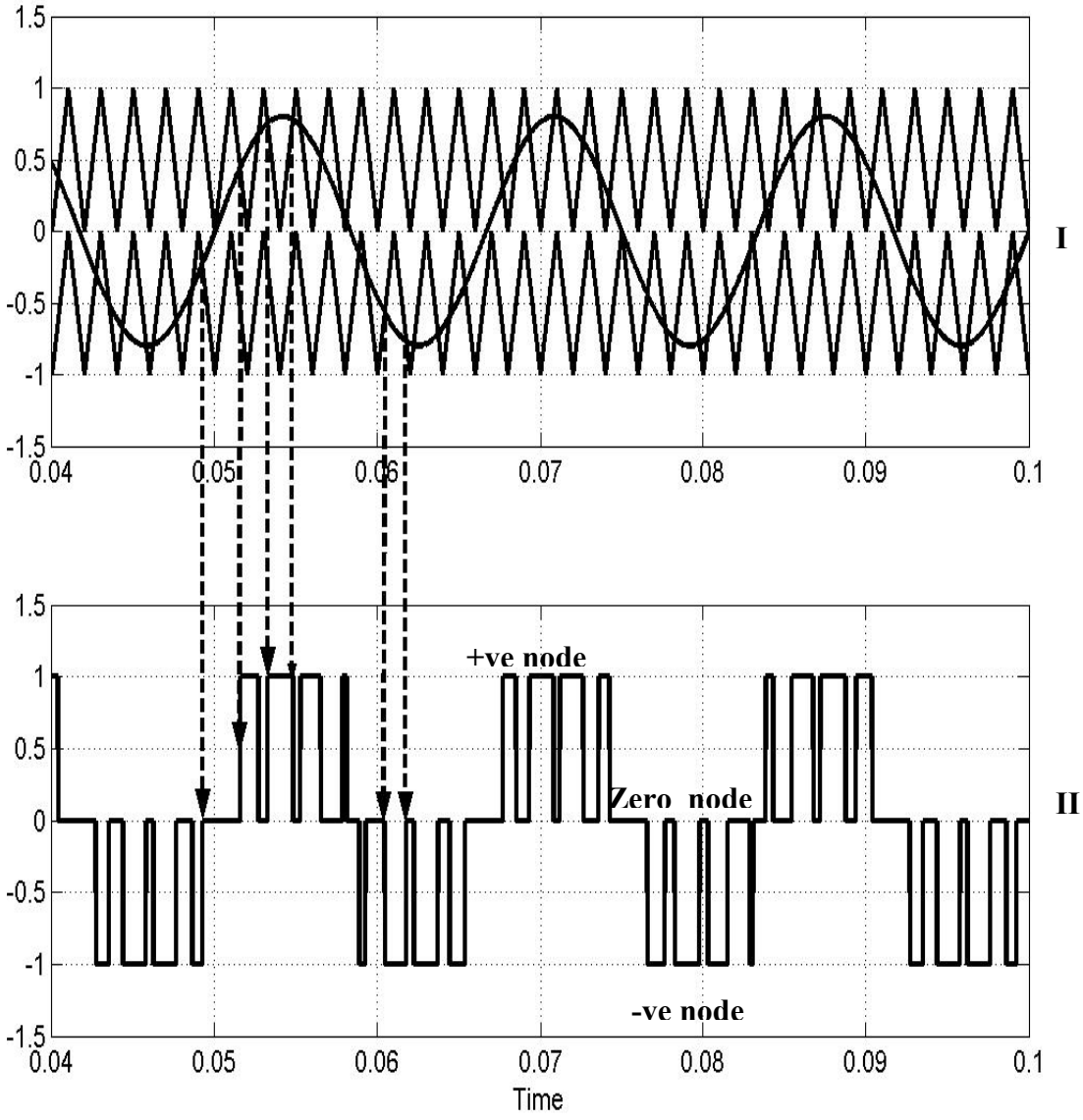

Figure 3.13: Simulation of carrier-based PWM scheme using the phase disposition (PD). I. Modulation signal and in-phase carrier waveforms (II) Phase "a" output voltage.

Figure 3.13 shows the implementation of the phase disposition (PD) scheme. Figure 3.13 (I) shows that two carriers waveforms are displaced in phase and compared with the sinusoidal modulation signal. Figure 3.13 (II) shows the phase "a" output voltage waveform.