AN ABSTRACT OF A THESIS

PWM SCHEMES FOR THREE PHASE CURRENT SOURCE CONVERTERS

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Master of Science in Electrical Engineering

An alternate topology to a Voltage Source Converter (VSC) is a Current Source Converter (CSC); its advantages in terms of ruggedness, inherent short circuit protection and significant reduction in load harmonics make the CSC a unique one. In the literature many offline and online PWM strategies for CSC have been proposed. But in the present work a unified approach for generating pulse width modulation for current source inverters/rectifiers has been presented.

A novel online carrier-based modulation scheme for the inverter is developed using the already developed non-sinusoidal and generalized discontinuous PWM modulation (GDPWM) for voltage source inverter (VSI). A mapping technique is developed in both sine triangle PWM scheme and space vector approach, which maps states of a VSI to states of a CSI, a proper method of distribution of the null states is presented, in order to satisfy the constraints of the CSI.

A novel direct carrier-based discontinuous pulse-width modulation (PWM) scheme based on space vector modulation using the states of the CSI is developed. The expressions for the modulating signals for the discontinuous carrier-based PWM scheme using the nine possible states of the CSI are derived. A new algorithm is stated using the maximum, medium and minimum of the reference signals, which automatically makes the switching pattern suitable for modulation of a CSI. In direct digital implementation scheme, a new technique for proper positioning of the null states in between the active states is presented. The above sorting technique is applied for both linear and over modulation region of operation. The above method of sequencing of the states has the advantages of having less number of switching transitions, which aids in the reduction of the effective switching of the inverter. Confirmatory experimental results are provided to illustrate the effectiveness of both the developed modulation schemes.

A new method of using complex q-d equations of the Current Source Rectifier (CSR), in designing a control structure for output DC voltage regulation under unity power factor operation of CSR is stated. The modeling of the CSR and detailed controller design methodology is set forth. Simulation results are presented to show the effectiveness of the control structure.

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CERTIFICATE OF APPROVAL OF THESIS

PWM SCHEMES FOR THREE PHASE CURRENT SOURCE CONVERTERS

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DEDICATION

This work is dedicated to my parents.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Power electronic converters belong to the family of electrical circuits, which modulate, i.e., to convert electrical energy from one level of voltage/current/frequency to another using semiconductor–based electronic switches. These switches are operated in either completely turned ON or completely turned OFF state, unlike control elements of most other electronic circuits, which operate in a near-linear region. Each family of power converters has own preferred modulation strategies associated with it that aim to optimize the circuit operation for the target criteria most appropriate for that family [B.1]. Parameters such as switching frequency, distortion, losses, harmonic generation, and speed of response are some of the typical issues, which must be considered while developing modulation strategies for a particular family of converter.

Power electronics has gone through intense technological evolution during the last three decades [B.2]. Recently, it has found wide applications in industrial, commercial, residential, and aerospace environments. At present, power electronics seems to have been polarized in two directions: Low–power high frequency electronics, which essentially caters to the need of switching–mode power supplies, and moderate to high power electronics, which essentially covers motor drives, uninterruptible power supplies, lightning and heating control, electrochemical process, DC and AC regulated power

supplies, induction heating, DC and AC electrical machine drives, electrical welding, active power line filtering, static var compensation, etc.

The core of the power electronics apparatus consists of a converter built with a matrix of power semiconductor switching devices that work under the guidance of control electronics. In general, a switching converter [A.1] takes power input and a control input, yielding the conditioned output power. In a DC-DC converter, the DC input voltage is converted to a DC output voltage having a larger or smaller magnitude, possibly with opposite polarity or with isolation of the input and the output ground references. In an AC-DC rectifier an AC input voltage is rectified producing a DC output voltage. The DC output voltage and/or AC input current waveform might be controlled. The inverse process, DC-AC inversion, involves transforming a DC input voltage into an AC output voltage of controllable magnitude and frequency. AC-AC cycloconversion involves converting an AC input voltage to a given AC output voltage of controllable magnitude and frequency.

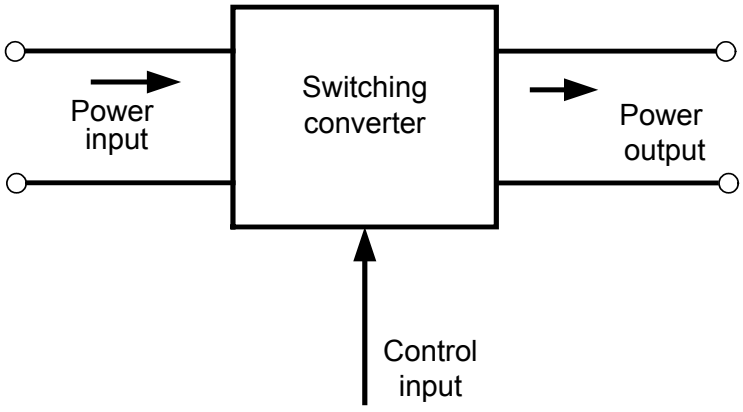


Figure 1.1 Basic power-processing block of switching converters

Converters can be classified as rectifiers (AC-to-DC converter), inverters (DC-to-AC converter), choppers (DC-to-DC converter), AC power controller (at same frequency), and cycloconverter (direct frequency changer). These converters make it possible to deliver high performance, low cost drives for a wide range of commercial, vehicular, military, and residential applications, thereby contributing to the efficient operation of electric power systems, enhancing the efficient use of electricity, and thus contributing to environmental protection. Converters are going to play a very important role in the future irrespective of their field of application.

Research has been going on different modulation strategies to modulate these converters for an efficient use. Many techniques have been proposed in order to have a minimum amount of switching in the converter and also to synthesize output voltages and output currents with very high gains. One of the most widely utilized strategies for controlling the AC output of power converters is the technique known as pulse width modulation (PWM), which varies the duty cycle of the converter switches at a high switching frequency to achieve low frequency output voltage or currents. Modulation theory has been a major research area in power electronics for over three decades and continues to attract considerable interest [A.5]. On the other hand, there has been a number of clear trends in the development of PWM concepts and strategies since 1970's, addressing the main objectives of reduced harmonic distortion and increased output magnitudes for a given switching frequency and to develop modulation strategies to suit different converter topologies [B.3].

In this work PWM-based modulation schemes are proposed for three-phase current source converters (CSC). These modulation schemes are useful in the modulation of current source inverters (CSI) and current source rectifiers (CSR).

1.2 PWM Methodologies

Many PWM methods are proposed for switching the converter switches but the two main types of PWM schemes are:

1. Comparison of a continuous or a discontinuous modulating signal with a high frequency carrier signal to generate PWM. (Sine triangle PWM)
2. Direct digital implementation by calculating the switching times for each device using the space vector approach. (SVPWM)

Both of these schemes have their own advantages; choice of scheme depends on the application and also other requirements, such as good waveform quality, high dynamic performance, low switching loss, and implementation simplicity.

1.3 Research Goals

This thesis will address the following issues in power electronic systems with special attention on development of new PWM strategies for the CSC and their advantages in respect of switching loss and the reduction of harmonic content.

- To explore different modulation strategies for CSC.
- To develop modulation strategies for current source inverter by using the modulation technique of a voltage source inverter.
- To develop a direct Generalized Discontinuous Pulse Width Modulation (GDPWM) for the current source inverter using the space vector approach.
- Discussion about the direct space vector implementation of the CSI in linear and over modulation region.
- Develop model of a new closed loop controller for CSR for DC voltage regulation under unity power factor operation.

1.4 Organization of Thesis

Chapter 2 discusses the literature review on a three-phase CSI with a focus on papers written specifically about the PWM modulation strategies for the current source inverters. And also there is a review of the work done on CSR with emphasis on the input filter design strategy a control of the rectifier for DC voltage regulation under unity power factor operation.

Chapter 3 explains the operation of a CSI and the constraint involved in modulating a current source inverter and presents a model for a current source inverter with discussions on the advantages and disadvantages of the inverter.

Chapter 4 presents a new modulation strategy for the CSI using a developed PWM scheme for a voltage source inverter. Both sine triangle scheme and space vector

approaches have been developed. Both the simulation and experimental results have been presented to validate the proposed modulation strategy.

Chapter 5 presents new a Generalized Discontinuous Pulse Width Modulation (GDPWM) scheme for the current source converter using nine states of the CSI. A novel algorithm is proposed in order to satisfy the constraints of the current source inverter switching. Discussion about the direct space vector implementation modulation of the CSI in linear and over modulation region is done. Both the simulation and the experimental results have been presented to validate the proposed modulation schemes and the proposed algorithm for the converter.

Chapter 6 explains the operation of the three-phase current source rectifier, and explains a new approach followed in order to design the closed loop controller for the rectifier for output DC voltage regulation under unity power factor operation. All the steps involved in the controller design are very well laid out. A procedure for calculating control parameters is clearly explained and also the effect of some of the system parameter on the control scheme is discussed using the steady state simulation of the system for unity power factor operation. Some experimental results are presented to show the effectiveness of the controller.

Chapter 7 presents the hardware design aspects in building the prototype for CSI and CSR. The algorithm for generating six independent switching patterns using the PWM ports of the Digital Signal Processor (DSP), and necessary of overlap time are discussed.

Chapter 8 provides a summary of the contributions provided by this thesis and directions for future work in this area.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter presents a brief review of previous literature on modulation methods or novel inverter modulation strategies for the three-phase current source inverters and rectifiers, with some control aspects for current source rectifier.

First section of this chapter gives a brief review of the different offline and online modulation strategies developed for the current source type converter. It discusses different proposed algorithms in order to satisfy the constraints of the converter and their advantages and disadvantages are studied.

In the second section a review is given about the operation of different current source rectifier topologies, modulation strategies for the rectifiers, and about the different control schemes proposed for DC voltage regulation under unity power factor operation. It also gives a review of the different design techniques involved in designing of input side filter for the rectifier.

2.2 Current Source Inverter

Current Source Inverter (CSI) has been used in industry for many years to drive large horsepower motors. Some of the advantages of this converter are its sustained regenerative capabilities [B.4], short circuit protection, and its buffering of the drive output form supply voltage variations. Since its inception CSI has gradually changed over the years.

In 1970's, the most popular form of CSI developed was the auto sequentially commutated inverter (ASCI), which used thyristors and produced quasi-square wave output line currents. However, ASCI fed motor suffered from severe torque pulsations at low speeds due to the harmonic content in the line current. The need to correct this and other problems spurred research into finding ways to improve the performance of CSI's.

The most common method of reducing current harmonics is to pulse width modulate (PWM) the CSI output line currents. Therefore, with the advent of Power Bipolar Junction Transistors (BJT's) and Gate Turn-off Thyristors (GTO's), the ASCI has been gradually replaced by PWM CSI [B.5-B.8, B.19]. The use of gate turn-off thyristors and other power semiconductor devices with an intrinsic turn-off capability is making pulse width modulation (PWM) a reality for CSI. Hombu et al. [B.5, B.6] and Nonaka et al. [B.7, B.8] have described several schemes for implementing PWM strategies in current source inverters. However, previous work on PWM CSI's has been limited to constant modulation index operation and the output current variation achieved by varying the input DC current via rectifier control as seen in [B.5-B.8]. This approach, though it offers excellent performance in steady state, suffers from the lack of fast

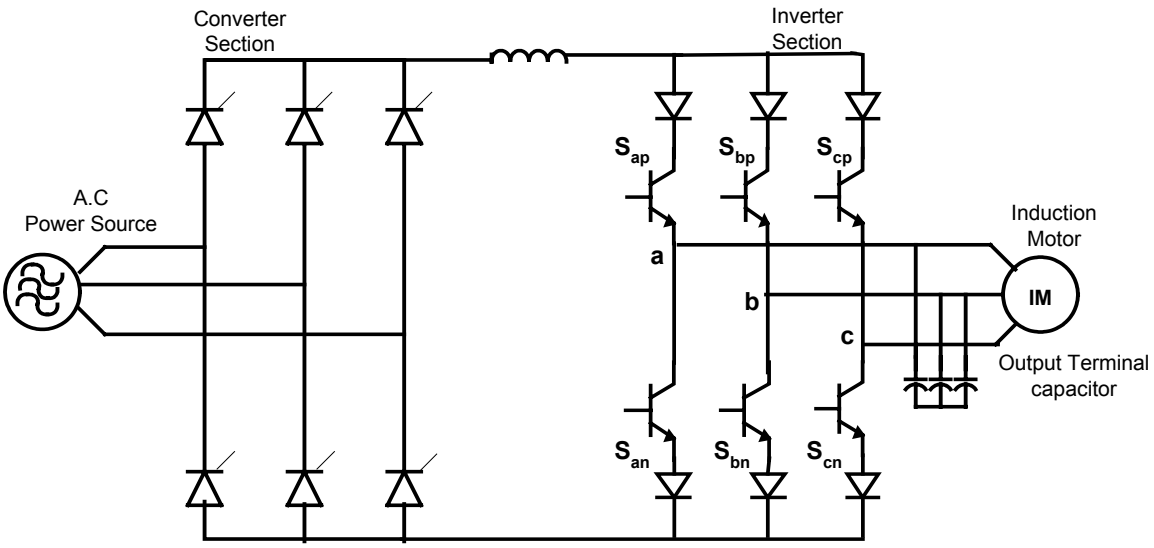


Figure 2.1 A high performance CSI with controllable rectifier at the input side.

response characteristics due to the presence of a large DC link filter inductor. Consequently, the transient response of the AC motors is severely limited.

Figure 2.1 shows a high performance CSI; it has a controllable rectifier at the input and an induction machine as a load at the output of the inverter. Many modulation strategies have been proposed for PWM current source inverter. In 1980's Hombu et al. [B.5, B.6] have proposed a new current source inverter with sinusoidal output voltage and currents. Six GTO's are used to form a three-phase bridge circuit, and overvoltage absorption capacitors are connected at the AC output terminals. For the PWM generation a trapezoidal modulating wave is compared with a triangular carrier wave to obtain a PWM controlled current output. In the PWM pattern storage memory, several current patterns are stored. This pattern storage memory, and shoot-through pulse generator are used so as to obtain the gate pulses for the GTO's. The pattern selector chooses an appropriate pattern from stored PWM patterns so that the GTO switching frequency will

be kept nearly constant and independent of the inverter frequency. But with the trapezoidal modulation for each phase is equivalent to tracking a reference around the outer boundary of the hexagon; i.e., were no null states used it implies, that the desired circular trajectory in d-q space is not achievable. In [B.6] the null states are used to smooth the transitions on the vertices of the hexagon; and thus reduces voltage spikes. In [B.5] null states are used to control the DC link voltage.

A modulation pattern was developed and analyzed for an eight–switch current source inverter, implementing neutral modulation in [B.9]. In this approach the space vector modulation analysis developed for VSI's are shown to apply for CSI. A fourth set of switch is added to the standard CSI to modulate the neutral point of the output capacitors. Thus to describe the two four pole switches, extra states are added to six existing states. So, using the total 12 vectors the desired current is approximated using the space vector approach. From the above analysis an improved modulation strategy was simply derived which reduces the voltage ripple on the load. But it has a drawback of using an extra switch in the topology [B.11]. States to add switches to the basic bridge configuration to provide alternative paths for the DC link reactor current to flow through as seen in [B.19, B.12]. With an extra switch, many restrictions on the PWM pattern can be removed and sinusoidal output currents and voltages can be obtained. However, these topologies have at least one of the following disadvantages

1. Cost of additional switch-some of them have four or more extra switches.
2. Sophisticated PWM techniques are required to produce sinusoidal output line currents.
3. In cases where extra switch(es) are connected across the DC bus, the modulation index is restricted to a high value. Otherwise, the extra switch(es) will short the DC bus for a

relatively large amount of time resulting in a rise of current through the DC link inductor, result in additional switching loss and low input power factor.

A Modified PWM CSI (MCSI) having sinusoidal output line currents without the disadvantages mentioned above has been presented in [B.10]. The MCSI topology differs from the conventional PWM CSI at the DC link where an extra switch has been added across the reactor. Firing of this extra switch is synchronized with the firing of the inverter switches; the switch is fired whenever there is no path for the current to flow in the inverter. This short circuits the DC-link reactor and allows the reactor current to freewheel. As a result, the DC bus current is chopped and it is equal to link reactor current or zero. This modified PWM current source inverter can operate with varying modulation indices and any standard VSI PWM switching pattern can be used for this inverter. This feature is obtained without compromising with the converter system efficiency and power factor, and at the cost of only one auxiliary switch .The added degree of freedom obtained through modulation index allows instantaneous control of output current and results in a high performance inverter system.

A new approach for the control of a current source PWM inverter is proposed in [B.13]. The approach is fully analyzed and experimentally investigated to achieve instantaneous current control capability. The proposed current source PWM inverter can respond to the current command signal instantaneously by varying the modulation index of the current source PWM patterns. In order to achieve this task, an optimal programmed PWM patterns with selective elimination of a lower order harmonic in the motor line currents are employed. The front side of this topology has a three-phase PWM rectifier. The rectifier and the DC link reactor comprise the system current source, the function of

this front-end converter is to regulate the DC-link current in response to load change. And at the output side it has a conventional three-phase current source inverter used to synthesize three phase currents. Modulation for the CSI is done using a programmed PWM pattern that selectively eliminates the lower order harmonics.

A generalized technique for realizing PWM patterns, that provides Selective Harmonic Elimination and current magnitude Modulation (SHEM) for Current Source Inverters/Rectifiers (CSI/R) is presented in [B.14]. A combination of chops and short circuit pulses are positioned in such a way that lower order harmonics are eliminated selectively besides current magnitude modulation with minimum switching frequency. Generalized equations and tables, which show relationship of various PWM-SHEM parameters to the position of short circuit pulses and the number of chops per 30^{o}, are provided and discussed in detail.

An online PWM pattern generation techniques in which the states of VSI are mapped to state of CSI with a simple logic circuit is presented. The mapping technique was developed using sine triangle PWM and using Space vector approach. But the only drawback of this method is that, proper explanation for the derivation of logic circuit is not given in [B.15]. Using the above similar online PWM strategy, [B.16] has proposed an improved modulation for selective harmonic elimination in synthesized currents and voltages. A method of improved voltage regulation for CSI has been developed and a control scheme for a better regulation of the voltages at the output side capacitor is presented in [B.17].

A Linearizing Pulse Width Modulator (LPWM) is presented in [B.18], which linearizes the control-to-output characteristics of the three phase inverters employing

single-pole multiple-throw switch. The paper shows how such an LPWM can be realized using integrator, hold and reset which are familiar building blocks in mixed signal integrated circuits. In this scheme in order to synthesize the three-phase reference voltages a combination of space vector modulation (SVM) and (LPWM) referred to as LSVM, (Linearizing Space-Vector Modulation) is employed. A hardware module is developed which uses basic integrators, reset and hold circuits, enables the output voltages of a nonlinear three-phase boost inverter to track the control signals linearly, and improves line voltage regulation.

2.3 Current Source Rectifiers

The input and output performance of three-phase AC/DC converters can be greatly improved by using pulse-width modulation (PWM) technique. Significant benefits are obtained as regards AC power factor, line current distortion, and output ripple. This implies substantial reduction of the reactive power compensation and filter requirements on the DC and the AC side of the rectifier. Among all the PWM operated rectifiers, Current Source Rectifier (CSR) with optimum control techniques allows distortion-free input currents, perfectly smoothed DC voltage and also freedom of full range of regulation can be obtained. Many researchers have been working on PWM rectifier to attain better quality of input current and simple control for voltage regulation and to attain unity power factor.

A control technique giving full regulation of the output voltage while maintaining the desired input performances is proposed in [C.1]. A feedforward PWM technique is employed in this work. The feedforward PWM generator produces logic signals, which determine the status of the six switches of the bridge. The operating intervals are recognized depending on the instantaneous relative amplitudes of reference currents. Actual implementations of these functions for PWM can be done either by discrete logic or by means of microprocessor. And some filter design techniques are proposed for maximum DC output voltage and to minimize the ripple due to the modulation.

Following the classic paper of Hombu, Ueda, Ueda, and Matsuda [B.5-B.8], much research has been devoted to the development of the three levels or trilogic PWM. [C.2] proposed a trilogic PWM technique for CSR, the trilogic PWM is a method of synthesizing the three level logic signals required for the 6-device current- source bridge converter. This work developed a method of translating the biologic PWM signals to trilogic PWM signals that can be used in all 6-device, current–source PWM converters. In both the inverters and rectifier applications, experimental demonstration has been done to show the ability of the strategy to operate as a linear amplifier.

A new delta-modulated scheme for Buck type three-phase PWM rectifier has been described in [C.3]. These rectifiers are intended to be used in conjunction with the controlled current source inverters. An outer proportional feedback loop regulates the unidirectional output current flowing through the DC link. An inner feedback loop maintains near sinusoidal currents waveforms at unity power factor from the utility power supply. The inner loop controls the current indirectly by delta modulation of the voltage across the ac terminals of the converter. Delta modulation: In delta modulation if the

input side capacitor voltage gradient is ascending then S_a = -1 and if the gradient descending then the S_a = +1. In this modulation the voltage trajectory is made to follow a reference voltage with a specified tolerance band. The capacitor voltage is measured and compared with the reference signals and PWM switching pattern is developed depending upon the band.

In order to overcome the LC filter resonance problem especially in transient condition a state feedback control is introduced in [C.4], and a control strategy suitable for the DC output current as well as the AC side current control is proposed. Circuit parameters and feedback coefficients in the AC-side-current control system are treated as a sampled data system. The control strategy is based on a novel viewpoint of a rectifier; that is, it can be regarded as a controlled DC voltage source when it is viewed from its ac side and DC side, respectively. With this control strategy, both the gain of DC output voltage control and gain of the AC side current control are kept constant regardless of the value of the DC output current. Therefore, the parameters and the coefficients in these two control systems can be investigated separately.

Some steady state analysis, dynamic and small signal performance of the three-phase AC/DC buck rectifier using pulse width modulation magnitude and control has been done in [C.5]. Using the transformed nonlinear equations a simplified steady state and small signal model is presented; unity power factor operation of the converter is extremely studied. To eliminate the lower order harmonics a systematic and a user-friendly approach in choosing the filter components is presented. Designing of the LC filter involves the positioning of the resonant frequency to meet the harmonic attenuation requirements, and introduce the damping at the resonant frequency to avoid amplification

of residual harmonics [C.6]. A control algorithm is proposed for CSR in [C.7], with a input filter. The algorithm employs a separate control loop for compensation of the input current displacement factor in steady state, in addition to the standard output voltage regulation loop. This algorithm allows a separate design for the input filter and of closed loop output voltage control. A control method for CSR, is presented which provides active damping function to the rectifier. This damping function is effective only on the harmonic components of AC input current. The transient oscillations in the steady state are reduced by this damping effect. From the analytical results, the influence of the circuit parameters and control delay on the active damping effects and the stability of the operation are clarified in [C.8].

A nonlinear control technique is developed in [C.9]; a nonlinear control technique that introduces more flexibility in the control of the rectifier and results in a more straightforward approach for controller design. The proposed technique is based on a nonlinear state variable feedback approach in the synchronous rotating reference frame. The approach allows the independent control of the two components of the line current with the same performance regardless of the operating point. The control strategy also eliminates the need of the input damping resistors and rejects the effect of supply voltage variation. Space vector method is also used for maximum utilization of the supply voltage.

An analysis of the CSR in transient and steady state is presented in [C.11], the models are developed in synchronous reference frame. The load behavior is characterized for two load conditions, resistive load and for a constant power load. Several static converter characteristics such as power factor, real and reactive power are analyzed for

both types of load. Transient characteristics are analyzed for both types of load by exact small-signal model with full set of equations [C.10]. Static and dynamic characteristics of buck–type three-phase PWM rectifiers are fully analyzed based on the DC and AC circuit models developed by the circuit q-d transformation.

A control system is proposed in which the active and reactive power is independently controlled with real and imaginary axis components of the supply current vector. A new damping method for supply current oscillations was introduced in [C.12]. An active damping control method is proposed for the reduction in line currents THD of high power CSR, two types of LC resonances are investigated in [C.13], the parallel resonance excited by harmonic currents drawn by the rectifier and the series resonance caused by harmonic pollution in the source voltage.

2.4 Summary

It was mentioned earlier that each of these controls and modulation strategies of CSI/CSR has advantages and disadvantages. The disadvantages of the [B.5 – B.6] [B.19], strategies is that these modulation schemes use an extra switch in the converter topology, which increases the effective cost of the system. Some of the modulation schemes do not synthesize currents directly, they use offline programmed PWM patterns, which are not suitable for control applications. For the phase and amplitude control, the advantage is that the optimal switching pattern can be used to reduce the input current and output voltage ripple. And it is able to control the output voltage and achieve unity power factor

at the same time. Its disadvantages are its slow dynamic response and a DC current offset during transients. The thyristor current control is the simplest one to built and has fast dynamic response, but its random and uneven switching pattern can cause excessive stress on devices. The line voltage orientation control has fast dynamic response. On the other hand, it is complicated to implement. The predicted current control with a fixed switching frequency has a fast dynamic response and it is easy to implement at the same time. However, it does not have the ability to control two outputs at the same time, since it has only one input control.

The objective of this thesis is to develop a new control strategy for the CSR, which has the least amount of input current harmonic and output voltage ripple, and to be able to regulate output DC voltage under unity power factor at the supply. There is not much work done on the detailed analysis, especially with regards to the dynamic response of this converter. One of the reasons might be because the mathematical model of the PWM converter is discontinuous, time varying, and nonlinear and thus, it is hard to find the solution. This thesis will lead to a new design strategy in industry application which will eventually reduce or eliminate those weakness mentioned earlier.

CHAPTER 3

MODELING AND OPERATION OF A THREE-PHASE CURRENT SOURCE INVERTER

3.1 Introduction

The most common inverter topology for variable speed drive systems is a three-phase pulse width modulated Voltage Source Inverter (VSI). This topology has the advantage of being simplistic when DC supply is from a rectifier and is stable open-loop operation using a constant–volts–per hertz characteristic. As a result, optimization of open-loop voltage control and closed loop current control strategies for VSI has been major research areas for decades. However, due to the nature of the VSI topology, it cannot regenerate an incoming AC supply without a complex rectifying converter, and it also provides large d_v/d_t transitions on the phase leg output voltage. These transitions can lead to problems, such as increased motor noise in the load and insulation degradation because of voltage surges.

An alternate topology to a Voltage Source Inverter (VSI) is a Current Source Inverter (CSI) is as shown in Figure 3.1, It has the advantages of directly supporting regeneration back to the AC supply when supplied from an SCR rectifier, implicit output, and short circuit protection, and significant reduction in load harmonics because of the voltage filtering that occurs at the output capacitors of the inverter.

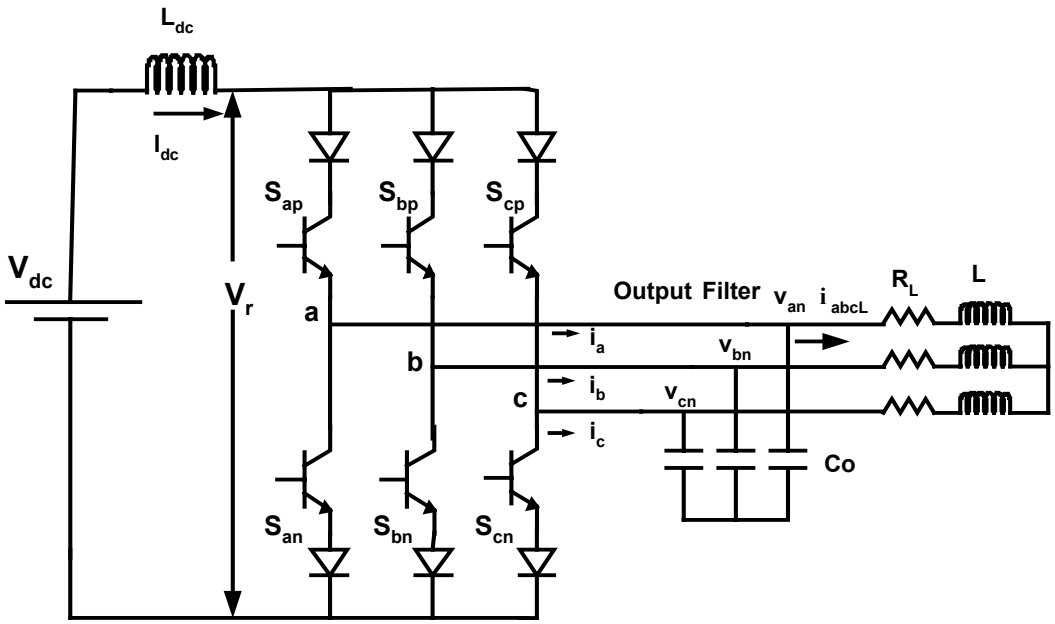


Figure 3.1 Schematic of CSI for connected to three-phase R-L load.

CSI topologies have certain performance advantages in terms of ruggedness and their capability to feed capacitive and low impedance loads with ease. Although modulation and control strategies for a CSI are much less developed than for a VSI, some advances have been made in applying pulse width modulation (PWM) theory as mentioned in [B.24] to control these inverters.

This chapter discusses about the basic principle of operation of a CSI. It deals with the constraints involved while switching a CSI in order to satisfy the Kirchhoffs Voltage and Kirchhoff's Current Law's. The mathematical model of the inverter and also derivation of the expressions for the modulating signal using the constraints and the model equations is presented.

3.2 Square Wave Operation

Figure 3.2 illustrates the gating signals for square wave operation of a CSI. In this mode of operation rapid changes in output current transitions causes voltage spikes across inductive loads [A.4]. Thus in practice, to allow the device to operate in a Safe Operating Area (S.O.A.), the commutation between the high power devices is slowed. The square wave inverter does not provide for the magnitude control of the output current within the inverter, hence the rectifier supplying the inverter controls the current. The rectifier aids in bi-directional power flow thus allowing simplicity and reliability in the dynamic current control in high performance AC drives.

Figure 3.2 shows plots of the time versus switching devices and neutral currents. S_{ap}, S_{an}, S_{bp}, $S_{bn,}$ S_{cp}, S_{cn} represent the top (p) and bottom (n) switching functions, and i_{as}, i_{bs}, i_{cs} are the three phase line currents. Fourier analysis of these waveforms yields a simple square–wave type of geometric progression of the harmonics. When written as an explicit time function, the Fourier expansion for the time varying line current can be easily determined. The disadvantage is that the output current stepped waveform introduces high distortion in the waveform quality.

$$i_{as}(t) = I_{dc}\frac{4}{\pi}\left[\frac{\pi}{4} + \sin\omega_o t + \frac{1}{3}\sin 3\omega_o t + \frac{1}{5}\sin 5\omega_o t + \frac{1}{7}\sin 7\omega_o t + ...\right] \quad (3.1)$$

The b and c phase currents are given by replacing $\omega_o t$ with $\omega_o t - 2\pi/3$ and $\omega_o t + 2\pi/3$, respectively. From Equation 3.1; line-to-line current I_{ab} is given as

$$i_{ab}(t) = I_{dc}\frac{4\sqrt{3}}{\pi}\left[\sin(\omega_o t + \frac{\pi}{6}) + \frac{1}{5}\sin(5\omega_o t - \frac{\pi}{6}) + \frac{1}{7}\sin(7\omega_o t + \frac{\pi}{6}) + ...\right]. \quad (3.2)$$

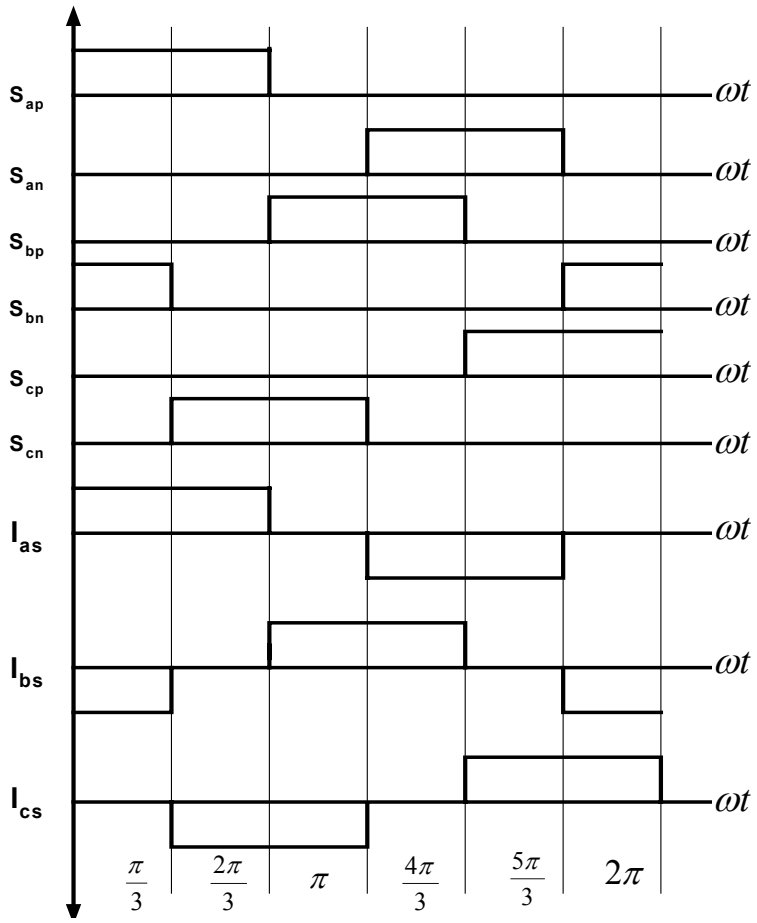


Figure 3.2 Gating signals and output currents of three-phase current source inverter in square wave mode.

Similar relationship can be found for I_{bc} and I_{ca} currents, phase shifted by $-\frac{2\pi}{3}$ and $\frac{2\pi}{3}$, respectively. Note that the harmonics of the order of multiples of three are absent from the line-to-line current, since these *triple* harmonic cancel between the phase legs. In terms of RMS value, each harmonic of the line- neutral current has the value of

$$I_{n,\ln,rms} = I_{dc}\frac{2\sqrt{2}}{\pi}\frac{1}{n}. \tag{3.3}$$

For line–to-line currents

$$I_{ll,rms} = I_{dc}\frac{2\sqrt{6}}{\pi}\frac{1}{n} \tag{3.4}$$

where $n = 6k \pm 1$, k = 1,2,3……..

Because of its utility as a reference value for pulse width modulation, in later chapters, it is useful to write the fundamental component of the line-to-line current in terms of its peak value.

$$I_{1,\ln,pk} = I_{dc}\frac{4}{\pi} \tag{3.5}$$

This value is the fundamental component of a square wave of amplitude I_{dc}. It is thus mandatory to develop the PWM scheme in order to reduce the switching transients and improve output voltage as well as current waveform quality.

3.3 PWM Operation

Areas of application for power converters are expanding rapidly due to the improvement in semiconductor technology, which offers high voltage and current ratings as well as better switching characteristics [B.4]. The main advantages of modern power electronic converters, such as high efficiency, low weight, small dimensions, fast operation, and high power densities are being achieved through the use of the so–called switch mode operation, in which power semiconductor devices are controlled in ON/OFF fashion. Different PWM methods have been developed such as:

1. Sine triangle comparison technique.
2. Direct digital implementation using space vector approach.

Basic requirements of PWM converters are:

- Wide range of linear operation.
- Minimum number of switching to maintain low switching losses in power components.
- Minimal content of harmonics in voltage and current, because they produce additional losses and noise in load.
- Elimination of low-frequency harmonics.
- Operation in over modulation region including square wave.

3.3.1. Sine Triangle Comparison Technique

Sine triangle PWM (SPWM) method is also known as the triangulation, sub harmonic, or sub oscillation method. This technique was first proposed by Schonung and Stemmler in 1964. In this technique a modulating signal (reference signal) V_r, which has the characteristics of the desired voltage or current, is compared with a high frequency triangular (carrier signal) V_c. Intersection of V_c and V_r determines the switching instants and commutation of the modulated pulse. The PWM scheme is illustrated in Figure 3.3 in which V_c is the peak value of triangular carrier wave and V_r is the peak of the reference wave. Figure 3.3 shows the triangle and the three modulating signals, which are phase shifted with an angle of 120^o having some arbitrary frequency and magnitude. The switching pattern of these comparisons is shown in Figure 3.3 (b), (c), (d). If the

magnitude of the reference wave V_r is greater then the magnitude of the triangle wave V_c or carrier signal then switch is turned ON.

i.e., if $V_r > V_c$ then S = 1 switch is turned ON

$V_r < V_c$ then S = 1 switch is turned OFF

If the modulating signal is a continuous signal then the PWM is known as the Continuous Pulse Width Modulation (CPWM) and if the modulating signals is a discontinuous signal then the PWM is known as Discontinuous Pulse Width Modulation (DPWM).

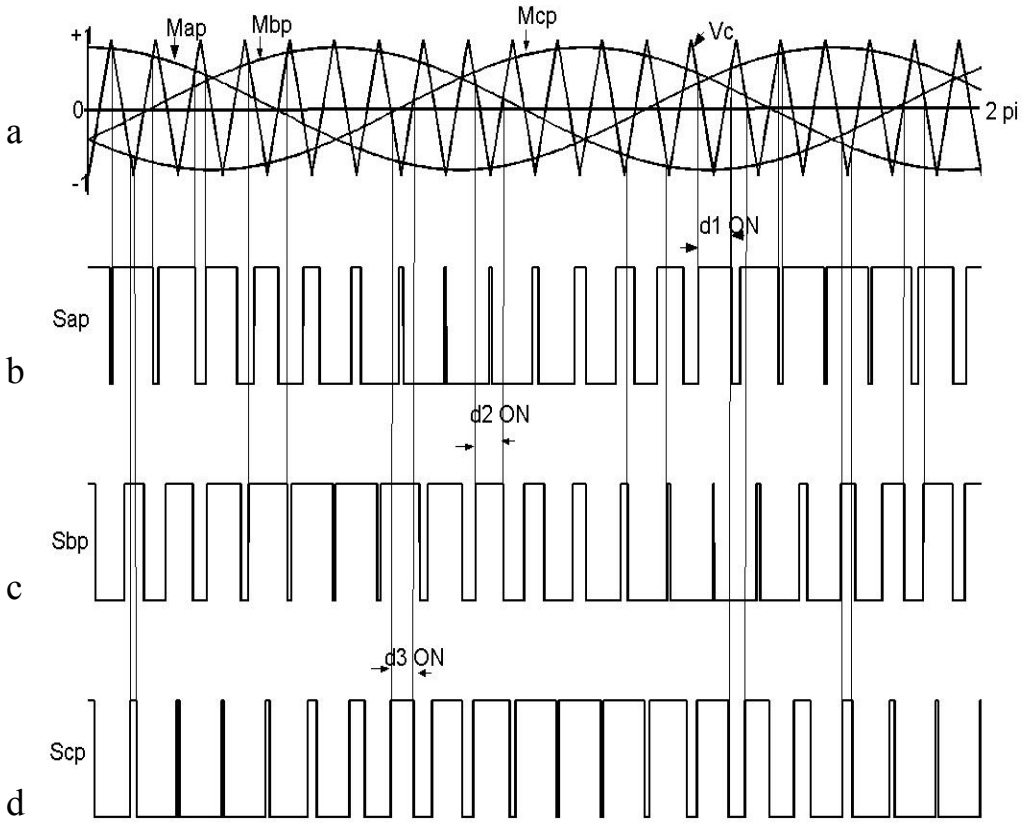


Figure 3.3 Three-phase continuous switching pattern (a) Three phase reference signals (M_{ap}, M_{bp}, M_{cp}) and carrier triangle wave (b) phase 'a' switching function (S_{ap}) (c) phase 'b' switching function (S_{bp}) (d) phase 'c' switching function (S_{cp}).

3.3.2 Direct Digital PWM Technique

In this approach the Space Vector Modulation methodology (SVM) is used. The SVM strategy is based on space vector representation of the converter AC side voltages or currents and is very popular because of its simplicity. The direct digital technique involves utilization of space vector approach in which the duty cycles for the switching inverter are calculated. The gating signals are pre-sequenced and stored in a lookup table. In a converter the active vectors divide the plane into different sectors depending upon the number of active vectors and also the zero switching vectors. Whereas reference vector U^* which has to be synthesized is obtained by switching ON (for the proper time) two adjacent vectors of a sector in which U^* resides. It is seen that this vector can be generated by different switch ON/OFF sequence of U_1 and U_2. In brief this method calculates the total time for the switch to be turned ON or turned OFF in order to synthesize the reference currents. A powerful microprocessor or a DSP can be used to generate the switching times.

3.4 Mathematical Representation of Switching Function

Fourier series can be used in making analysis of the switching function, since the switching pattern of the devices is a periodic function. Let the repetition frequency of the pulses be f with a time-period $T=1/f$, and angular frequency $\omega = 2\pi f$ then $\omega T = 2\pi$

radians. If the angular duration of the unit-value period is $2\pi/A$ when $A \geq 1$, then the boundaries of the unit-value period with respect to the time zero reference are $-\pi/A$ and π/A radians, the Fourier series for this periodic signal is given in Equation (3.6)

$$H(\omega t) = \sum_{n=0}^{n=\infty} [C_n \cos(n\omega t) + S_n \sin(n\omega t)]. \tag{3.6}$$

From the standard determination of co-efficient for a Fourier expansion:

$$S_n = \frac{2}{T} \int_{T/2}^{T/2} H \sin(n\omega t) dt$$

$$\frac{1}{\pi} \int_{\pi/A}^{\pi/A} H \sin(n\omega t) d\omega t = 0 \tag{3.7}$$

$$C_0 = \frac{1}{T} \int_{T/2}^{T/2} H dt$$

$$\frac{1}{2\pi} \int_{\pi}^{\pi} H d\omega t = 1/\mathrm{A} \tag{3.8}$$

$$C_n (n \neq 0) = \frac{2}{T} \int_{-T/2}^{T/2} H \cos(n\omega t) dt$$

$$= \frac{1}{\pi} \int_{-\pi/A}^{\pi/A} \cos(n\omega t) d\omega t \tag{3.9}$$

$$= \frac{2}{\pi} \sin(n\pi / A) / n$$

Thus $H(\omega t) = \frac{1}{A} + \frac{2}{\pi} \sum_{n=1}^{n=\infty} [\sin(n\pi / A)] \cos(n\omega t)$. (3.10)

The expression (3.5) can be given as

$$H(\omega t) = \frac{1}{\pi} \sum_{n=-\infty}^{n=\infty} [\sin(n\pi / A)] \cos(n\omega t) \ . \tag{3.11}$$

Since cos(ωt) = cos(n(ωt-2kπ/A)) Equation (3.5) can be written as

$$H(\omega t) = \frac{1}{A} + \frac{2}{\pi}\sum_{n=1}^{n=\infty}[\sin(n\pi / A)]\cos(n(\omega t - 2k\pi / A)\,. \tag{3.12}$$

In the above equation A can be an integer, rational, or an irrational number. In Equation (3.12) all those terms in which n is an integer multiple of A vanish, and so it reduces to a fundamental component and a time varying term. Thus the switching pulses can be represented as a dc component and a cos or sine varying term as in Equation (3.13),

$$S = \frac{1}{A} + M \tag{3.13}$$

where M is called the modulating signal, which can be any sine or cos term (in accordance to Fourier series) depending on the control we want to implement. The more general fundamental component for M is given as

$$M = M_i \cos(\omega t - \alpha) \tag{3.14}$$

for a three phase switching function modulating signals are given by

$$M_a = M_i \cos(\omega t - \alpha) \tag{3.15}$$

$$M_b = M_i \cos(\omega t - \alpha - 120^o) \tag{3.16}$$

$$M_c = M_i \cos(\omega t - \alpha + 120^o) \tag{3.17}$$

in the above expressions M_i is called the modulation index.

3.5 Operation of a Current Source Inverter

Similar to a VSI the CSI also has a three-phase bridge circuit. In the case of CSI, the input side has a DC supply with a very big smoothing reactor which removes the ripple in the DC current. It has a three-phase bridge circuit as shown in Figure 3.1, which has two devices in each leg and has a diode in series with each device. A switch thrown in the current source converter can be realized as a bi-directional voltage blocking and a unidirectional current carrying device. The output of the bridge circuit has a three-phase capacitor bank to filter the current harmonics and provide sinusoidal load voltages and load currents. In case of a CSR it has a three-phase supply at the input side and three-phase shunt capacitor bank at the AC side to filter the current harmonics in the line current. It has a three-phase bridge circuit with two devices in each leg and a reverse blocking diode placed in series with the device. The output of the bridge has an inductor to filter the ripples in the DC current and a DC-link capacitor on the load side. The PWM operation for the two converters, i.e., CSI and CSR will be the same. In the case of a CSI the references signals will be the normalized three phase currents that has to be synthesized at the output side. For the rectifier the reference signals will be the normalized three-phase input line currents. In modulating the CSI or CSR the switching should be such that it satisfies the Kirchhoff's voltage and current laws.

3.6 Kirchhoff's Voltage Law

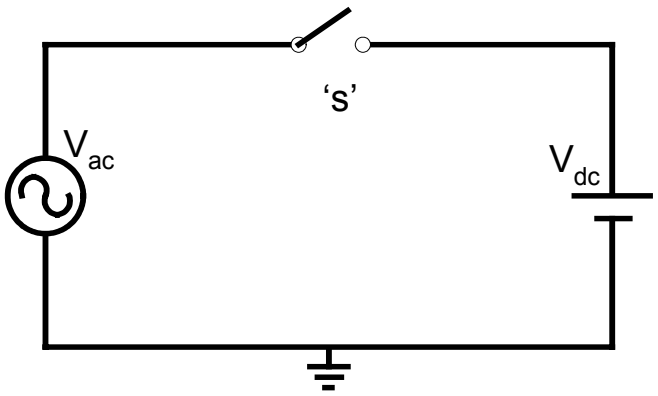


Figure 3.4: Demonstration of KVL

Care has to be taken while switching the converter matrix, that it does not violate Kirchhoff's Voltage Law (KVL) i.e., two unequal voltages should never be connected without any element in between which can account for the inequality in two voltages. Consider the circuit shown in the Figure 3.4. This circuit can be operated with the switch 'S' closed owing to the fact that when the switch is closed the sum of the voltages around the loop is not equal to zero. In reality a very large current will flow and this voltage drop appears across the wires and may result in burning of the wires.

In a CSC, in order to satisfy the KVL no two devices in the top and bottom should be turned ON at the same time, as this will short the output side capacitors; i.e., at every instant it has to satisfy the following conditions.

$$S_{ap}.S_{bp} = 0,\ S_{bp}.S_{cp} = 0,\ S_{ap}.S_{cp} = 0 \tag{3.18}$$

$$S_{an}.S_{bn} = 0,\ S_{bn}.S_{cn} = 0,\ S_{an}.S_{cn} = 0$$

S_{ap}, S_{bp}, S_{cp} are the switching function of top three devices, S_{an}, S_{bn}, S_{cn} are those of the bottom three devices. Equation (3.6) states that the product of any two devices in the top and in the bottom should always be zero which implies that no two devices from the top and no two devices from the bottom should be turned ON at the same time to satisfy the KVL condition and avoid short circuit in the system.

3.7 Kirchhoff's Current Law

As already discussed in section 3.5, Kirchhoff's Current Law (KCL) has to be similarly satisfied, while switching the converter matrix. It states that the sum of the currents at a node should be equal to zero at all times. Thus any circuit in which KCL is not satisfied is dangerous to operate, as it may get open-circuited. Consider the circuit in Figure 3.5, which can be operated if the switch 'S' is closed. If it is open, that particular path is open so the current is zero and the other two current sources are unequal which violates KCL, as the sum of the currents entering the node is not equal to zero.

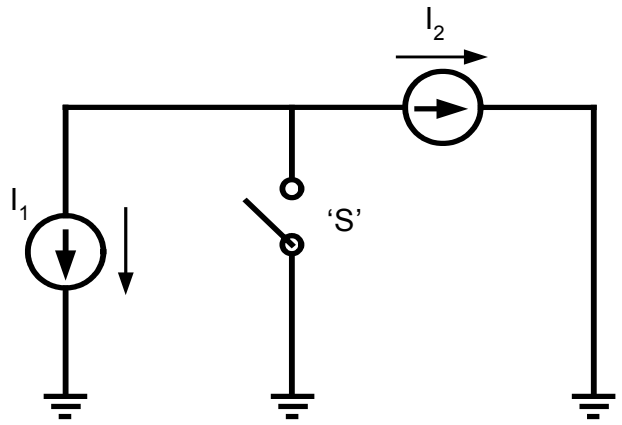


Figure 3.5 Demonstration of KCL

In a current source inverter in order to satisfy the KCL, at least one top device and one bottom device should be turned on to avoid the open circuit of the input side of the converter; i.e., at any instant it has to satisfy the condition:

$$S_{ap} + S_{bp} + S_{cp} = 1 \ , \ S_{an} + S_{bn} + S_{cn} = 1 \ . \tag{3.19}$$

From Equation (3.7) the sum of the switching function of the top three devices and bottom three devices should be unity, which describes that one of the devices from the top three devices and one of the devices from the bottom three devices should always be turned ON. This ensures that KCL is always satisfied there is no open circuit in the system and the input current always flows to the output load.

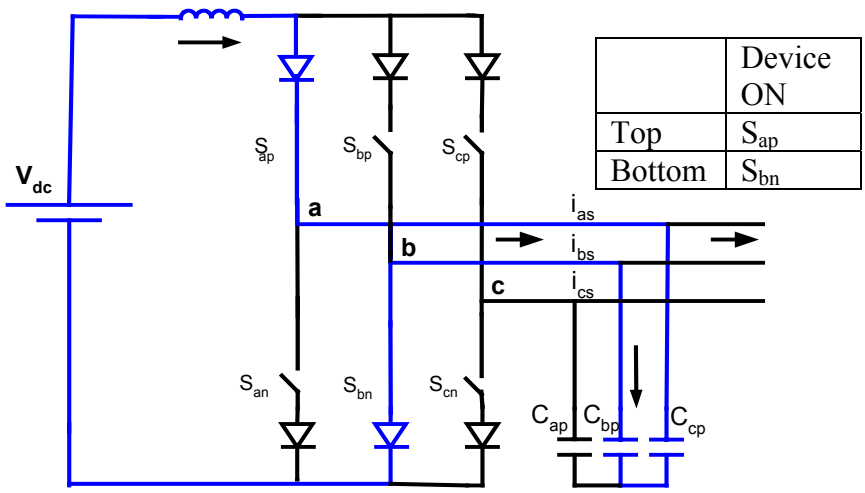
3.8 Modes of Operation of a CSI

There are nine modes of operation in a CSI, based on the switching among the switches in the bridge circuit to satisfy KVL and KCL. Table 3.1 shows the current flowing from source to load in each state of operation and also lists the turned ON device and the corresponding amount of current flowing in each phase at the output side.

Table 3.1 Possible switching modes of three-phase CSI.

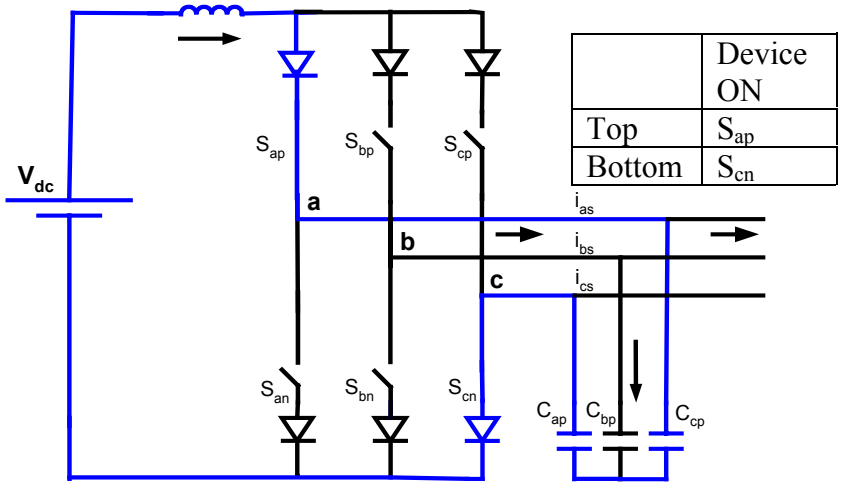
ON Device	**ON Device**	$\mathbf{i_{as}}$	$\mathbf{i_{bs}}$	$\mathbf{i_{cs}}$
S_{ap}	S_{bn}	I_d	$-I_d$	0
S_{ap}	S_{cn}	I_d	0	$-I_d$
S_{bp}	S_{an}	$-I_d$	I_d	0
S_{bp}	S_{cn}	0	I_d	$-I_d$
S_{cp}	S_{an}	$-I_d$	0	I_d
S_{cp}	S_{bn}	0	$-I_d$	I_d
S_{ap}	S_{an}	0	0	0
S_{bp}	S_{bn}	0	0	0
S_{cp}	S_{cn}	0	0	0

Mode I



Mode II

(I)

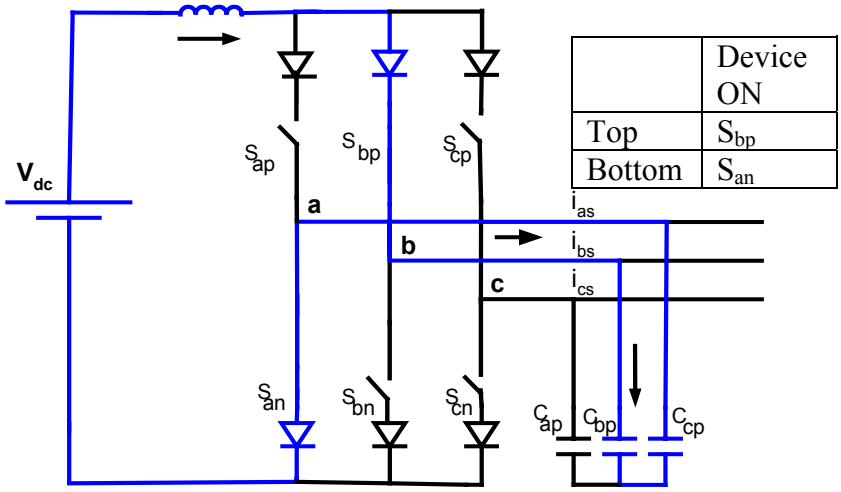


(II)

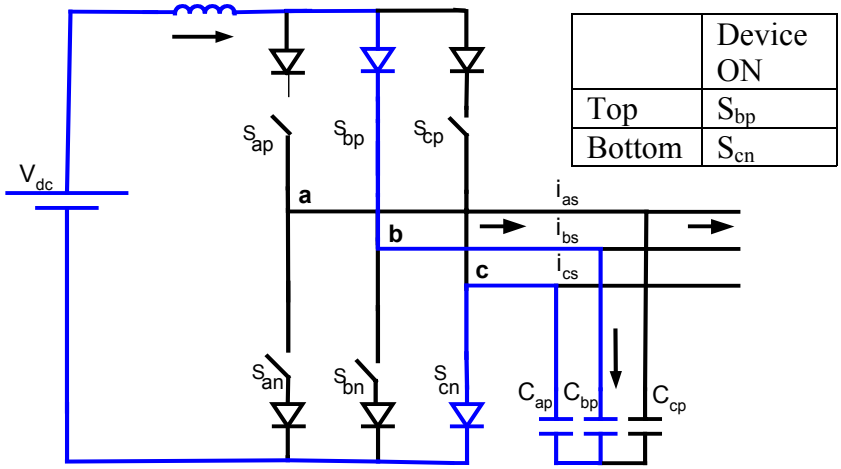
Figure 3.6 (I) and (II) Schematic of CSI showing mode I and II of operation.

Figure 3.6 (I) The mode I of operation in which phase 'a' top device is turned ON and phase 'b' bottom device is turned ON which makes current I_{dc} flows through the phase 'a' and $-I_{dc}$ flows through phase 'b'. Figure 3.6 (II) The mode II of operation in which phase 'a' top device is turned ON and phase 'c' bottom device is turned ON which makes current I_{dc} flows through the phase 'a' and $-I_{dc}$ flows through phase 'c'.

Mode III



Mode IV **(I)**

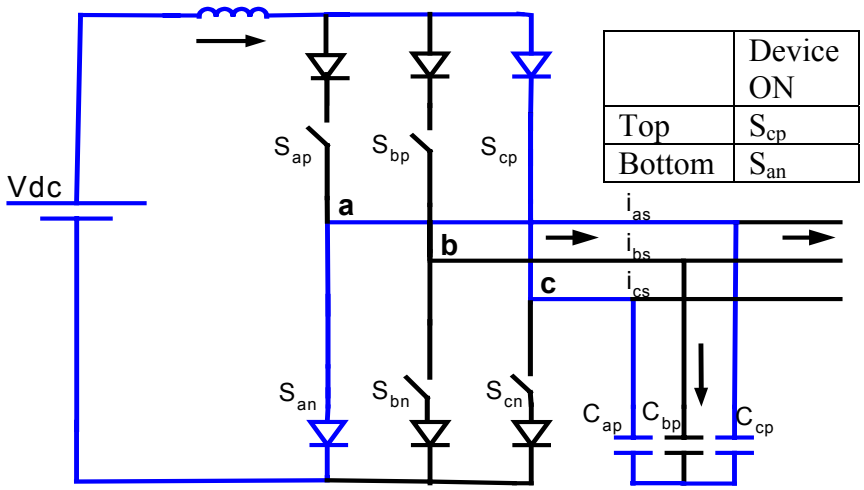


((II)

Figure 3.7 (I) and (II) Schematic of CSI showing mode III and VI of operation.

Figure 3.7 (I) The mode III of operation in which phase 'b' top device is turned ON and phase 'a' bottom device is turned ON which makes current I_{dc} flows through the phase 'b' and $-I_{dc}$ flows through phase 'a'. Figure 3.7 (III) The mode IV of operation in which phase 'b' top device is turned ON and phase 'c' bottom device is turned ON which makes current I_{dc} flows through the phase 'b' and $-I_{dc}$ flows through phase 'c'.

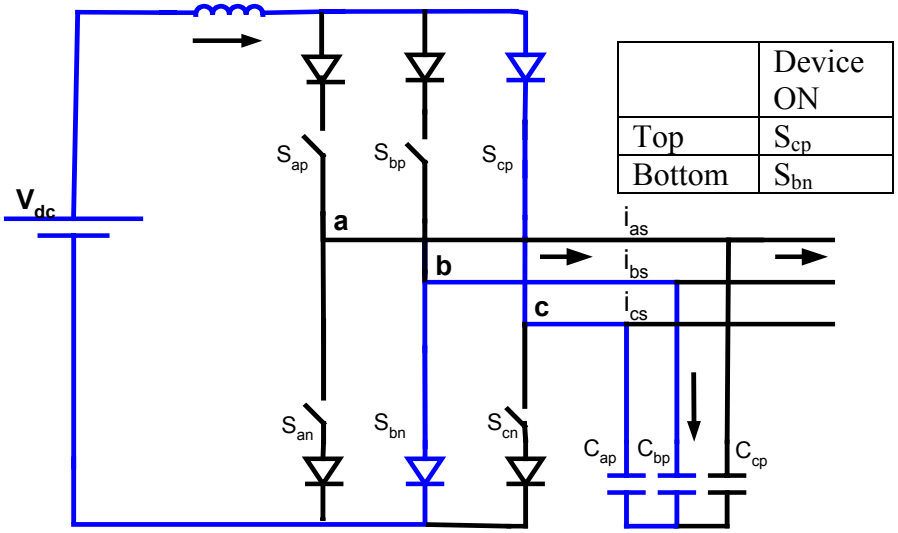
Mode V



	Device ON
Top	S_{cp}
Bottom	S_{an}

(I)

Mode VI

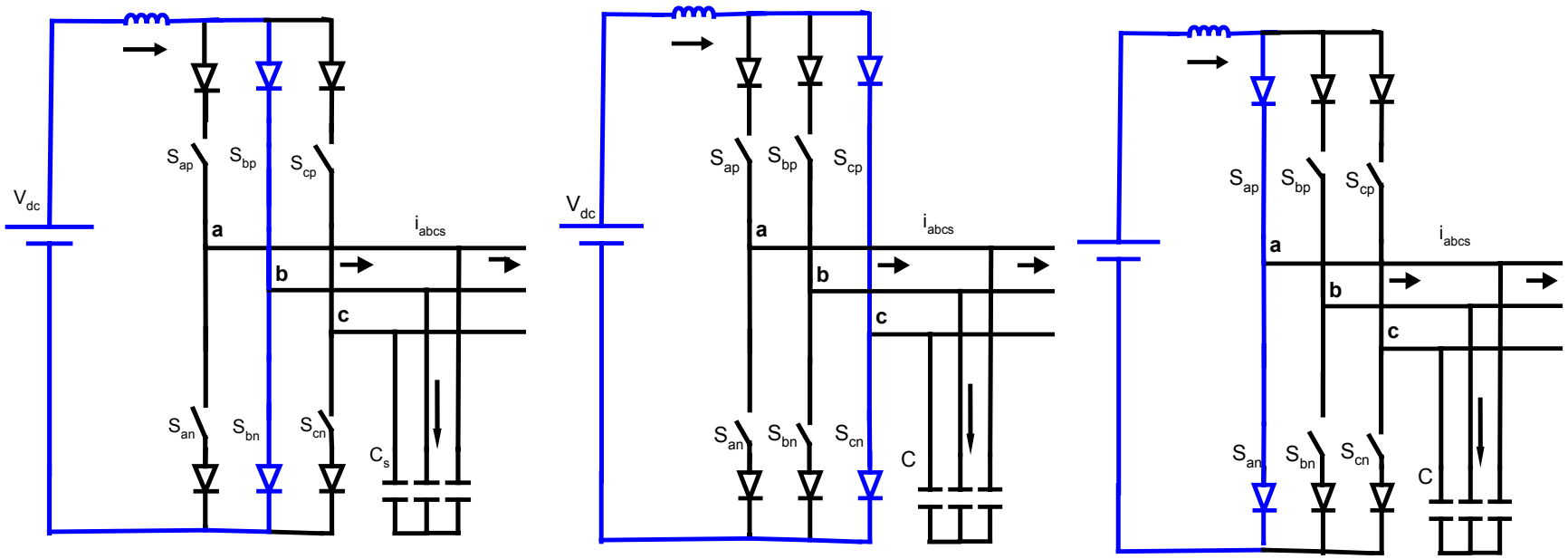


	Device ON
Top	S_{cp}
Bottom	S_{bn}

(II)

Figure 3.8 (I) and (II) Schematic of CSI showing mode V and VI of operation.

Figure 3.8 (I) The mode of V of operation in which phase ‘c’ top device is turned ON and phase ‘a’ bottom device is turned ON which makes current I_{dc} flows through the phase ‘c’ and $-I_{dc}$ flows through phase ‘a’. Figure 3.9 (II) The mode VI of operation in which phase ‘c’ top device is turned ON and phase ‘b’ bottom device is turned ON which makes current I_{dc} flows through the phase ‘c’ and $-I_{dc}$ flows through phase ‘b’.



(I) **(II)** **(III)**

	Device ON
Top	S_{ap}
Bottom	S_{an}

	Device ON
Top	S_{bp}
Bottom	S_{bn}

	Device ON
Top	S_{cp}
Bottom	S_{cn}

Figure 3. 9 Schematic of CSI showing (I) Mode VII (II) Mode VIII (III) Mode IX

Figure 3.9 shows mode VII, VIII, IX of operation, in these modes of operation both the top and bottom devices in the same leg are switched ON at the same time. Such that no current is transferred from the source to the load. These states of operation are termed as null states because these states do not generate any current to the load side. They are shown in following Figure 3.12.There are six active Modes and three null modes of operation. Null states act as free wheeling states.

3.9 Modeling of Three Phase CSI

Figure 3.13 shows the schematic diagram of the three-phase CSI with star connected R-L load and all the quantities in Figure 3.13 are described in Table 3.2. By applying KVL and KCL conditions, the model equations can be written for the topology and use the model equations to simulate the system.

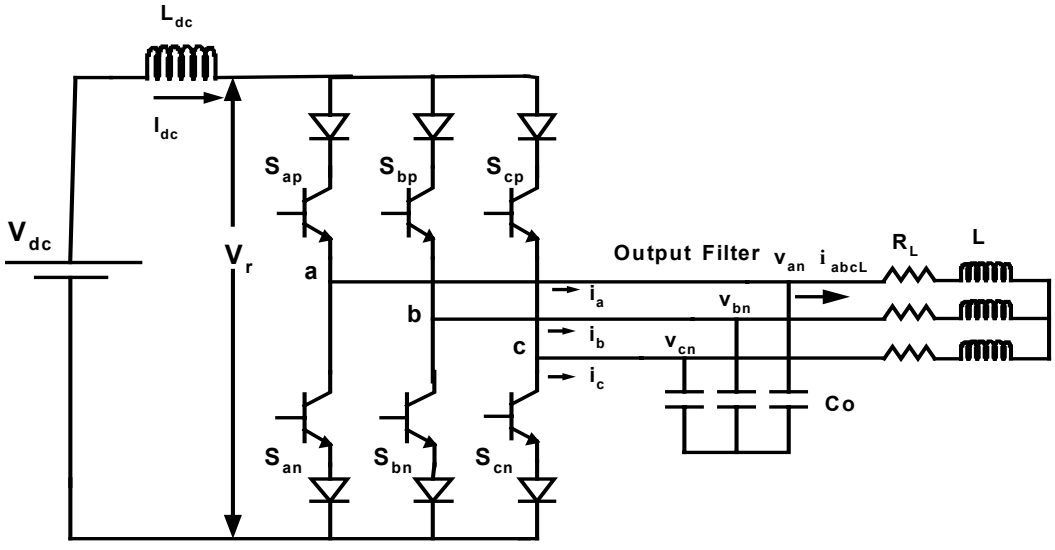


Figure 3.10 Circuit diagram of three-phase CSI with star connected R-L load.

Table 3.2 Terminology used in modeling of CSI

Parameters	Description
v_{an}, v_{bn}, v_{cn}	Three phase output capacitor voltages
i_a, i_b, i_c	Three phase output currents for the inverter
i_{al} , i_{bl}, i_{cl}	Three phase load currents
R_L , L	Load resistance and load inductor
L_{dc}	Input load resistance
I_{dc}	Input DC current
V_{dc}	Input DC voltage
S_{ap}, S_{bp}, S_{cp}	Top three devices
S_{an}, S_{bn}, S_{cn}	Bottom three devices

Writing the KVL equation at the source side

$$LpI_{dc} = V_{dc} - (S_{ap} - S_{an})v_{an} + (S_{bp} - S_{bn})v_{bn} + (S_{cp} - S_{cn})v_{cn} \tag{3.20}$$

where I_{dc} is the input dc current v_{an}, v_{bn}, v_{cn} are the three phase capacitor voltages at the output side, S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn}, S_{cn} represent the switching functions for all the six devices. V_{dc} is the input DC voltage to the inverter.

Output currents from the converter can be written as

$$i_a = (S_{ap} - S_{an})I_d \tag{3.21}$$

$$i_b = (S_{bp} - S_{bn})I_d \tag{3.22}$$

$$i_c = (S_{cp} - S_{cn})I_d \tag{3.23}$$

where i_a, i_b, i_c are the three phase current outputs form the inverter.

Voltage across the DC Link is given by

$$V_r = (S_{ap} - S_{an})v_{an} + (S_{bp} - S_{bn})v_{bn} + (S_{cp} - S_{cn})v_{cn}. \quad (3.24)$$

Current flowing into the output filter capacitor can be expressed as

$$C_o p v_{an} = i_a - i_{al} \quad (3.25)$$

$$C_o p v_{bn} = i_b - i_{bl} \quad (3.26)$$

$$C_o p v_{cn} = i_c - i_{cl} \quad (3.27)$$

where i_{al}, i_{bl}, i_{cl} are the three phase output load currents and C_o is the output shunt capacitor. The output voltages with an R-L load is given as

$$v_{an} = r_L i_{al} + L_L p i_{al} \quad (3.28)$$

$$v_{bn} = r_L i_{bl} + L_L p i_{bl} \quad (3.29)$$

$$v_{cn} = r_L i_{cl} + L_L p i_{cl} \quad (3.30)$$

where r_L is the load resistance and L_L is the load side inductor.

3.10 Derivation of the Continuous Modulating Signals

Let i_{as}, i_{bs} , i_{cs} represent three phase currents, which are to be generated.

From the section 3.2 switching function can be approximated as

$$S_{ij} = \frac{1}{A} + M_{ij} \quad \text{i = a, b, c and j = p, n..} \quad (3.31)$$

S_{ij} is the switching function for all the devices in all the phases and M_{ij} is the modulating signal. From Equations (3.21) to (3.23).

$$I_d (S_{ap} - S_{an}) = i_{as} \quad (3.32)$$

$$I_d(S_{bp} - S_{bn}) = i_{bs} \tag{3.33}$$

$$I_d(S_{cp} - S_{cn}) = i_{cs} \tag{3.34}$$

$$S_{ap} + S_{bp} + S_{cp} = 1 \tag{3.35}$$

$$S_{an} + S_{bn} + S_{cn} = 1. \tag{3.36}$$

These Equations (3.32) to (3.36) are underdetermined because there are five linear independent equations with six unknown switching functions. Due to this indeterminacy, there are infinite numbers of solutions, which are obtained by various optimizing performance functions defined in terms of existence function. Equations (3.32 to 3.36) can be expressed as [A] [S] = [Y] where,

$$\text{A}=\begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \end{bmatrix} \text{S} = \begin{bmatrix} S_{ap} \\ S_{an} \\ S_{bp} \\ S_{bn} \\ S_{cp} \\ S_{cn} \end{bmatrix} \quad \text{Y} = \begin{bmatrix} 1 \\ 1 \\ \dfrac{i_a}{I_d} \\ \dfrac{i_b}{I_d} \\ \dfrac{i_c}{I_d} \end{bmatrix}. \tag{3.37}$$

For a set of linear indeterminate equations expressed as A.S = Y, a solution which minimizes the sum of squares of the variable 'S' is obtained using the Moore-Penrose inverse [A.2] .The solution is given as $S = R\, A^T((ARA^T)^{-1})Y$ where

$$R=\begin{bmatrix} K_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & K_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & K_4 & 0 & 0 \\ 0 & 0 & 0 & 0 & K_5 & 0 \\ 0 & 0 & 0 & 0 & 0 & K_6 \end{bmatrix}. \quad (3.38)$$

The solution for the minimization of the sum of the squares of the six-switching functions (equivalently, this is the maximization of the inverter output–input current gain), i.e. $K_1S^2_{ap}+ K_2S^2_{bp} + K_3S^2_{cp}+ K_4 S^2_{an}+ K_5S^2_{bn}+ K_6S^2_{cn}$ subjected to constrains in equation (3.32) to (3.26). Solving the above equations for 'S' we obtain the expressions for the switching functions given in.

$$S_{ap} = \left[\frac{\left(2*\left(\frac{i_a}{I_d}\right)*K_3*K_5*K_2 + \left(\frac{i_a}{I_d}\right)*K_3*K_5*K_1 + \left(\frac{i_b}{I_d}\right)*K_1*K_2*K_5 + \left(\frac{i_c}{I_d}\right)*K_1*K_2*K_3 + 2*K_2*K_3*K_5 + K_1*K_2*K_5 + K_1*K_2*K_3 \right)}{-K_1*K_3*K_5} \right] \quad (3.39)$$

$$S_{an} = \left[-\frac{\left(\left(\frac{i_a}{I_d}\right)*K_4*K_6*K_2 + 2*\left(\frac{i_a}{I_d}\right)*K_4*K_6*K_1 + \left(\frac{i_b}{I_d}\right)*K_1*K_2*K_6 + \left(\frac{i_c}{I_d}\right)*K_1*K_2*K_4 + K_2*K_4*K_6 - 2*K_1*K_4*K_6 - K_1*K_2*K_6 \right)}{-K_1*K_2*K_4} \right] \quad (3.40)$$

$$S_{bp} = \left[\frac{\left(\left(\frac{i_a}{I_d}\right)*K_3*K_4*K_5 + 2*\left(\frac{i_b}{I_d}\right)*K_1*K_5*K_4 + \left(\frac{i_b}{I_d}\right)*K_1*K_5*K_3 + \left(\frac{i_c}{I_d}\right)*K_1*K_3*K_4 + 2*K_1*K_4*K_5 + K_3*K_4*K_5 + K_4*K_1*K_3 \right)}{-K_1*K_3*K_5} \right] \quad (3.41)$$

$$S_{bn} = \left[-\frac{\left(\left(\frac{i_a}{I_d} \right) * K_4 * K_3 * K_6 + \left(\frac{i_b}{I_d} \right) * K_2 * K_6 * K_4 + 2 * \left(\frac{i_b}{I_d} \right) * K_2 * K_6 * K_3 + \left(\frac{i_c}{I_d} \right) * K_2 * K_4 * K_3 + K_2 * K_4 * K_6 - 2 * K_2 * K_3 * K_6 - K_3 * K_4 * K_6 \right)}{-K_3 * K_2 * K_4} \right] \quad (3.42)$$

$$S_{cp} = \left[\frac{\left(\left(\frac{i_a}{I_d} \right) * K_5 * K_3 * K_6 + \left(\frac{i_b}{I_d} \right) * K_1 * K_5 * K_6 + 2 * \left(\frac{i_c}{I_d} \right) * K_1 * K_3 * K_6 + \left(\frac{i_c}{I_d} \right) * K_1 * K_3 * K_5 + 2 * K_1 * K_3 * K_6 + K_6 * K_3 * K_5 + K_6 * K_1 * K_5 \right)}{-K_1 * K_3 * K_5} \right] \quad (3.43)$$

$$S_{cn} = \left[-\frac{\left(\left(\frac{i_a}{I_d} \right) * K_6 * K_4 * K_5 + \left(\frac{i_b}{I_d} \right) * K_2 * K_6 * K_5 + 2 * \left(\frac{i_c}{I_d} \right) * K_2 * K_4 * K_6 + 2 * \left(\frac{i_c}{I_d} \right) * K_2 * K_4 * K_5 + K_2 * K_4 * K_6 - 2 * K_2 * K_4 * K_5 - K_5 * K_4 * K_6 \right)}{-K_5 * K_2 * K_6} \right] \quad (3.44)$$

(when $K_1 = K_2 = K_3 = K_4 = K_5 = K_6 = 1$) .

$$S_{ap} = \frac{1}{3} + \frac{3i_a + i_b + i_c}{2I_d} \tag{3.45}$$

$$S_{an} = \frac{1}{3} - \frac{3i_a + i_b + i_c}{2I_d} \tag{3.46}$$

$$S_{bp} = \frac{1}{3} + \frac{i_a + 3i_b + i_c}{2I_d} \tag{3.47}$$

$$S_{bn} = \frac{1}{3} - \frac{i_a + 3i_b + i_c}{2I_d} \tag{3.48}$$

$$S_{cp} = \frac{1}{3} + \frac{i_a + i_b + 3i_c}{2I_d} \tag{3.49}$$

$$S_{cn} = \frac{1}{3} - \frac{i_a + i_b + 3i_c}{2I_d} \tag{3.50}$$

Using Equation (3.37) to simplify Equations (3.28) to (3.33) have the expressions for the six devices switching functions as

$$S_{ap} = \frac{i_a}{2I_d} + \frac{1}{3} \qquad S_{an} = -\frac{i_a}{2I_d} + \frac{1}{3}$$

$$S_{bp} = \frac{i_b}{2I_d} + \frac{1}{3} \qquad S_{bn} = -\frac{i_b}{2I_d} + \frac{1}{3} \tag{3.51}$$

$$S_{cp} = \frac{i_c}{2I_d} + \frac{1}{3} \qquad S_{cn} = -\frac{i_c}{2I_d} + \frac{1}{3}.$$

From Section 3.4 it is seen that the switching function ‘S’ can be expressed sum of a fundamental component and a time varying term. Hence, from the above Equations (3.36) the expression for the fundamental component can be taken as the modulating signals for the switching devices.

Hence, modulating signals for the six devices are given using Equation (3.26) as

$$M_{ap} = \frac{i_a}{2I_d} \qquad M_{an} = -\frac{i_a}{2I_d}$$

$$M_{bp} = \frac{i_b}{2I_d} \qquad M_{bn} = -\frac{i_b}{2I_d} \tag{3.52}$$

$$M_{cp} = \frac{i_c}{2I_d} \qquad M_{cn} = -\frac{i_c}{2I_d}.$$

CHAPTER 4

PWM SCHEMES FOR CURRENT SOURCE INVERTER USING VOLTAGE SOURCE INVERTER MODULATION SCHEME

4.1 Introduction

This chapter deals with one of the modulation strategies for the Current Source inverter using the states of a voltage source inverter. VSI has a large d_v/d_t transitions on the phase leg output voltages; this results in problems such as increased motor losses, acoustics noise in load, insulation degradation due to voltage surges and electromagnetic interference effects. In voltage source inverter PWM scheme, by adding zero sequence voltages to the existing modulating signals in high modulation region, the switching loss, voltage linearity, and over modulation performance of the inverter is optimized [B.20]. In a similar way, by adopting these modulation strategies into a CSI, the advantages in the modulation schemes in VSI can be extended to a CSI. Different methods of mapping VSI switching methodology to the current source inverter switching have been suggested [B.21].

1. Online carrier-based PWM Scheme (SPWM).
2. Digital on-line space vector–based technique (SVPWM).

The following section will explore the utilization of the discontinuous PWM schemes as applied in VSI into a CSI. This will also cover the gating requirements to avoid shorting of adjacent legs, and the logic circuit development. The operation is

studied with a current source inverter feeding a R-L load. The performance is examined through both simulation and experimental results.

4.2 Online Carrier-Based PWM Scheme

Online Pulse Width Modulation (PWM) pattern generators for current-source rectifiers and inverters, offer a number of control advantages over off-line optimized patterns [B.9, B.10, B.22]. The online carrier-based PWM scheme [B.15-B.17, B.22] is the easiest to implement using the state concepts developed for CSI and VSI. It is clear that any CSI can be controlled by any VSI modulation strategy if the active states created by the modulator are mapped to the stationary vectors and to the switching combinations associated with these vectors. In developing this scheme, it is necessary to determine how the CSI null state should be related to the modulator state outputs.

In case of the VSI, with every sine triangle comparison there is an implicit transition of the null states and thus it is not a separate part of the modulation process. Whereas, in the case of CSI, there is no direct mapping of the sine triangle output to the corresponding null states of a CSI, hence the null states have to be defined explicitly.

This section deals with the development of the gating schemes for the CSI. The main objective of the scheme is to attain a modulation scheme for the CSI; i.e., the switching pattern has to satisfy the conditions given by Equations (3.18) and (3.19) in Chapter 3. In this scheme, both continuous and an already developed Generalized Discontinuous Pulse Width Modulation (GDPWM) scheme for VSI given in [B.21] is

used to synthesize three-phase reference currents. The voltage terms are replaced with the current terms in the generalized equation developed for VSI [B.21]. The discontinuous modulating signals are compared with a high frequency triangle. But the output of the modulator will not satisfy constrains laid out for operation of a CSI. So it is passed through an algorithm, which maps voltage source PWM switching, to a current source PWM and removes undesirable states.

4.2.1 Carrier-Based Modulation Scheme for Three Phase VSI

In complying with Kirchhoff's voltage (KVL) and current (KCL) law, the VSI is restricted in the sense that both the devices in a same leg cannot be turned ON at the same time, as it would result in shorting of the DC link capacitor. But it does allow the shorting of the adjacent legs. Thus the nature of the two switches in the same leg is complimentary. In accordance to Figure 4.1,

$$S_{11} + S_{12} = 1 \tag{4.1}$$

$$S_{21} + S_{22} = 1 \tag{4.2}$$

$$S_{31} + S_{32} = 1. \tag{4.3}$$

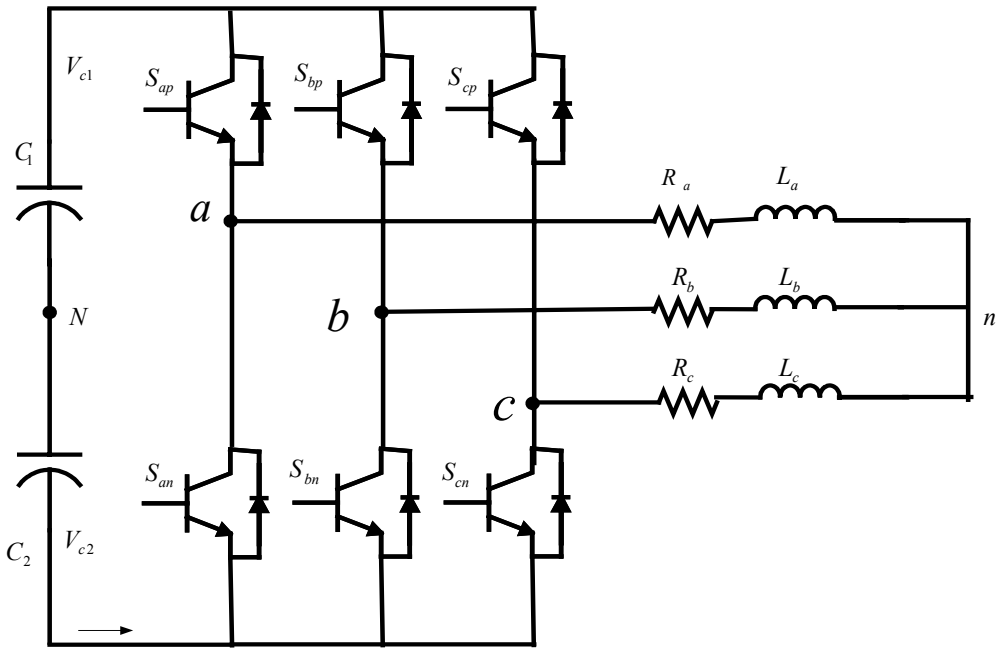


Figure 4.1 Schematic of a three-phase voltage source inverter

Table 4.1 Switching states in a three phase VSI

	State	S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}
A	V_1	0	0	1	1	1	0
C	V_2	0	1	0	1	0	1
T	V_3	0	1	1	1	0	0
I	V_4	1	0	0	0	1	1
V	V_5	1	0	1	0	1	0
E	V_6	1	1	0	0	0	1
N	V_0	1	1	1	0	0	0
U							
L	V_7	0	0	0	1	1	1
L							

Table 4.1 gives the possible switching states for a VSI. The states from V_1 to V_6 are the termed as active states and V_0 and V_7 are as null states. From Table 4.1 it is seen that a VSI has six active states and two null states making a total of eight possible states. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the switching functions and input DC voltage V_{dc} is given as

$$\frac{V_{dc}}{2}(S_{ap} - S_{an}) = v_{an} + v_{no} \tag{4.4}$$

$$\frac{V_{dc}}{2}(S_{bp} - S_{bn}) = v_{bn} + v_{no} \tag{4.5}$$

$$\frac{V_{dc}}{2}(S_{cp} - S_{cn}) = v_{cn} + v_{no} \tag{4.6}$$

where v_{an}, v_{bn}, v_{cn} are the phase voltages of the load while the voltage of the load neutral to inverter reference is v_{no}.

Adding Equation (4.4) to (4.6) together gives Equation (4.7)

$$\frac{V_{dc}}{2}(S_{ap} + S_{bp} + S_{cp} - S_{an} - S_{bn} - S_{cn}) = v_{an} + v_{bn} + v_{cn} + 3v_{no}. \tag{4.7}$$

Since voltages are balanced $v_{an} + v_{bn} + v_{cn} = 0$ and making use of the conditions Equations (4.1) to (4.3), Equations (4.4) to (4.6) becomes

$$\frac{V_{dc}}{2}(2S_{ap} - S_{bp} - S_{cp}) = v_{an} \tag{4.8}$$

$$\frac{V_{dc}}{2}(-S_{ap} + 2S_{bp} - S_{cp}) = v_{bn} \tag{4.9}$$

$$\frac{V_{dc}}{2}(-S_{ap} - S_{bp} + 2S_{cp}) = v_{cn}. \tag{4.10}$$

4.2.1.1 Expression for the continuous modulating signals.

The switching functions of the switching devices in the converter can be approximated as a sum of a fundamental component and a DC component using Fourier series expansion discussed in Section 3.4, hence the approximated switching functions can be given as

$$S_{ap} = \frac{1}{2}[1 + M_{ap}] \qquad S_{bp} = \frac{1}{2}[1 + M_{bp}] \qquad S_{cp} = \frac{1}{2}[1 + M_{cp}] \tag{4.11}$$

where M_{ap}, M_{bp}, M_{cp} represent the modulating signals for the switching devices. From Equations (4.4) to (4.6) modulating signals can be expressed as

$$M_{ap} = \frac{v_{an}}{V_d / 2} + \frac{v_{no}}{V_d / 2} \tag{4.12}$$

$$M_{bp} = \frac{v_{bn}}{V_d / 2} + \frac{v_{no}}{V_d / 2} \tag{4.13}$$

$$M_{cp} = \frac{v_{cn}}{V_d / 2} + \frac{v_{no}}{V_d / 2}. \tag{4.14}$$

4.2.1.2 Generalized discontinuous PWM.

Equations (4.12) to (4.14) give the expressions for the continuous modulation scheme of a VSI, an alternative carrier based discontinuous modulation scheme is obtained by using the space vector methodology to determine the expression for the discontinuous modulation scheme.

Table 4.2 Switching modes of the three-phase voltage source inverter and corresponding stationary reference frame q-d-o voltages.

Mode	S_{ap}	S_{bp}	S_{cp}	V_{qs}	V_{ds}	V_{os}
1	0	0	0	0	0	$-V_{dc}/2$
2	0	0	1	$-V_{dc}/\sqrt{3}$	$V_{dc}/\sqrt{3}$	$-V_{dc}/6$
3	0	1	0	$-V_{dc}/3$	$-V_{dc}/\sqrt{3}$	$-V_{dc}/6$
4	0	1	1	$-2V_{dc}/3$	0	$V_{dc}/6$
5	1	0	0	$2V_{dc}/3$	0	$-V_{dc}/6$
6	1	0	1	$V_{dc}/3$	$-V_{dc}/\sqrt{3}$	$V_{dc}/6$
7	1	1	0	$V_{dc}/3$	$V_{dc}/\sqrt{3}$	$V_{dc}/6$
8	1	1	1	0	0	$V_{dc}/2$

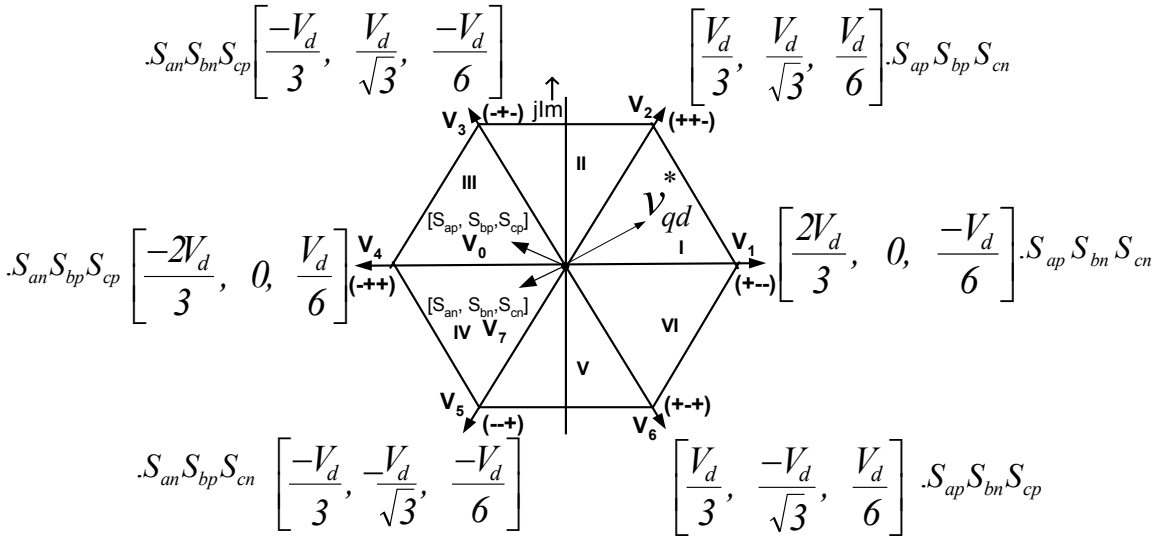


Figure 4.2 Projection of the available states of a VSI on the q-d plane.

The eight possible switching states for the voltage source inverter along with the q-d transformation in stationary reference frame of the three phase voltages are shown in Table 4.2. The voltages as given in Table 4.2 can be graphically represented as a hexagon whose sides are the switching states. In Figure 4.2, V_1 to V_7 correspond to the six active states and V_0, V_8 corresponds to null states. The reference zero sequence voltage v_{no} is approximated by time averaging of the zero sequence voltages of two active modes and a null mode. v_{no} over switching period t_s is given as

$$<V_{no}> = V_{oa}\, t_a + V_{ob}\, t_b + V_{oo}\, t_o\, V_{o7}\, t_7. \tag{4.15}$$

It should be noted that t_c is portioned into dwell times for the two null voltage vector - $t_c\alpha$ for V_o and $t_c\,(1-\alpha)$ for V_7. Where V_{oa}, V_{bo}, V_{oo}, and V_{o7} are the zero sequence voltages in both the two active and two null states, respectively, t_a, t_b, and t_7 represents the normalized times with respect to the inverter sampling frequency. Table 4.3 gives the expression for the averaged neutral voltage $<v_{no}>$ for the six sectors of the space vector in terms of t_a and t_b.

By expressing the values of t_a and t_b in terms of the reference voltages generalized expression for average zero sequence voltage can be given as

Table 4.3 Average zero sequence voltage for the sectors.

Sectors	I, III, IV	II, IV, VI
$<v_{no}>$	$< v_{no} > = \frac{V_{dc}}{6}(t_b - t_a) + \frac{t_c V_{dc}}{6}(1-2\alpha)$	$< v_{no} > = \frac{V_{dc}}{6}(t_a - t_b) + \frac{t_c V_{dc}}{6}(1-2\alpha)$

$$< v_{no} > = \frac{V_{dc}}{2}[V_{\max}(1-2\alpha) - \alpha V_{\min}] \tag{4.16}$$

where V_{max} and V_{min} are the maximum and minimum values of the reference phase voltages in each sector. Hence, by substituting Equation (4.16) into Equations (4.12) to (4.14) the expression for the modulating signals can be given as

$$M_{ap} = \frac{v_{an}}{V_{dc}/2} + (1-2\alpha) + \frac{[V_{\max}(1-2\alpha) - \alpha V_{\min}]}{V_{dc}/2} \tag{4.17}$$

$$M_{bp} = \frac{v_{bn}}{V_{dc}/2} + (1-2\alpha) + \frac{[V_{\max}(1-2\alpha) - \alpha V_{\min}]}{V_{dc}/2} \tag{4.18}$$

$$M_{cp} = \frac{v_{cn}}{V_{dc}/2} + (1-2\alpha) + \frac{[V_{\max}(1-2\alpha) - \alpha V_{\min}]}{V_{dc}/2}. \tag{4.19}$$

Equations (4.17) to (4.19) can be expressed in a generalized form as

$$M_{ip} = \frac{v_{in}}{V_{dc}/2} + (1-2\sigma) + \frac{[V_{\max}(1-2\sigma) - \sigma V_{\min}]}{V_{dc}/2} \tag{4.20}$$

where $\sigma = 0.5\,[1 + \mathrm{Sgn}\,(\mathrm{Cos}\,(3\omega t + \delta))]$, and i = a, b, c.

In Equation (4.20), v_{in} is the three phase voltages, ω is the angular frequency of the reference voltage and δ is the modulation angle.

4.2.2 Carrier-Based Modulation Scheme for Three Phase CSI

In complying with Kirchhoff's voltage (KVL) and current (KCL) law, for a CSI it is mandatory that only one device in the top and in the bottom is turned ON at a time, else the output capacitors will be short circuited. It has to satisfy constrains mentioned in Chapter 3 Equations (3.19) and (3.20).

Table 4.4 gives the possible switching states for a current source inverter. The states [$I_1 \ldots I_6$] are termed as active states and I_7, I_8, I_9 as null states. Hence, from the above table, it can be stated that there are six active states and three null states making a total of nine states for the current source inverter. The active states in the CSI are helpful in synthesizing the reference currents and the three null states are like freewheeling states used to remove the energy stored in the input side inductor.

Table 4.5 gives all the states of the current source converter and the magnitude of the current in each state, which is given by transforming the current in each state to the stationary q-d-o reference frame. Equation (4.20) gives the expression for the modulating signals adopted for the VSI. In this expression the voltage quantities have been replaced with the current quantities so as to synthesize reference currents.

Table 4.4 Switching States in a 3 Phase CSI

	State	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
ACTIVE	I_1	1	1	0	0	0	0
	I_2	0	1	1	0	0	0
	I_3	0	0	1	1	0	0
	I_4	0	0	0	1	1	0
	I_5	0	0	0	0	1	1
	I_6	1	0	0	0	0	1
NULL	I_7	1	0	0	1	0	0
	I_8	0	1	0	0	1	0
	I_9	0	0	1	0	0	1

Table 4.5 Switching modes of the three-phase current source inverter and corresponding stationary reference frame q-d-o currents.

ON Device	**ON Device**	$\mathbf{i_{as}}$	$\mathbf{i_{bs}}$	$\mathbf{i_{cs}}$	$\mathbf{I_{qq}}$	$\mathbf{\sqrt{3}\ I_{dd}}$
S_{ap}	S_{bn}	I_d	$-I_d$	0	I_d	I_d
S_{ap}	S_{cn}	I_d	0	$-I_d$	I_d	$-I_d$
S_{bp}	S_{an}	$-I_d$	I_d	0	$-I_d$	$-I_d$
S_{bp}	S_{cn}	0	I_d	$-I_d$	0	$-2I_d$
S_{cp}	S_{an}	$-I_d$	0	I_d	$-I_d$	I_d
S_{cp}	S_{bp}	0	$-I_d$	I_d	0	$2I_d$
S_{ap}	S_{an}	0	0	0	0	0
S_{bp}	S_{bn}	0	0	0	0	0
S_{cp}	S_{cn}	0	0	0	0	0

$$M_{ip} = \frac{2i_{ip}}{I_{dc}} + (1-2\sigma) + \frac{2.[I_{\max}(1-2\sigma) - \sigma I_{\min}]}{I_{dc}} \qquad (4.21)$$

where $\sigma = 0.5\ [1 + \mathrm{Sgn}\ (\mathrm{Cos}\ 3(\omega t + \delta))]$.

In Equation (4.21) i_{in} are the reference phase currents where i = a, b, c . This GDPWM clamps the devices for some period of the fundamental frequency to either positive or negative rail in the process of which the modulator performance may be improved. By varying the angle δ, various types of carrier–based discontinuous PWM modulators [GDPWM] are obtained. In Equation (4.21), M_{ip} is the three phase modulating signal and

I_d is the input dc current, and I_{max} & I_{min} are the maximum and minimum values of the reference currents. These modulating signals are compared with the high frequency triangular carrier wave. The switching pattern attained is passed through the algorithm developed to transform the states of the VSI into null and active states of the CSI. From the Figures 4.2 and 4.7, it is seen that a difference of 30^o in space vectors of the two inverters. The currents synthesized using the mapping technique are not exactly same as the commanded currents. The output current and the commanded current have phase difference of 30^0 between them and $\sqrt{3}$ times the magnitude. In order to generate three phase commanded currents the following modifications is done for the modulating signals.

$$i_{ap} = \frac{i_{as} - i_{bs}}{\sqrt{3}} \qquad i_{bp} = \frac{i_{bs} - i_{cs}}{\sqrt{3}} \qquad i_{cp} = \frac{i_{cs} - i_{as}}{\sqrt{3}} \tag{4.22}$$

where I_{max} = Maximum (i_{ap}, i_{bp}, i_{cp}), I_{min} = Minimum (i_{ap}, i_{bp}, i_{cp}).

4.3 Algorithm For Mapping VSI States to CSI States

From Table 4.1 and 4.2 the mapping procedure is done as follows:

Consider the output state, which is desired from the available input states. By combining the VSI [V_1 ....V_8] states in a particular way the desired CSI [I_1…I_9] states can be obtained, thus:

$h_1 = V_1 + V_3$

By taking the complement of both sides,

$$\overline{h_1} = \overline{V_1 + V_3}$$

$$\overline{h_1} = \overline{S_{cp} S_{an} S_{bn} + S_{bp} S_{cp} S_{an}} \tag{4.23}$$

$$\overline{h_1} = \overline{S_{cp} S_{an} (S_{bn} + S_{bp})}$$

Using the identity

$\overline{A.B} = \overline{A} + \overline{B}$ and $\overline{A + B} = A.B$.

$$\overline{h_1} = \overline{S_{cp} S_{an}} + \overline{(S_{bn} + S_{bp})} = \overline{S_{cp} S_{an}} + S_{bn} S_{bp} = \overline{\bar{S}_{cn} . \overline{S}_{ap}} + S_{bn} S_{bp} \tag{4.24}$$

Using the property $\overline{\overline{A}.\overline{B}} = A.B$

$$h_1 = S_{cn} S_{ap} + S_{bn} S_{bp} . \tag{4.25}$$

Here, the first term corresponds to the active state while the second term corresponds to a null state in CSI. The remaining CSI states are listed as

$$h_2 = S_{cn} S_{bp} + S_{an} S_{ap} \tag{4.26}$$

$$h_3 = S_{bp} S_{an} + S_{cn} S_{cp} \tag{4.27}$$

$$h_4 = S_{cp} S_{an} + S_{bn} S_{bp} \tag{4.28}$$

$$h_5 = S_{cp} S_{bn} + S_{an} S_{ap} \tag{4.29}$$

$$h_6 = S_{bn} S_{ap} + S_{cn} S_{cp} . \tag{4.30}$$

It is evident from these expressions that any VSI state combination results in a combination of a CSI active state and a null state. The truth tables for the expressions are summarized in Table 4.6.

Table 4.6 Derivation of the desired states from the available states

						h_1	h_2	h_3	h_4	h_5	h_6
S_{ap}	S_{cn}	S_{bp}	S_{an}	S_{cp}	S_{bn}	$S_{ap}S_{cn}+$ $S_{bp}S_{bn}$	$S_{bp}S_{cn}+$ $S_{ap}S_{an}$	$S_{bp}S_{an}+$ $S_{cp}S_{cn}$	$S_{cp}S_{an}+$ $S_{bp}S_{bn}$	$S_{cp}S_{bn}+$ $S_{ap}S_{an}$	$S_{ap}S_{bn}+$ $S_{cp}S_{cn}$
0	1	0	1	0	1	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	1	1	0
0	1	1	1	0	0	0	1	1	0	0	0
0	0	1	1	1	0	0	0	1	1	0	0
1	1	0	0	0	1	1	0	0	0	0	1
1	0	0	0	1	1	0	0	0	0	1	1
1	1	1	0	0	0	1	1	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0

From Table 4.6, it is seen that there is no state in which two top or bottom devices are turned ON at the same time; i.e., only one device in the top and one device in bottom are switched ON at the same time. The null states of the VSI are not mapped into the null states of CSI; using the above algorithm because the product of two states is always zero.

4.3.1 Shorting Pulse Distributor

There is a necessity to introduce the null states in conjunction with the active states in the CSI. Thus, additional conditions of minimizing switching losses by reducing the number of switch transitions and maintaining balanced switch utilization are imposed. This should also ensure the symmetry in the output switched currents in order to have minimum harmonic distortion as in [B.16]. To satisfy the above requirements, a logic circuit is developed to detect the condition when the null state has to be applied. This logic circuit detects the null state whenever all the devices in the top and /or bottom are switched OFF. Once the condition for null state is detected, one of the three legs of the CSI has to be shorted. Gating the devices in the same leg by a common signal, which will be termed as a shorting pulse, is used to distribute the null states. The VSI has two null states, which have to be equalized into three null states of the CSI for one period of time. Null states in a CSI, means shorting one leg of any phase. This shorting of the legs has to be equally distributed in order to synthesize balanced reference currents. This distribution of the null states is done using the absolute maximum of the line-to-line of the three reference signals. If i_{ap} is maximum, leg 'A' is shorted, i_{bp} is maximum, leg B is shorted, i_{cp} is maximum, leg C is shorted.

From Table 4.7, it can be seen that one cycle of operation is divided into six sectors. And observed that the absolute maximum of each phase appears twice with an angle of 60^{o}.

Table 4.7. Absolute maximum of the reference currents in each sector

Sector	I	II	III	IV	V	VI
Max Current	i_{ap}	i_{bp}	i_{bp}	i_{cp}	i_{cp}	i_{ap}

Figure 4.3 shows the three phase line-line currents and absolute maximums of line-line currents and three phase distributing signals. It can be seen that when the absolute of i_{ab} is maximum then S_{pa} will be high, when i_{bc} is maximum then S_{pb} will be high, when i_{ca} is maximum then S_{pc} will be high. These pulses are used to distribute the null states equally.

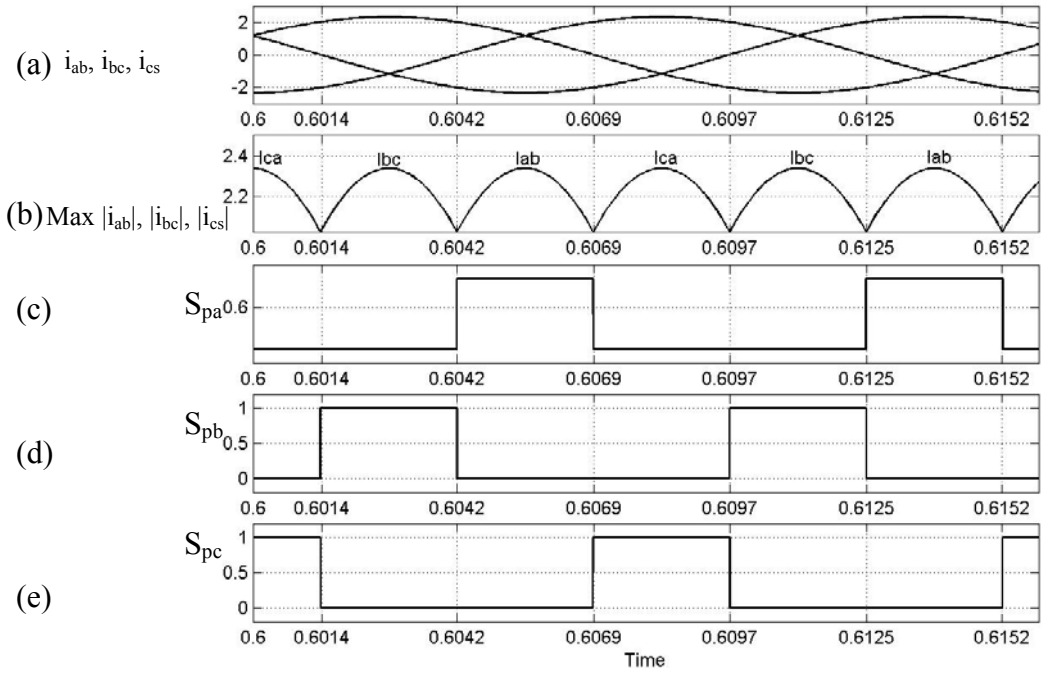


Figure 4.3 Distributing signals (a)Three phase Line-Line to currents, (b) absolute maximums of line-line currents, (c) phase 'a' distributing signal $S_{pa,}$ (d) phase 'b' distributing signal $S_{pb,}$ (e) phase 'c' distributing signal S_{pc}

4.3.2 Practical Implementation of the Logic Scheme

The PWM switching signals obtained from the output of the DSP are recombined to generate Table 4.5. Thus V_1 through V_6 are the outputs of the logic gates corresponding to the VSI states. These states are recombined using Equations 4.3 through 4.10 to obtain the states listed in Table 4.4. The third condition is for the detection of null states and their distribution logic. The null state logic detector activates $S_d = 1$ whenever the sum of all the devices in the top and bottom is found to be zero. This S_d in combination with the distribution logic generates shorting pulses of the corresponding leg. The calculation of the absolute maximum of the reference signals is done internally in the DSP to generate the distribution signals $S_{pa,}$ $S_{pb,}$ $S_{pc...}$Figure 4.4 shows the circuit diagram for the implementation of the logic. The switching pattern is passed through combinations of AND, OR gates and using the shorting pulse distributor S_d the phase legs are shorted in order to satisfy the constraints laid in Chapter 3. The Final switching pattern [S_{c1}...S_6] is given to the devices

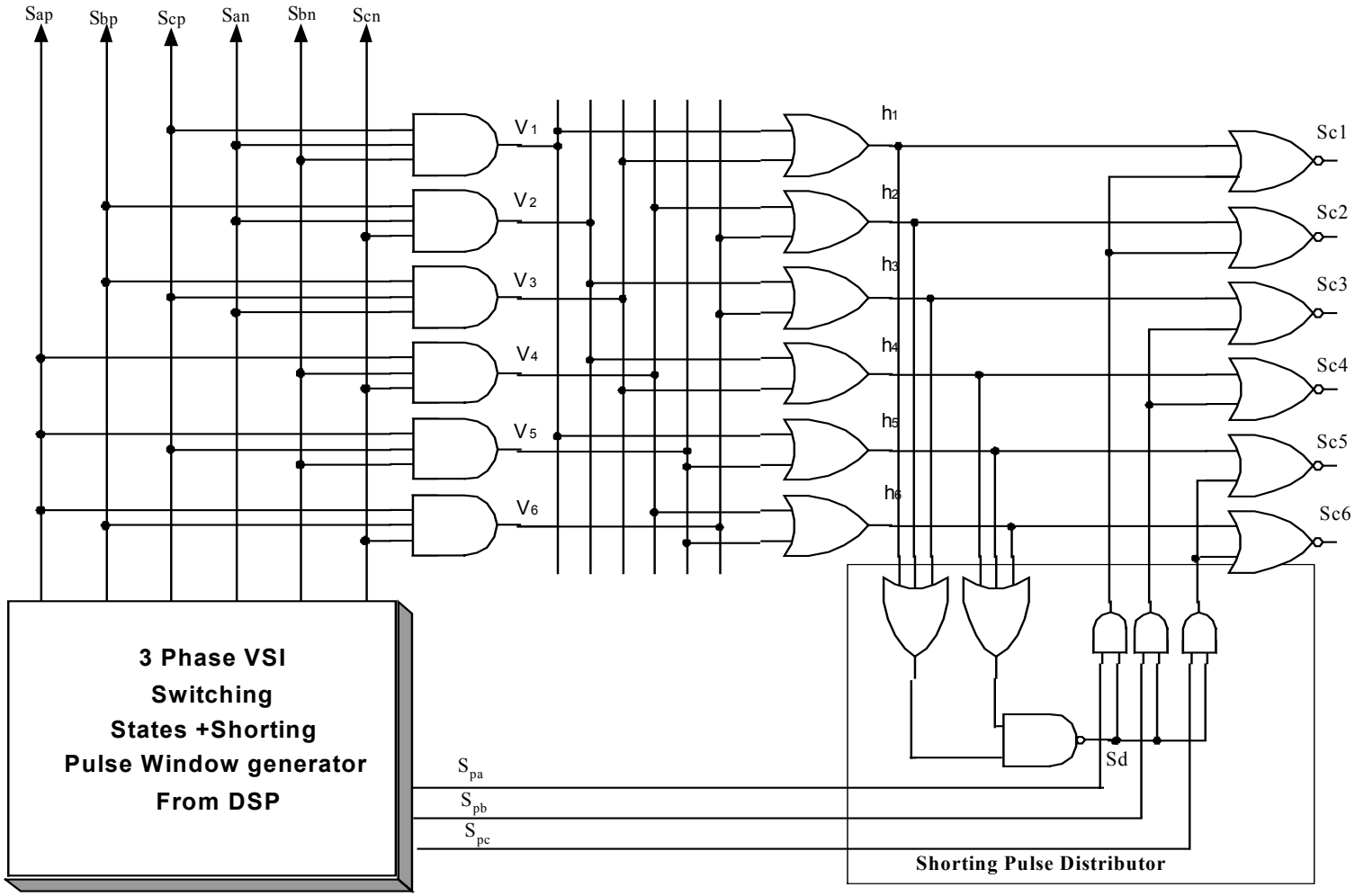


Figure 4.4 Practical scheme for implementing the VSI to CSI mapping

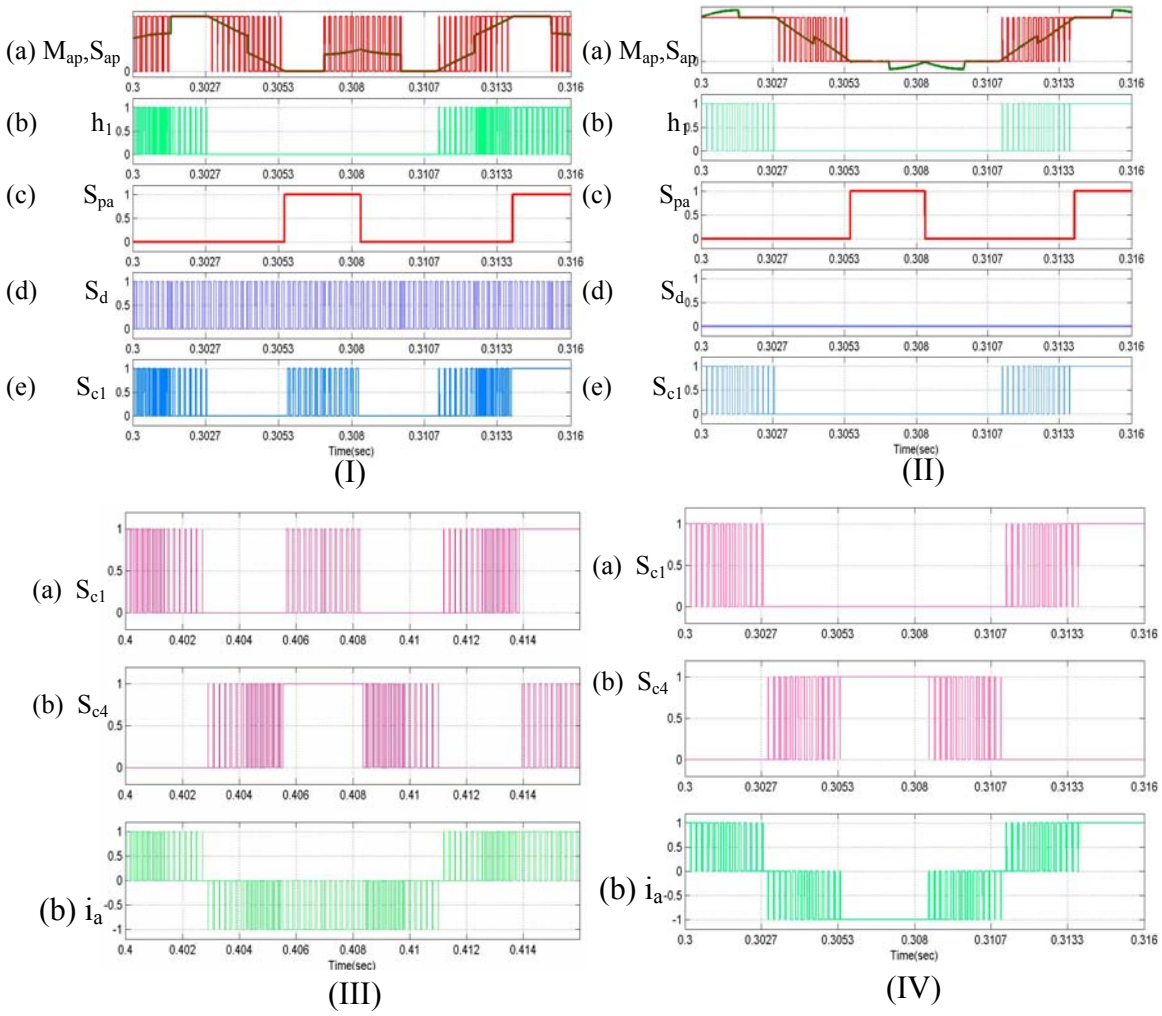


Figure 4.5 Simulation results showing sequence of operations in linear and overmodulation region.

Figure 4.5 shows the sequence of stages in which the switching pattern changes form its initial state to final state when they are passed through the algorithm in linear and overmodulation region. Figure 4.5 (I) and (II) (a) gives the phase 'a' modulating signal and the actual switching pattern, (b) gives the switching function h_1, (c) shows the pulse distributor S_{pa} which corresponds to the maximum of I_{ab} among absolute max (i_{ab}, i_c, i_{ca}), (d) shows the occurrence of the null states during the VSI operation, (e) shows the final

gating switching pattern for phase ‘a’ top device. Figures (III) and (IV) (a) and (b) gives the final switching pattern for the phase a top device and bottom devices, (c) phase ‘a’ generated current waveform. In ovemodulation region it is seen that there are no null states generating in VSI and so no null states are mapped into CSI.

4.4 Space Vector Approach

This scheme is different from that of a sine triangle method of mapping. The difference between space vector approach and the sine triangle PWM approach are:

- For space vector approach, the active state periods are calculated directly and then mapped to the required switch combinations. For sine triangle PWM, the duration of the active states are not exactly calculated and their switching combination is also implicit.
- In space vector approach, the ordering and placing of active and null states are done explicitly. But, in the case of the sine triangle PWM, the active state and null states are ordered implicitly.

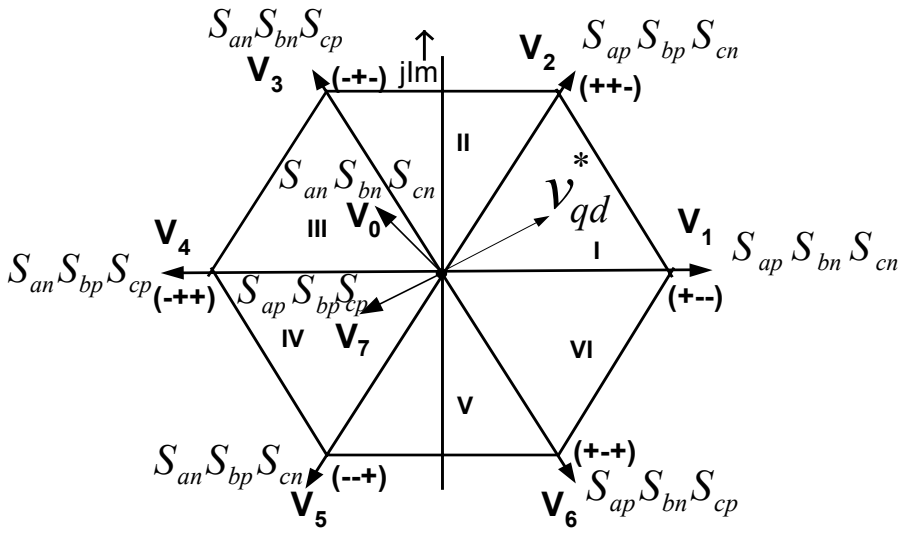


Figure 4.6 Space Vector diagram of the VSI showing all the six active sates.

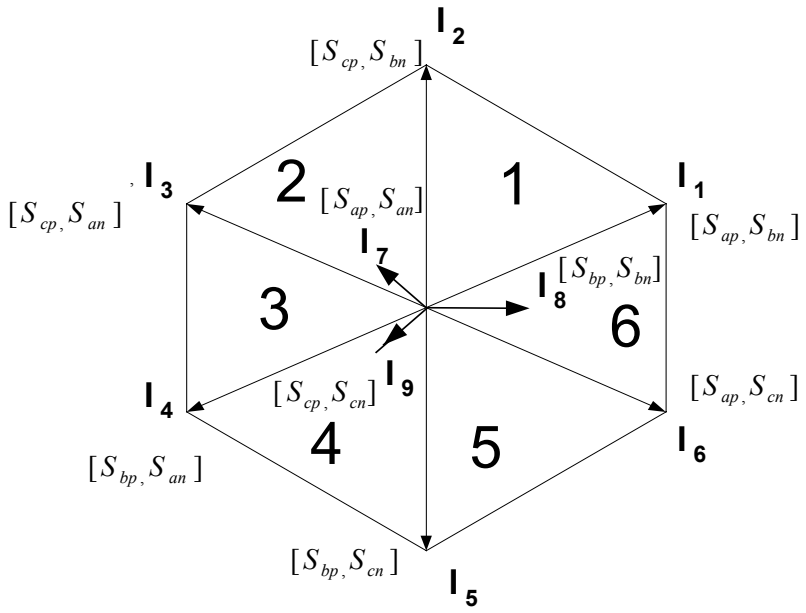


Figure 4.7 Space Vector diagram for a CSI

Figure 4.7 show the space vector diagram for a CSI [I_1…I_6] are the six active states and I_7, I_8, I_9 are the three null states. The main objective is to map the active states in Figure 4.6 to the active states in Figure 4.7 and also to distribute all the three null states of the CSI such that the balancing of the states is attained. From Figures 4.6 and 4.7, it

can be stated that there is a ONE –ONE correspondence between the states of the VSI to that of the active states of the CSI. So we can directly say the mapping of the states as

$$V_1 \text{ (State 1 of VSI)} \leftrightarrow I_1 \text{ (State 1 of CSI)}$$

$$V_2 \text{ (state 2 of VSI)} \leftrightarrow I_2 \text{ (State 2 of CSI)}$$

$$V_3 \text{ (state 3 of VSI)} \leftrightarrow I_3 \text{ (state 3 of CSI)}$$

$$V_4 \text{ (state 4 of VSI)} \leftrightarrow I_4 \text{ (state 4 of CSI)}$$

$$V_5 \text{ (state 5 of VSI)} \leftrightarrow I_5 \text{ (state 5 of CSI)}$$

$$V_6 \text{ (state 6 of VSI)} \leftrightarrow I_6 \text{ (state 6 of CSI).}$$

Hence by the above relation it can be stated that using the modulator of a VSI the CSI gating signals can be generated. The time durations calculated to turn ON the states of VSI can be used to turn the ON the corresponding states in the CSI. The times t_a and t_b calculated in VSI to synthesis the reference voltage can be used to synthesize the reference currents for a CSI using the above state mapping technique. It follows the following expression for generating desired currents

$$I^*_{qd} . t_{cycle} = I_i . t_a + I_b . t_{i+1} + I_o . t_o \qquad (4.11)$$

where I_i and I_{i+1} are the two adjacent states in which the reference current vector resides, and I_o is one of the null state. In a sextant the two adjacent active vectors are turned ON for times t_a and t_b and in the remaining time t_o one of the null state has to be selected. In selection of the null states some additional criteria must be used to determine which null states have to be used in different sectors. The most common criteria for selection of null states is to minimize the number of switch transitions per switching cycle.

4.4.1 Selection of the Null States

Consider Sector I.

In this sector, let us consider I_1 as the initial state and I_2 as the final state. In between these states there can be any null state (I_7, I_8, I_9). But selection of null state depends on number of switching transitions. Table 4.8 shows the number of switching transitions for different selections of null states.

From Table 4.8, it can be seen that if I_7 or I_9 are selected as null states in sector I then the number of switching transitions would be three. But if I_8 is selected as the null state, the number of switching transitions is two. Hence, by choosing the proper null state minimization of number of transitions can be decreased from three to two. This procedure has to be followed in all the sectors to attain minimum switching transition and since three null states are divided six sectors of the hexagon from table 4.9 it is seen that the balance distribution of the null states is done.

Table 4.8 Selection of null state for minimum transition

Initial State	Possible zero vector	Final state	Number of switching Transitions
I_1 (S_{ap}, S_{bn})	I_7 (S_{ap},S_{an})	I_2 (S_{cp}, S_{bn})	3
I_1 (S_{ap}, S_{bn})	I_8 (S_{bp},S_{bn})	I_2 (S_{cp}, S_{bn})	2
I_1 (S_{ap}, S_{bn})	I_9 (S_{cp}, S_{cn})	I_2 (S_{cp}, S_{bn})	3

Table 4.9 Selection of null states for minimum switching transition.

Sector	Initial state	Final State	Null state
1	I_1 (S_{ap},S_{bn})	I_2 (S_{cp},S_{bn})	I_8 (S_{bp},S_{bn})
2	I_2 (S_{cp},S_{bn})	I_3 (S_{cp},S_{an})	I_9 (S_{cp},S_{cn})
3	I_3 (S_{cp},S_{an})	I_4 (S_{bp},S_{an})	I_7 (S_{ap},S_{an})
4	I_4 (S_{bp},S_{an})	I_5 (S_{bp},S_{cn})	I_8 (S_{bp},S_{bn})
5	I_5 (S_{bp},S_{cn})	I_6 (S_{ap},S_{cn})	I_9 (S_{cp},S_{cn})
6	I_6 (S_{ap},S_{cn})	I_1 (S_{ap},S_{bn})	I_7 (S_{ap},S_{an})

Table 4.9 gives the null states in each sector to be selected for minimum switching transition for one period. From the space vector Figures 4.6 and 4.7 it can be seen that the angle between the active space vectors are 60^o for both the VSI and CSI, but the active space vectors of the CSI lead the VSI space vectors by 30^o. Hence the direct mapping of the states of a VSI to those of a CSI produces a 30^o lead in the output current compared to the reference currents. Hence a 30^o of lagging phase shift is introduced to compensate for the effects of space vector mapping which produces a net in-phase output current for the CSI compared to the input reference signals.

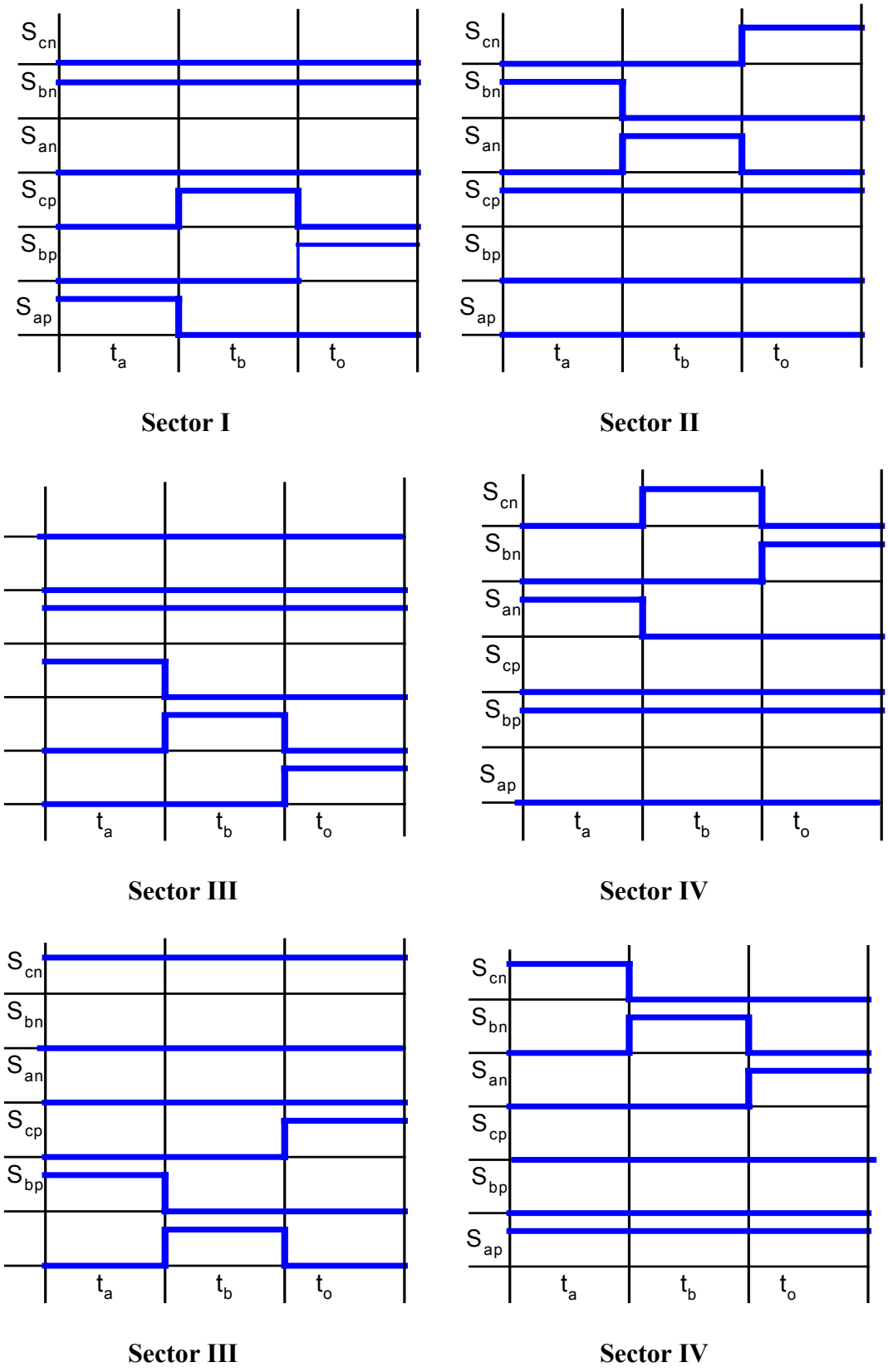


Figure 4.8 Timing sequences of the switches in al the six sectors

Figure 4.8 shows the timing diagram for six devices in six sectors following the sequence given in Table 4.9 active states spend time t_a and t_b and the null states spends time t_o.

4.5 Effect of Null States

One other issue with these mapping schemes is that, in transition of the reference vector from one sector of the space-vector sextant to the next, as shown in Figure 4.7. Depending upon the switch just prior to the sextant transition, the inverter may have to switch in a non-optimal way, which involves two simultaneous switch transitions, and this can cause undesirable transients in the current [B.17].

For example, if the state I_7 is chosen as null state in sector II. The switch transition takes from states I_7 to I_2 if there is any delay with the switch transitions, the inverter will switch from state I_7 to I_3 while approaching I_2. Because at state I_7 devices S_{ap} and S_{an} are turned ON, to change to I_2 state devices S_{cp}, and S_{bn} should be turned ON. So in between these transition their can be an occurrence of an adjacent state I_3 in which S_{cp} and S_{an} are turned ON. This improper transition into a different state instead of an actual target causes a glitch in the waveform of the current as shown in Figure 4.9.

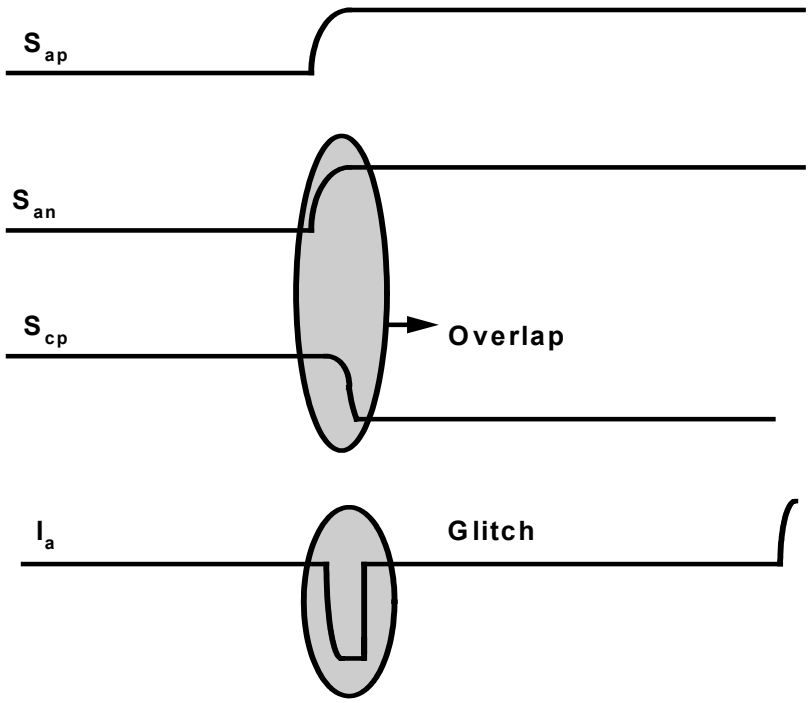


Figure 4.9 Switching transition from one state to other state and the glitch in the current waveform

From Figure 4.9 shows the switching transition form state V_7 to V_2 and also a transition into an in-between state V_3 that causes a glitch in the current. This glitch can be avoided by introducing an extra null state in between V_7 and V_2, which will results in an extra switch transition. Or, by introducing a null state V_8 or V_9 instead of V_7 in the above case glitch can be avoided. Since in the space vector the selection of null states is implicit. The above selection of different null state can be achieved by space vector implementation. This is one of the drawbacks in the sine triangle PWM technique

4.6 Simulation and Experimental Results

Simulation of a current source inverter is performed using the model equation described in Section 3.8 and the scheme of mapping voltage source inverter states to current source inverter states is used to modulate the current source inverter. Switching frequency of the carrier triangle is taken as 5kHz, with the input DC voltage of 100V, input side inductor of 100mH, output side load inductor as 12mH, output side filter capacitor 60μF, and three-phase resistive load of 30Ω.

An experimental setup is built using the TMS320LF2407A floating point DSP. The PWM ports of the DSP are used to generate all the switching patterns [S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn}, S_{cn}] and the distributing signals are generated using the DAC 's of the DSP. The logic explained in Section 4.3 is implemented using the simple AND, OR gates. Output switching pattern from the logic circuit will satisfy the conditions laid for the CSI. A small amount of overlap time is provided to the switching signals through an external hardware circuit to avoid open circuit of the supply current. Section 4.6.1 shows experimental and simulation results for a continuous modulation scheme in linear and over-modulation region. Section 4.6.2 gives the experimental and simulation results for GDPWM modulation with $\beta = 0$, 0.5, and 1 in both the regions of operation. Section 4.6.3 gives the experimental and simulation results for GDPWM with $\delta = 0$, -30, -60 for both M = 0.85 and 1.25. The objective was to observe the performance of various modulating schemes on the inverter output voltages and currents. Hence the FFT of the filtered output voltage and current was done to see the difference in the various PWM schemes.

4.6.1 Continuous Modulation in Linear Region

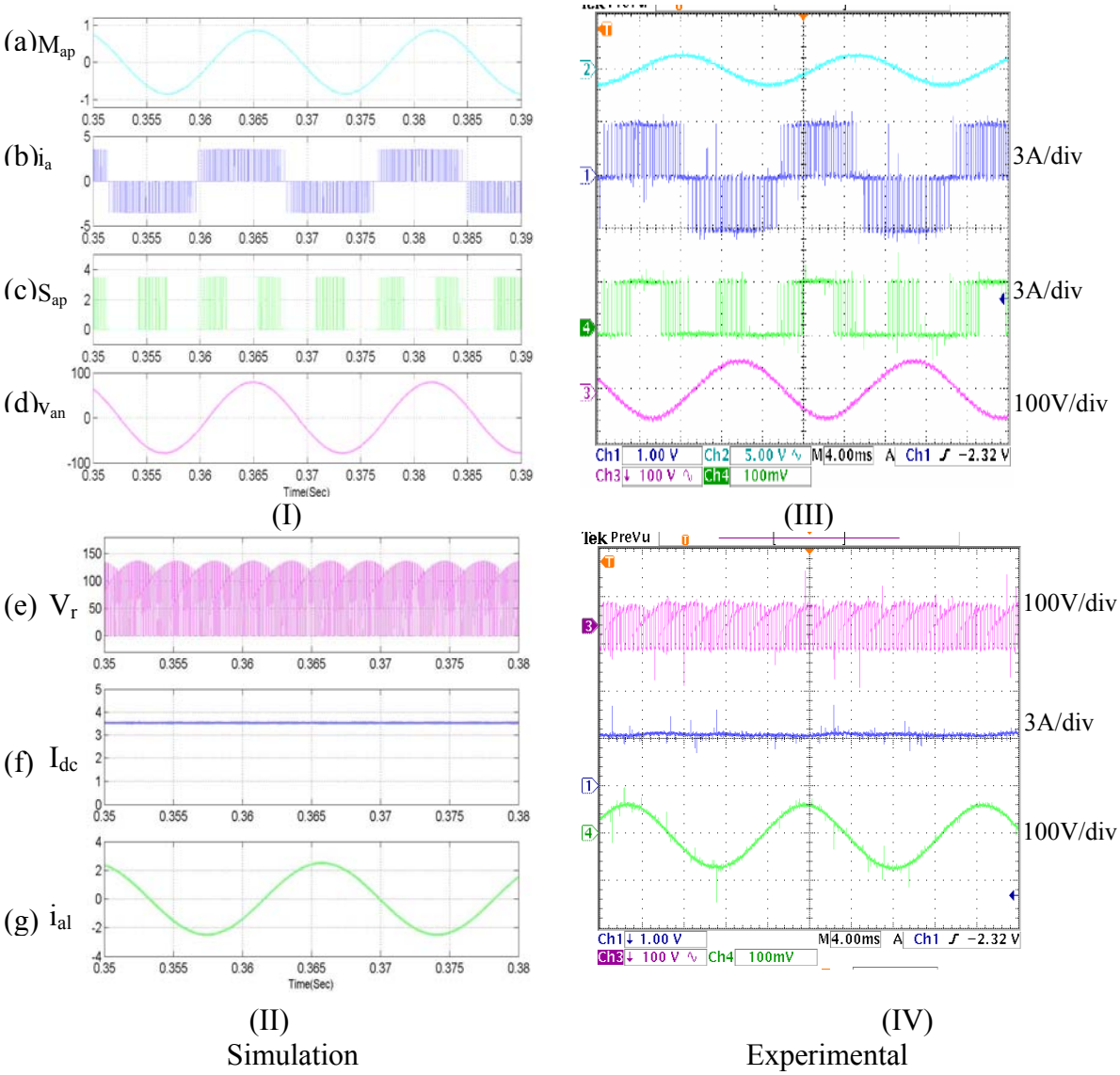


Figure 4.10 The three phase CSI using the VSI-CSI modulation scheme for continuous signals with $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30\Omega$ at $M = 0.85$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

4.6.2 Continuous Modulation in Overmodulation Region

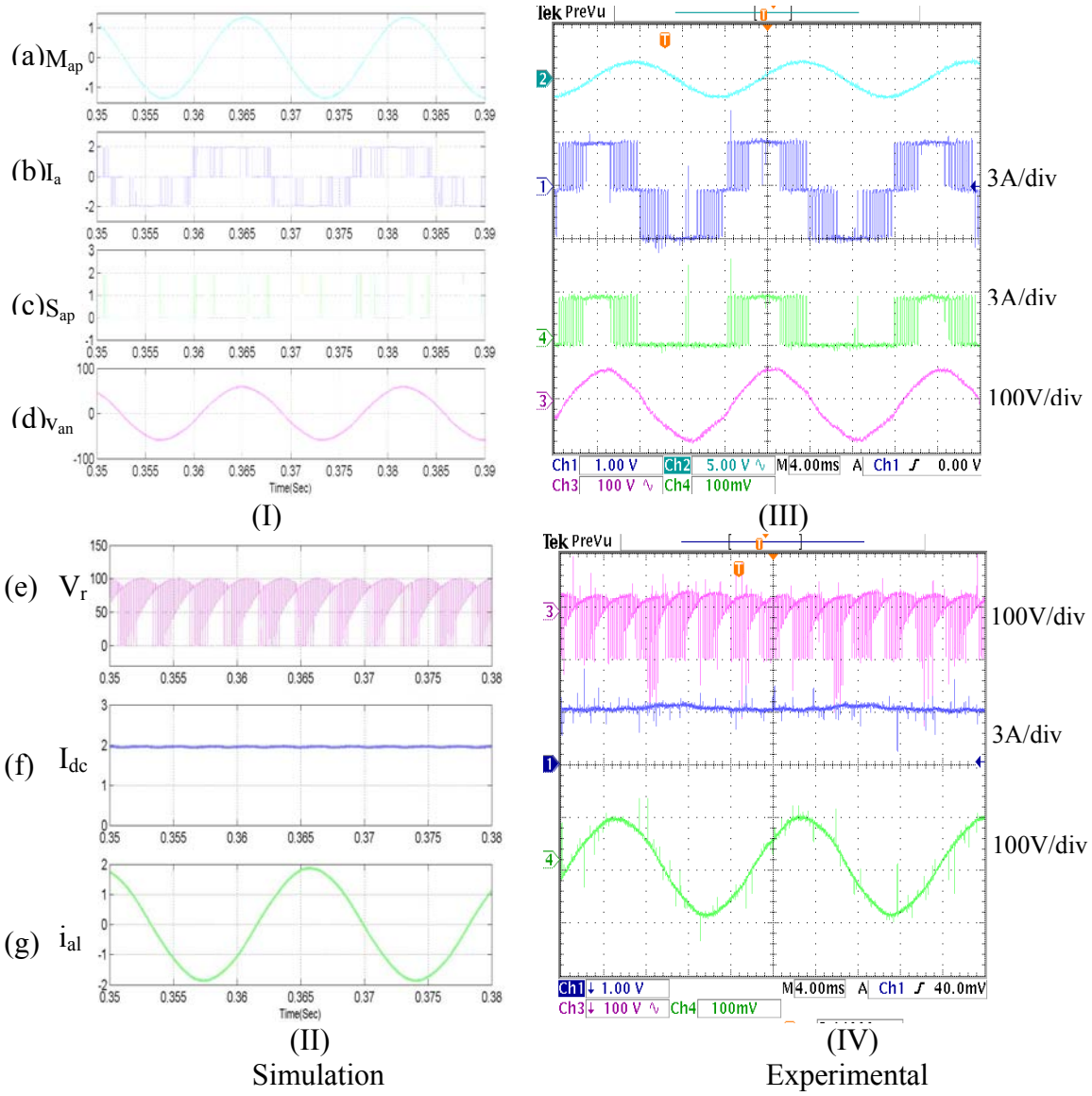


Figure 4.11 The three phase CSI using the VSI-CSI modulation scheme for continuous signals with V_{dc} = 100V, I_{dc} = 3A, R_L = 30Ω, at M = 1.25, f_s = 5kHz (a) phase 'a' modulating signal (b) phase 'a' output current, (c) phase 'a' device switching function (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

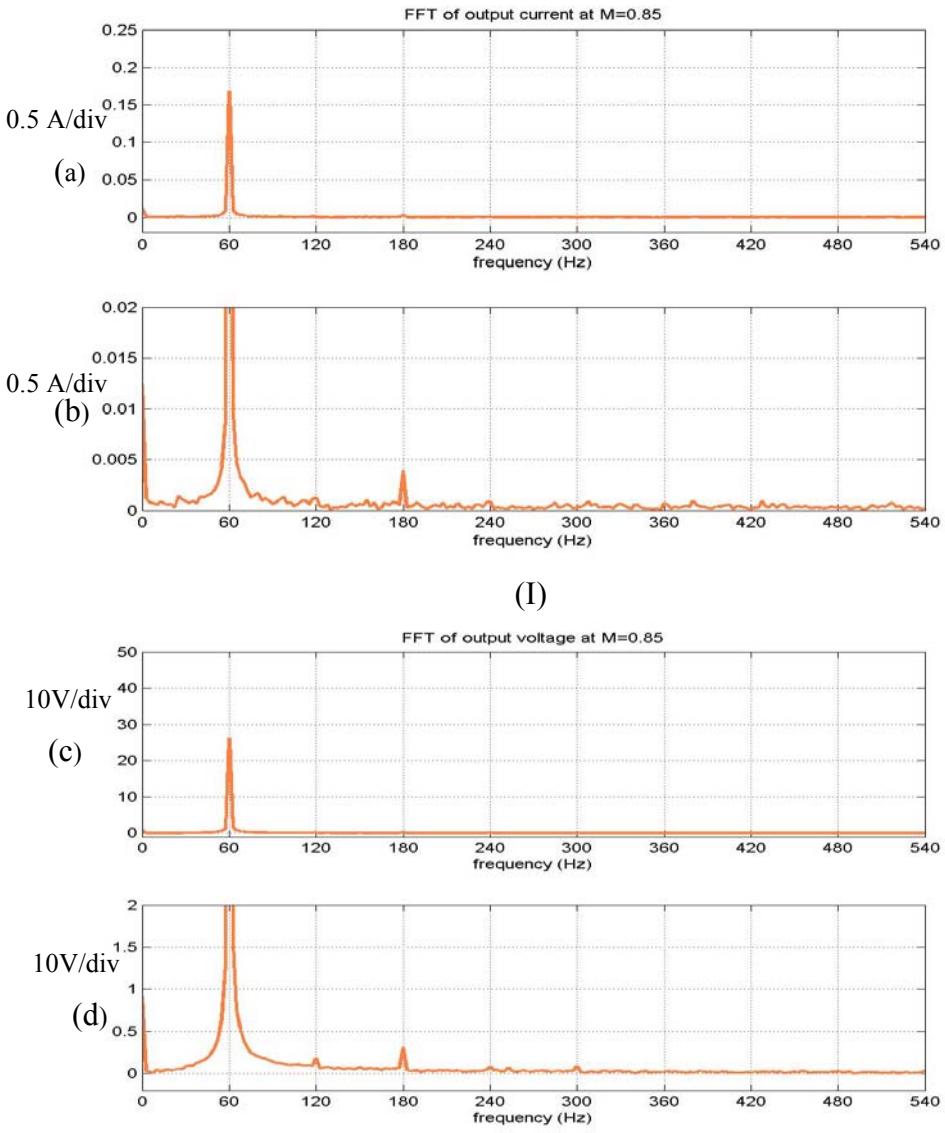


Figure 4.12 (I) and (II) FFT of the filtered output voltage and current for continuous modulation at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current, (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.

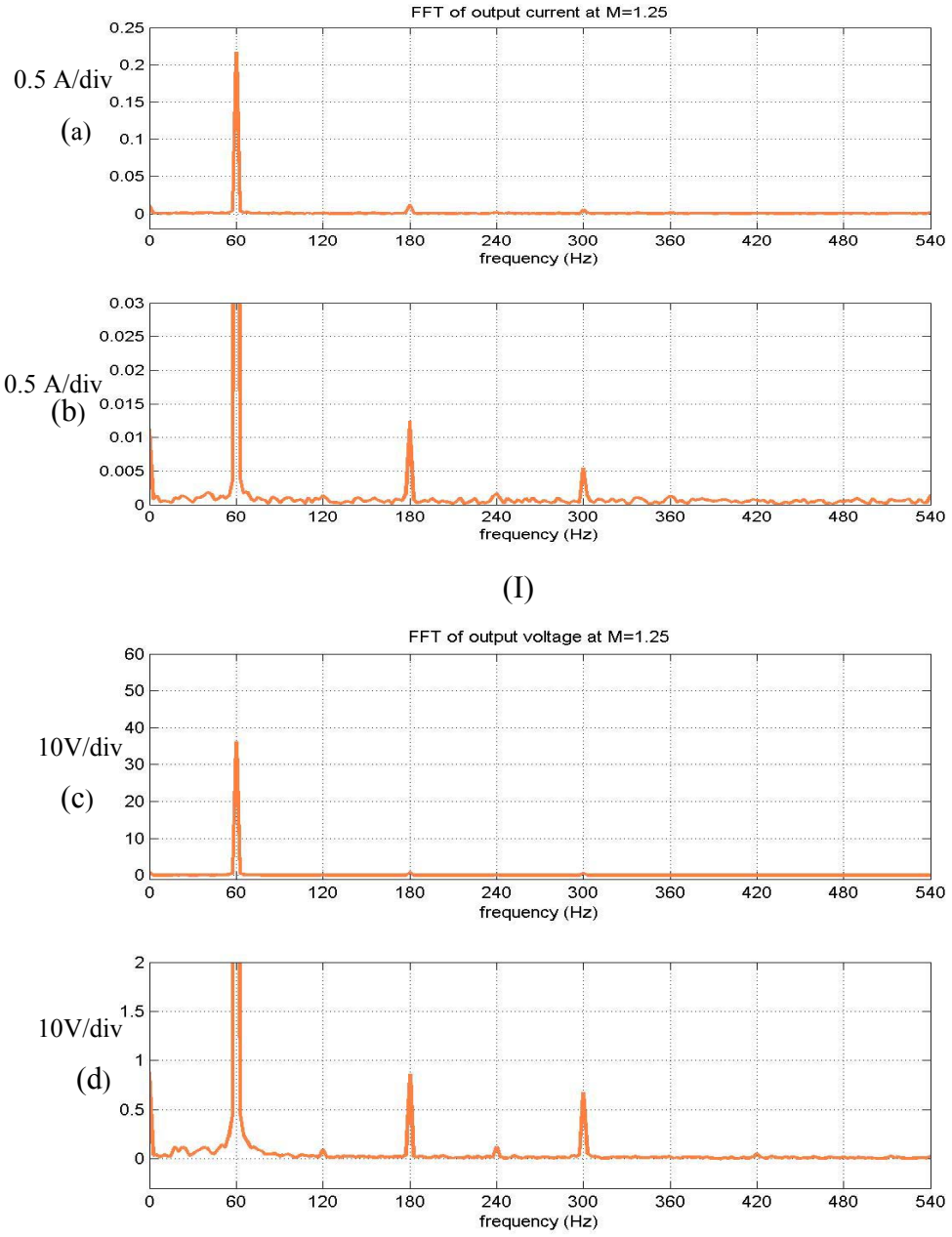


Figure 4.13 (I) and (II) FFT of the filtered output voltage and current for continuous modulation at M = 1.25 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current, (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.

4.6.3 Discontinuous Modulation for β = 0, β = 0.5, β = 1 in Linear Region

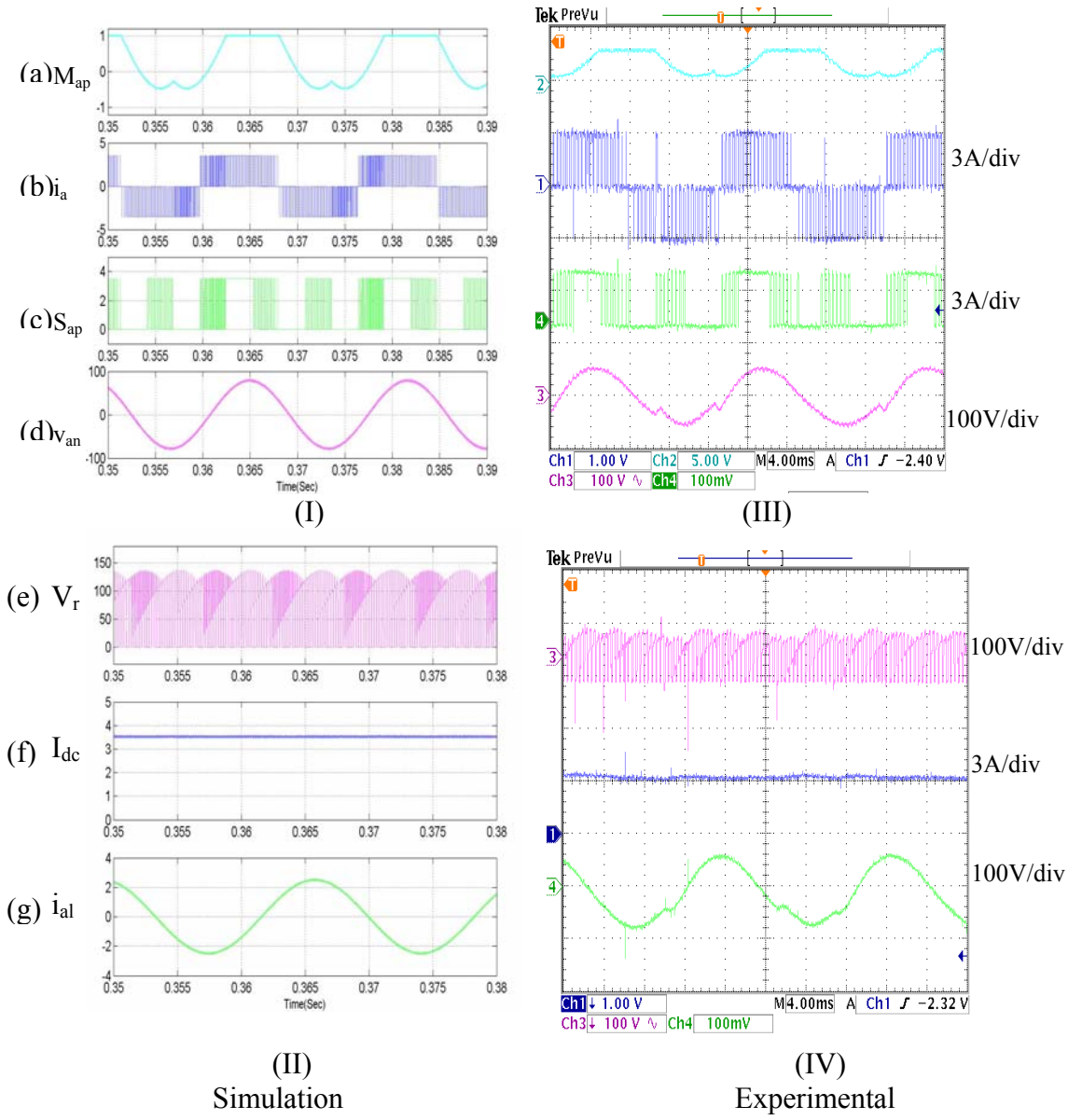


Figure 4.14 The three phase CSI using the VSI-CSI under GDPWM for β = 0 with V_{dc} = 100V, I_{dc} = 3A, R_L = 30Ω at M = 0.85, f_s = 5kHz (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

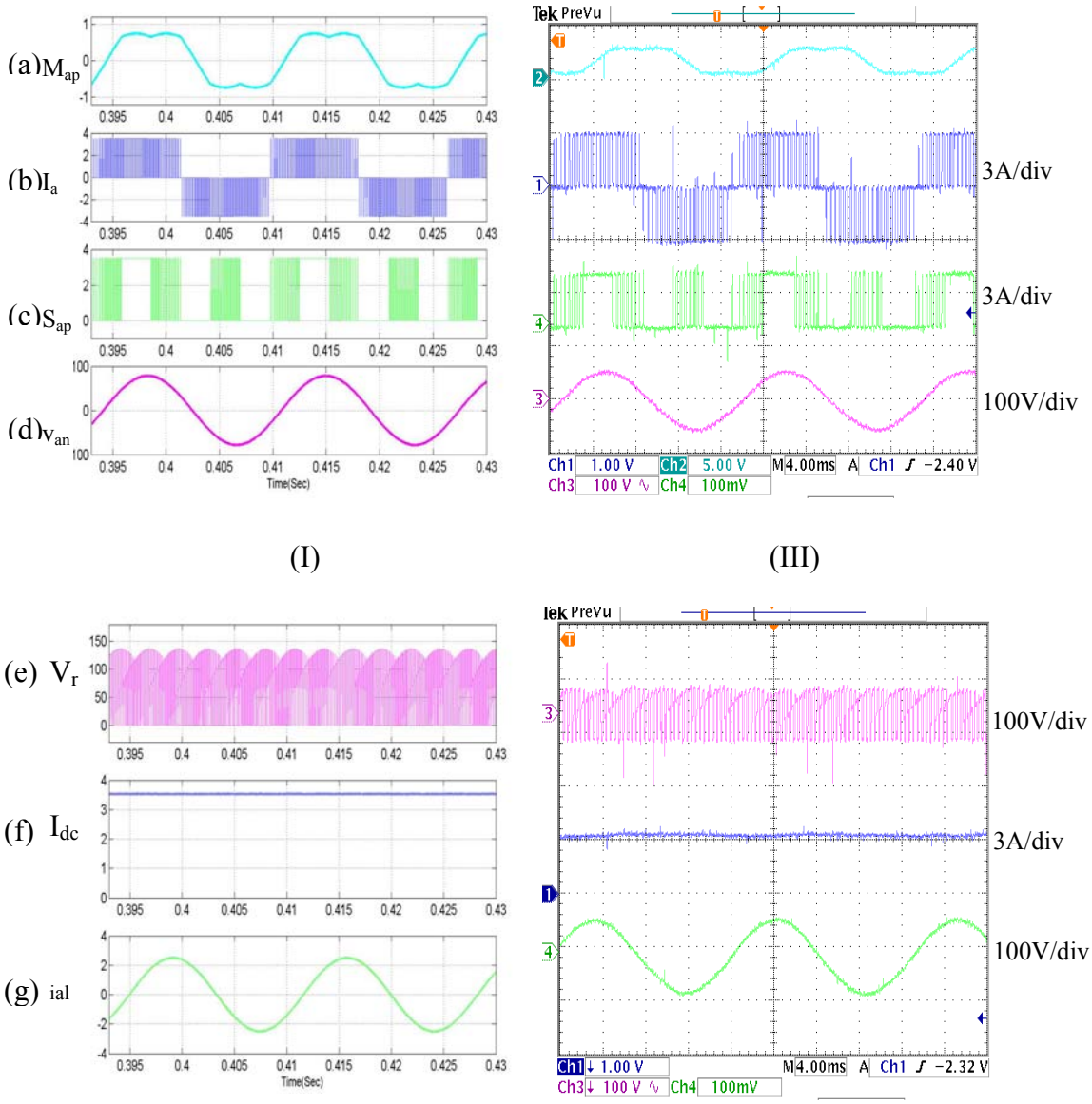


Figure 4.15 The three phase CSI using the VSI-CSI under GDPWM for $\beta = 0.5$, with $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30\Omega$ at $M = 0.85$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

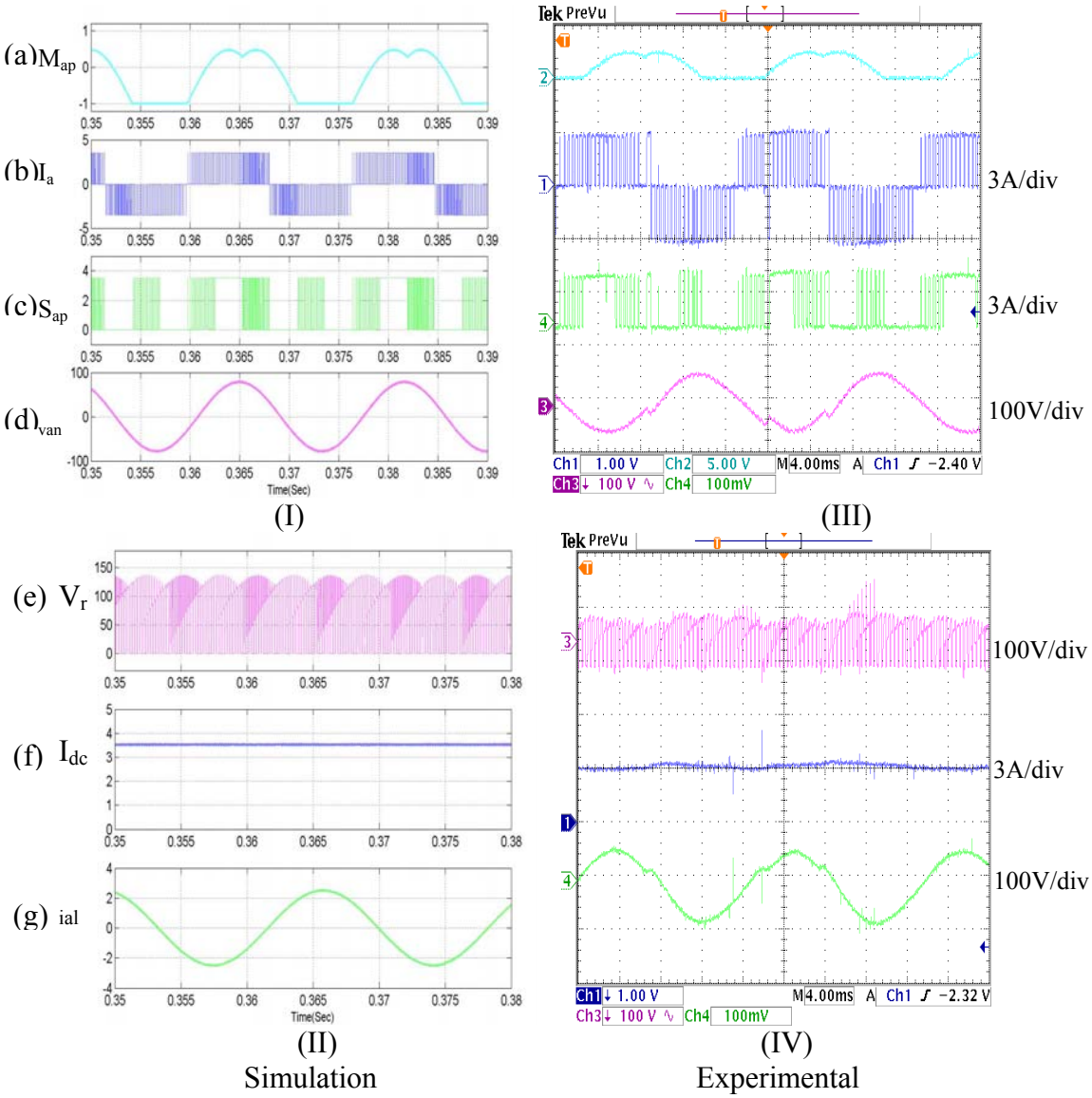


Figure 4.16 The three phase CSI using the VSI-CSI under GDPWM for β = 1, with V_{dc} = 100V, I_{dc} = 3A, R_L = 30Ω at M = 0.85, f_s = 5kHz (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

4.6.4 Discontinuous Modulation for β = 0, β = 0.5, β = 1 in Overmodulation Region

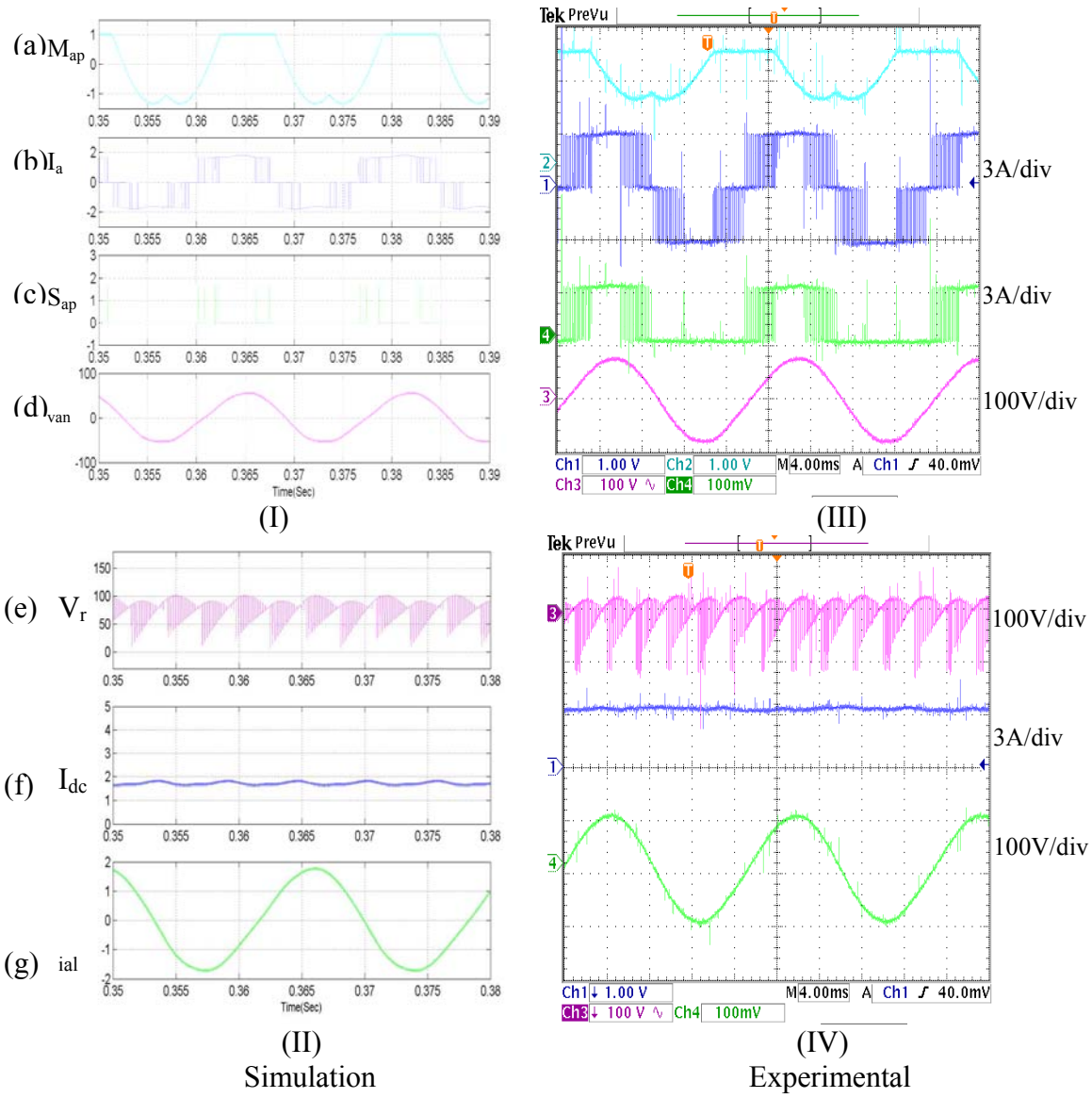


Figure 4.17 The three phase CSI using the VSI-CSI under GDPWM with, β = 0, V_{dc} = 100V, I_{dc} = 3A, R_L = 30Ω at M = 1.25, f_s = 5kHz (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

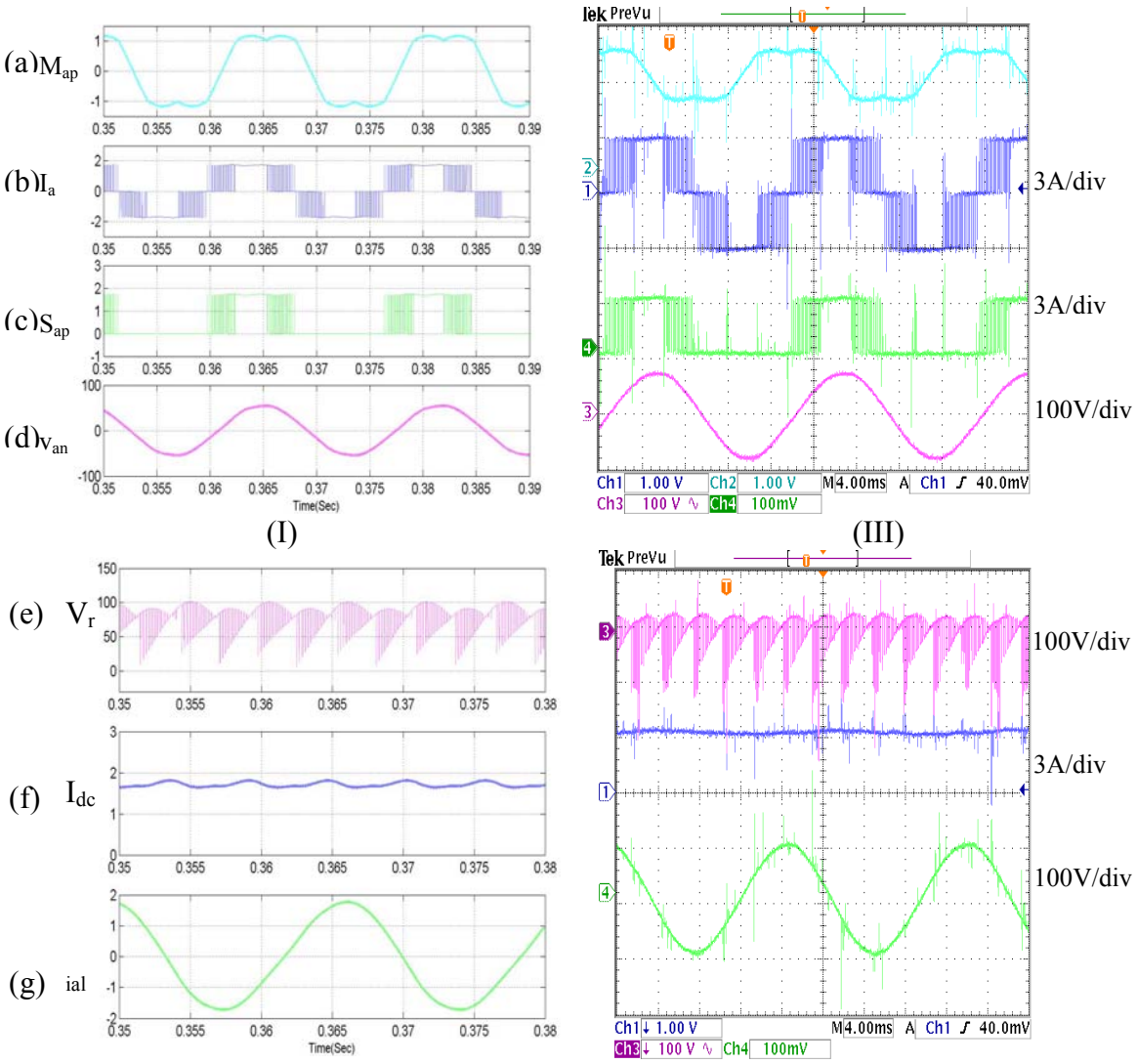


Figure 4.18 The three phase CSI using the VSI-CSI under GDPWM with, $\beta = 0.5$, $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30\Omega$ at $M = 1.25$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

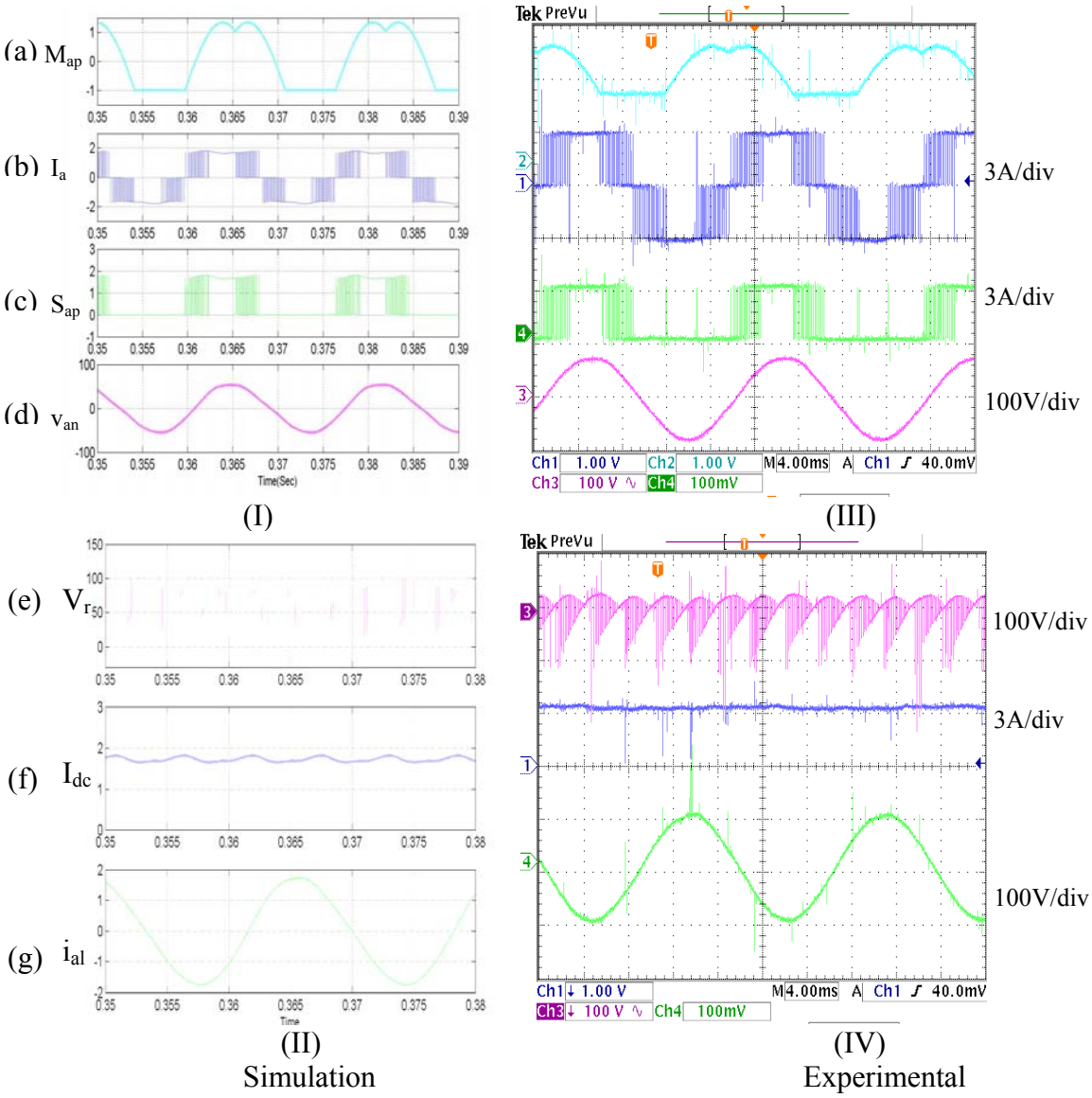


Figure 4.19 The three phase CSI using the VSI-CSI under GDPWM with, $\beta = 1$, $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30\Omega$ at $M = 0.85$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

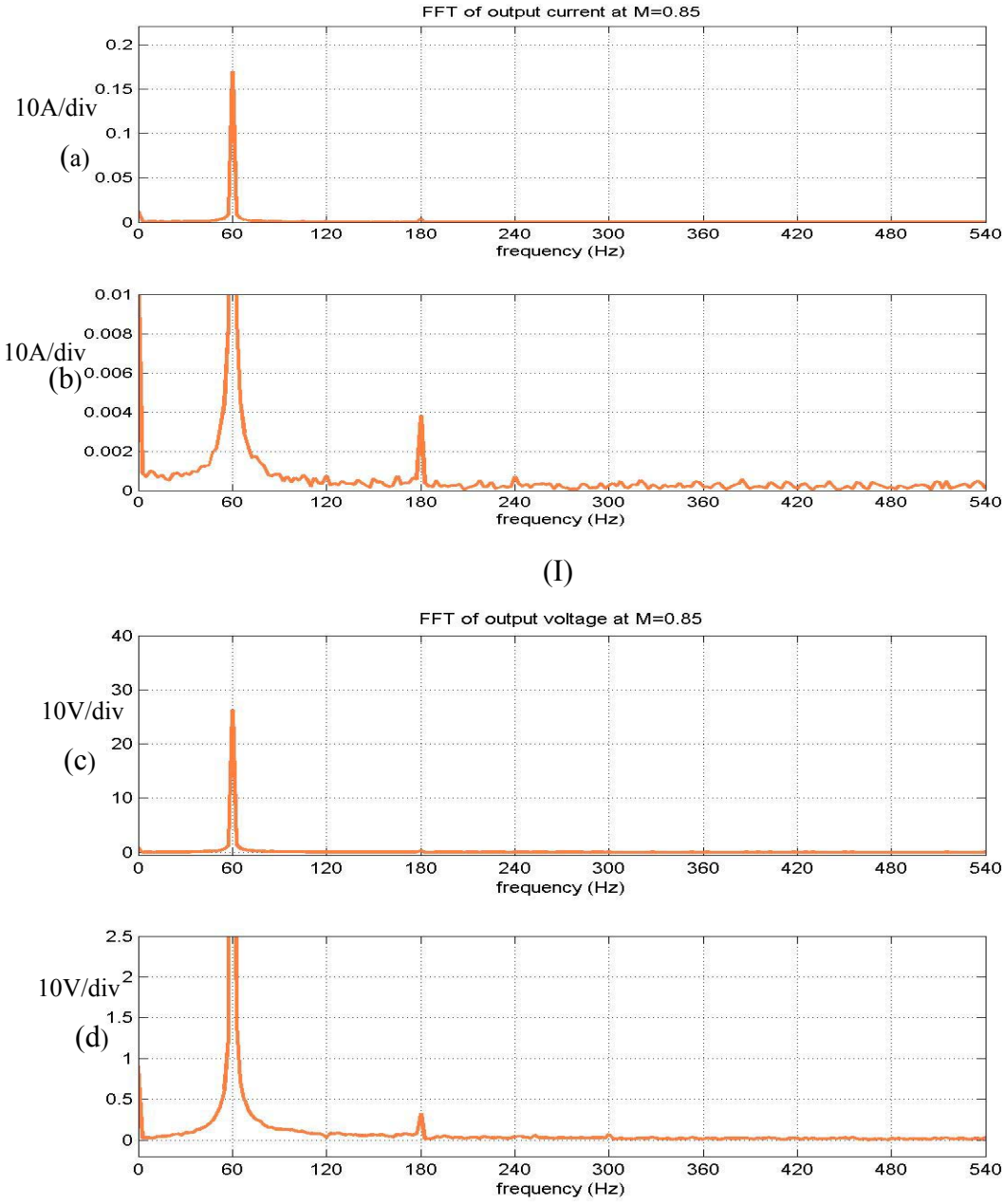
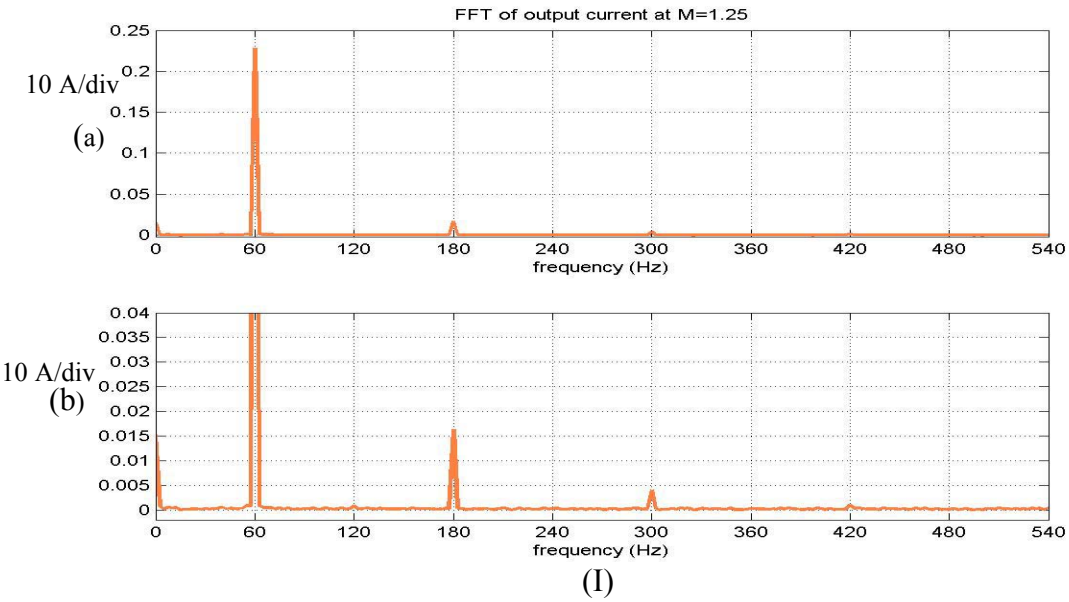
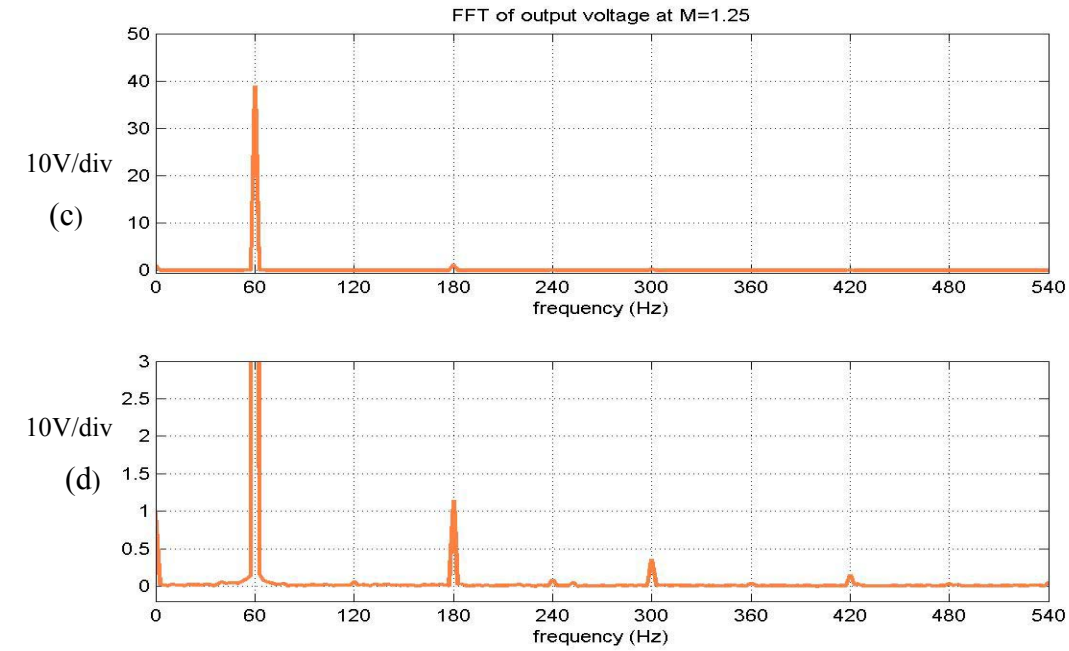


Figure 4.20 (I) and (II) FFT of the filtered output voltage and current for GDPWM modulating signals β = 0.5 at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current, (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.



(I)



(II)

Figure 4.21 (I) and (II) FFT of the filtered output voltage and current for GDPWM modulating signals β = 0.5 at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current, (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.

4.6.5 Discontinuous Modulation for δ = 0, δ = -30°, δ = -60° in Linear Region

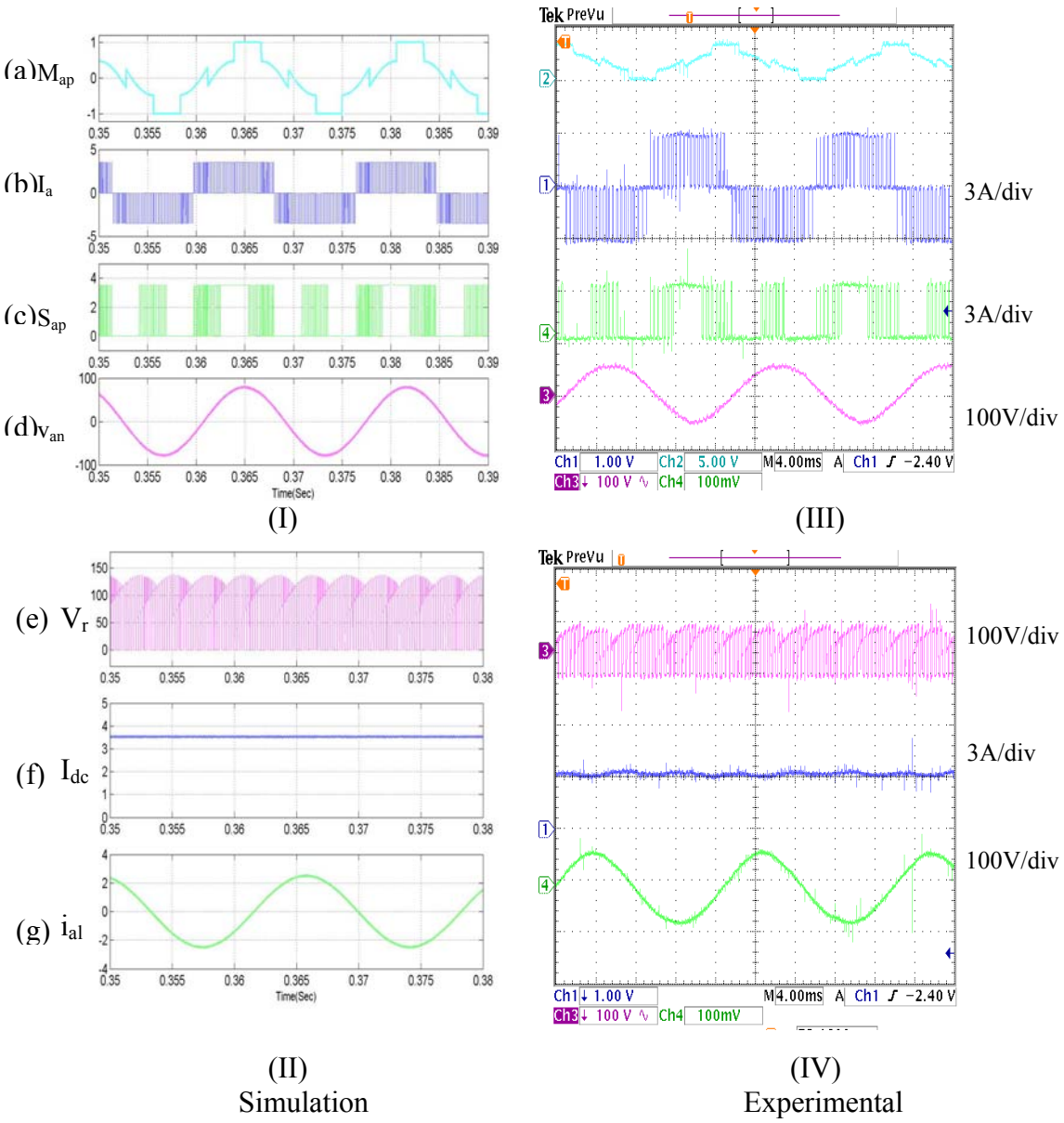


Figure 4.22 The three phase CSI using the VSI-CSI under GDPWM β = 0.5[1+SgnCos (3wt+δ)], δ = 0, V_{dc} = 100V, I_{dc} = 3A, R_L = 30 at M = 0.85, f_s = 5kHz (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) Input DC current, (g) phase 'a' load line current.

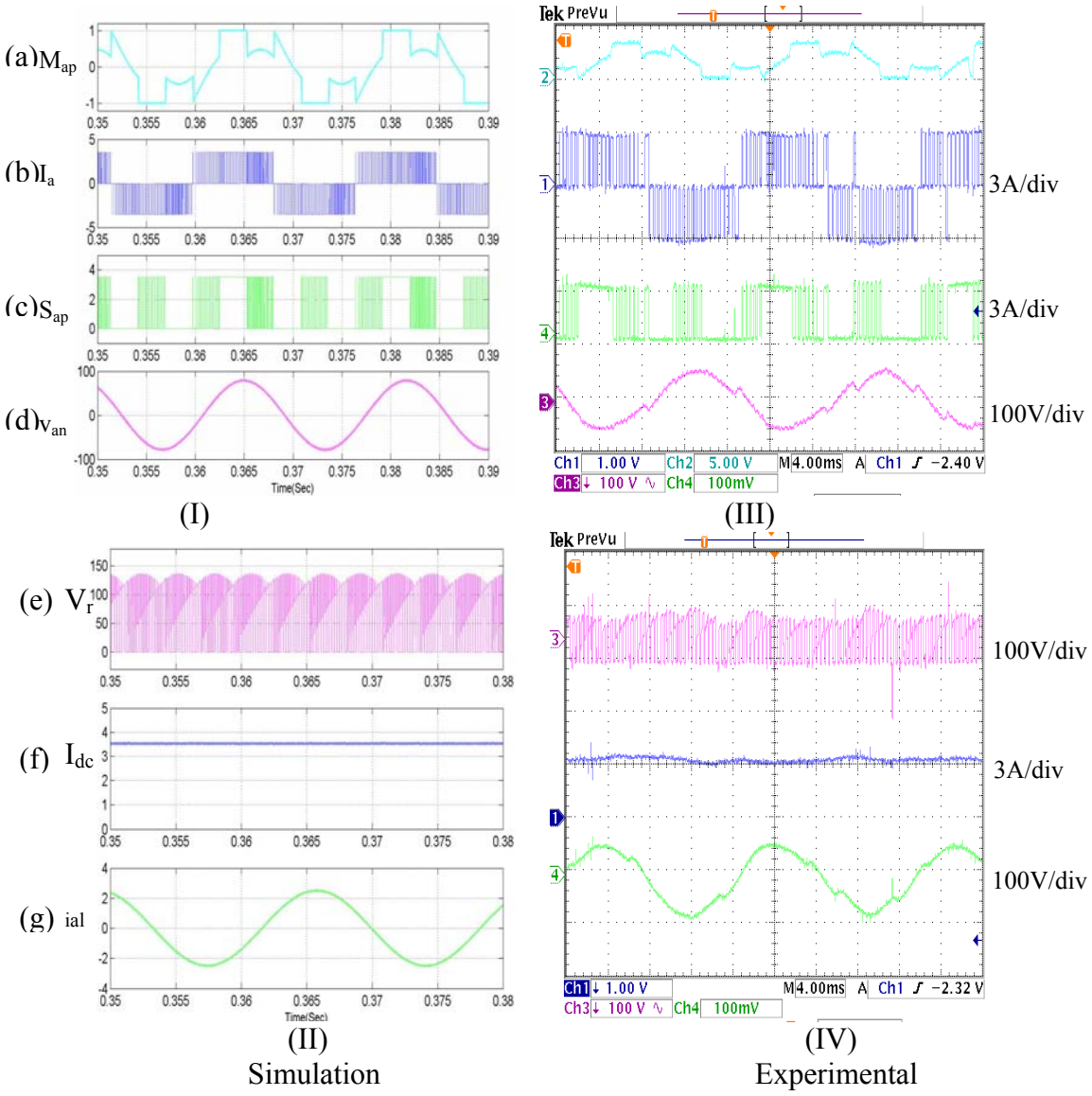


Figure 4.23 The three phase CSI using the VSI-CSI under GDPWM $\beta = 0.5[1+SgnCos(3wt+\delta)]$, $\delta = -30$, $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30$ at $M = 0.85$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) Input DC current, (g) phase 'a' load line current.

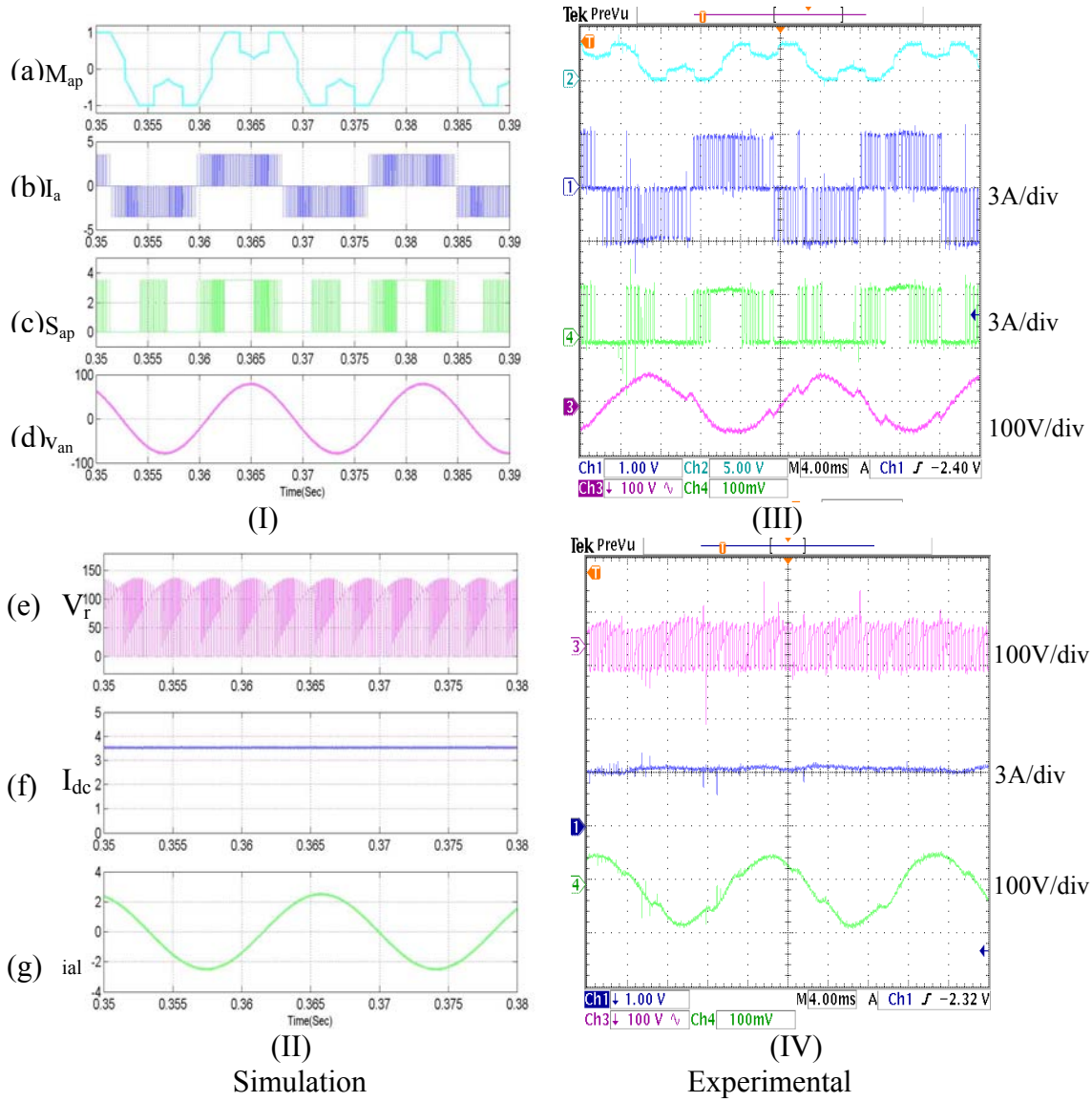


Figure 4.24 The three phase CSI using the VSI-CSI under GDPWM $\beta = 0.5[1+SgnCos(3wt+\delta)]$, $\delta = -60$, $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30$ at $M = 0.85$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

4.6.6 Discontinuous Modulation for δ = 0, δ = -30°, δ = -60° in Overmodulation

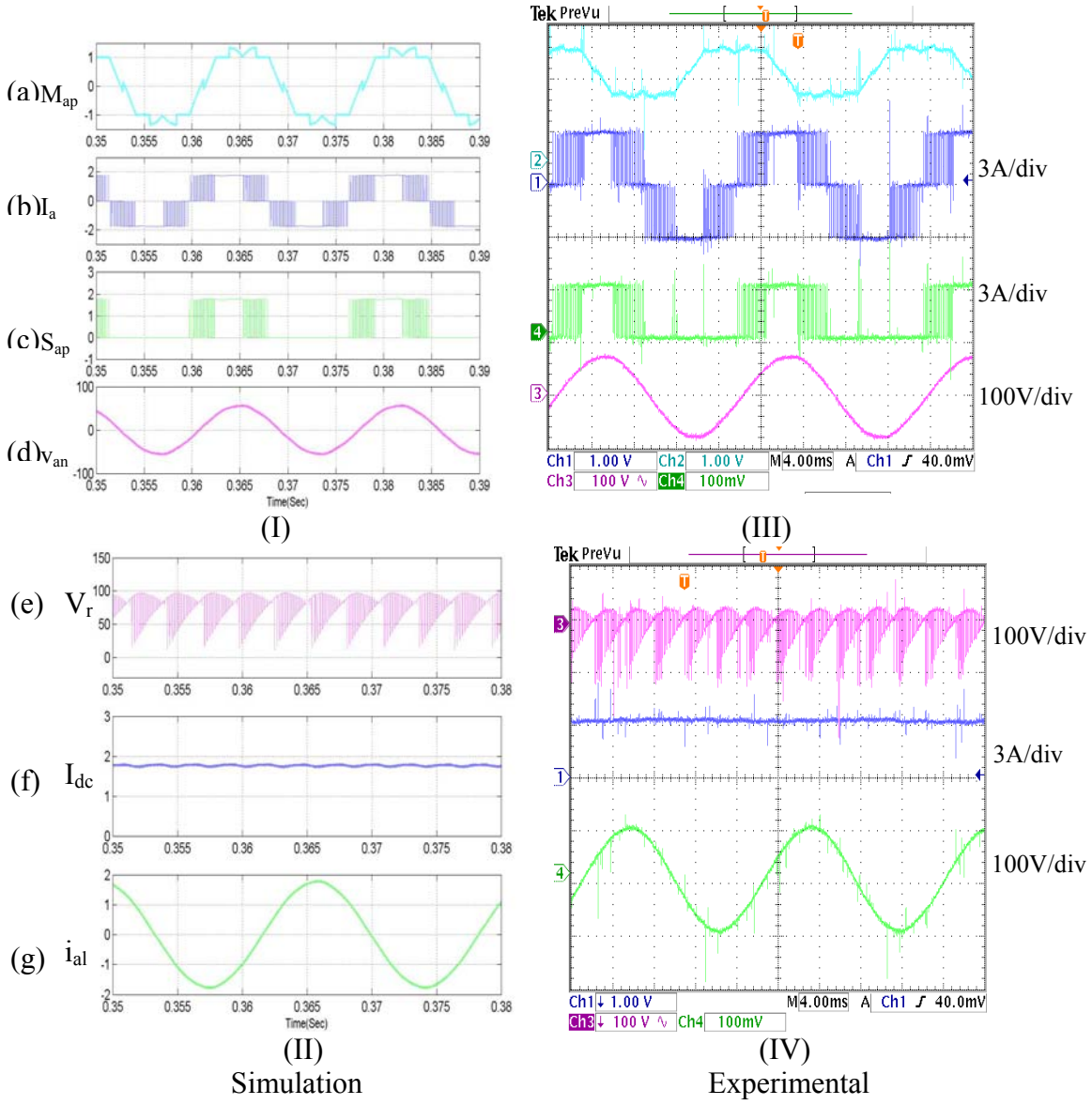


Figure 4.25 The three phase CSI using the VSI-CSI under GDPWM β = 0.5[1+SgnCos (3wt+δ)], δ = 0, V_{dc} = 100V, I_{dc} = 3A, R_L = 30 at M = 1.25, f_s = 5kHz (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

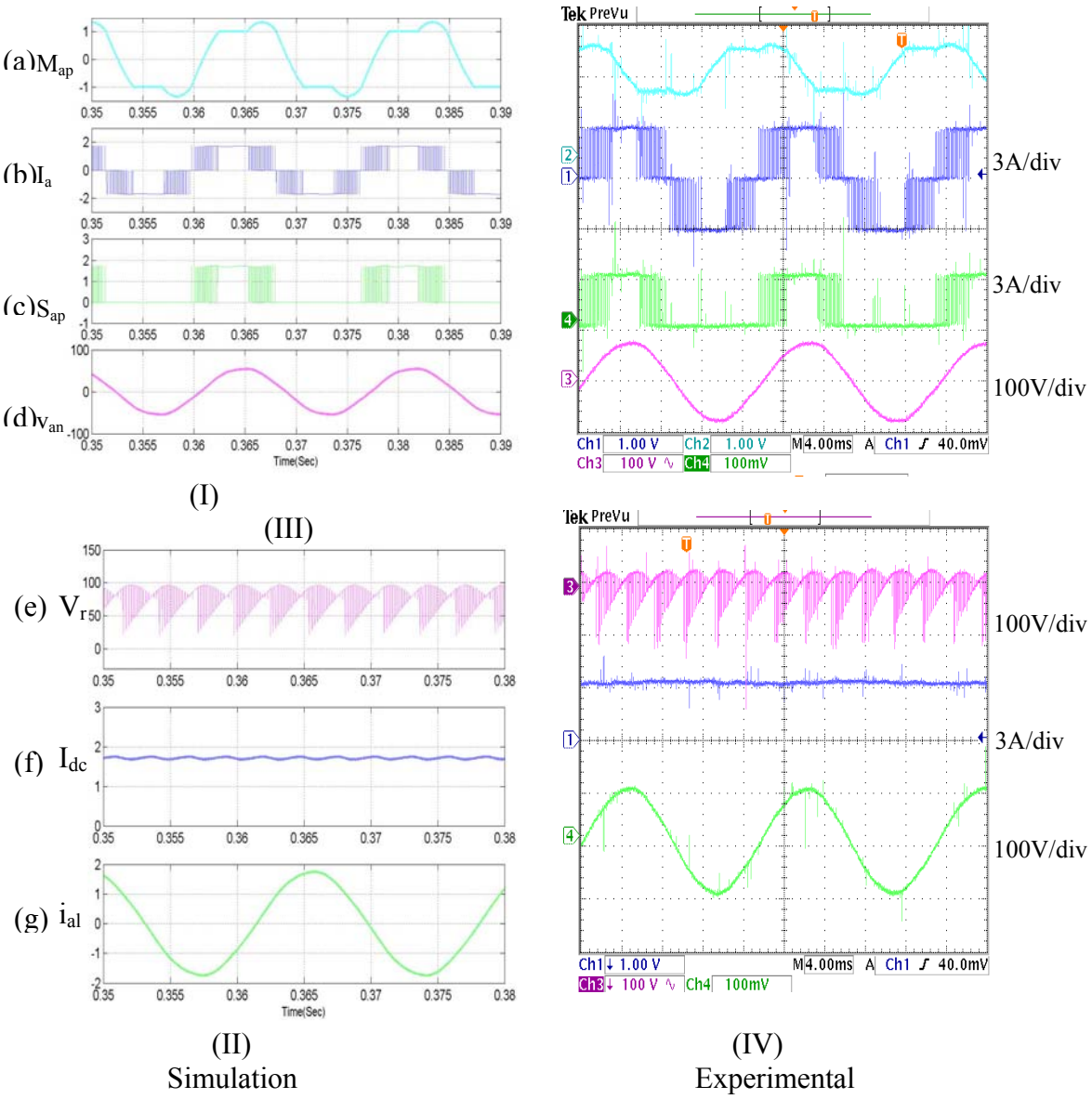


Figure 4.26 The three phase CSI using the VSI-CSI under GDPWM $\beta = 0.5[1+SgnCos(3wt+\delta)]$, $\delta = -30$, $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30$ at $M = 0.85$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

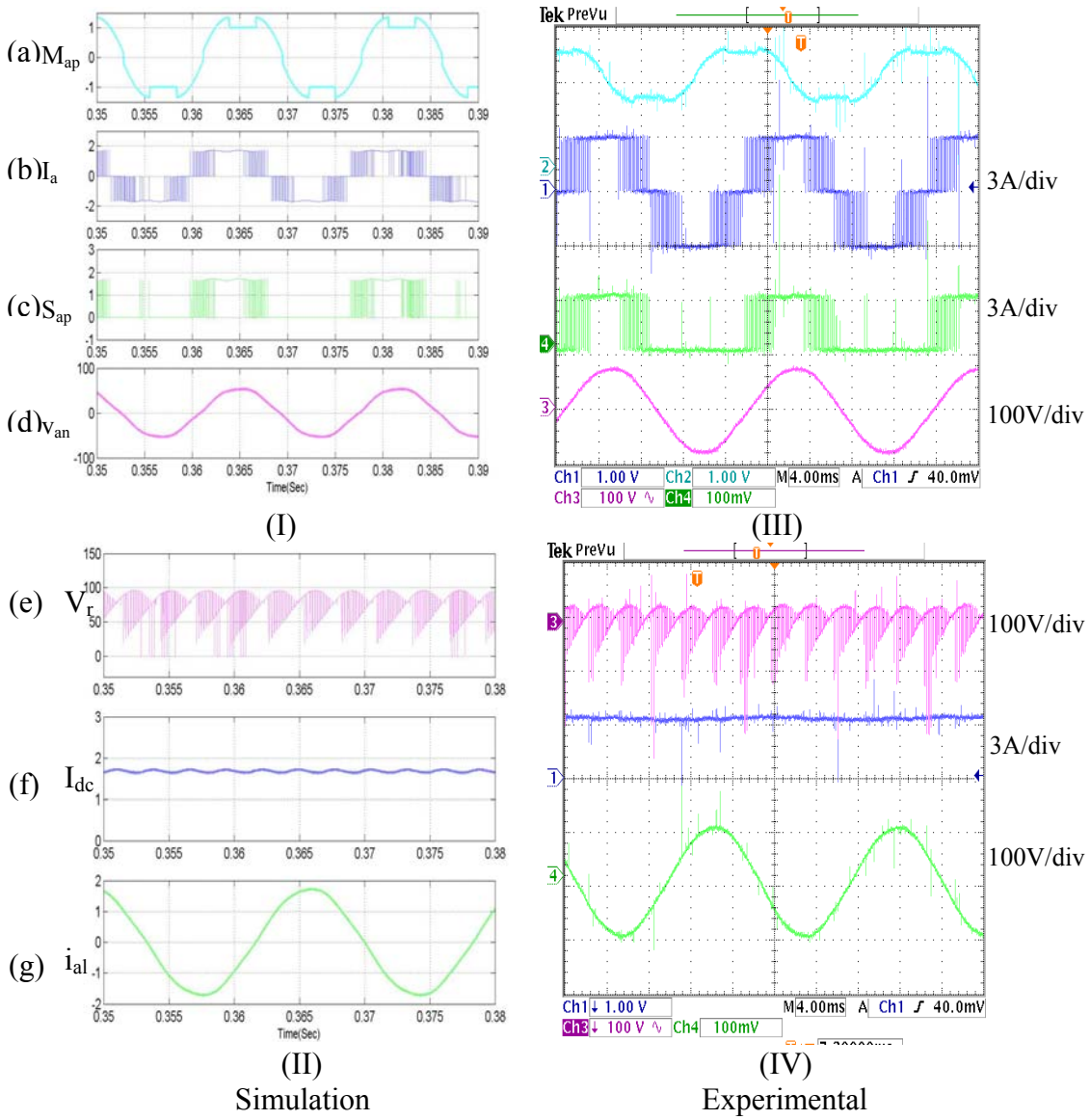


Figure 4.27 The three phase CSI using the VSI-CSI under GDPWM $\beta = 0.5[1+SgnCos(3wt+\delta)]$, $\delta = -60$, $V_{dc} = 100V$, $I_{dc} = 3A$, $R_L = 30$ at $M = 1.25$, $f_s = 5kHz$ (a) phase 'a' modulating signal, (b) phase 'a' output current, (c) phase 'a' device switching function, (d) phase 'a' capacitor voltage, (e) DC link voltage, (f) input DC current, (g) phase 'a' load line current.

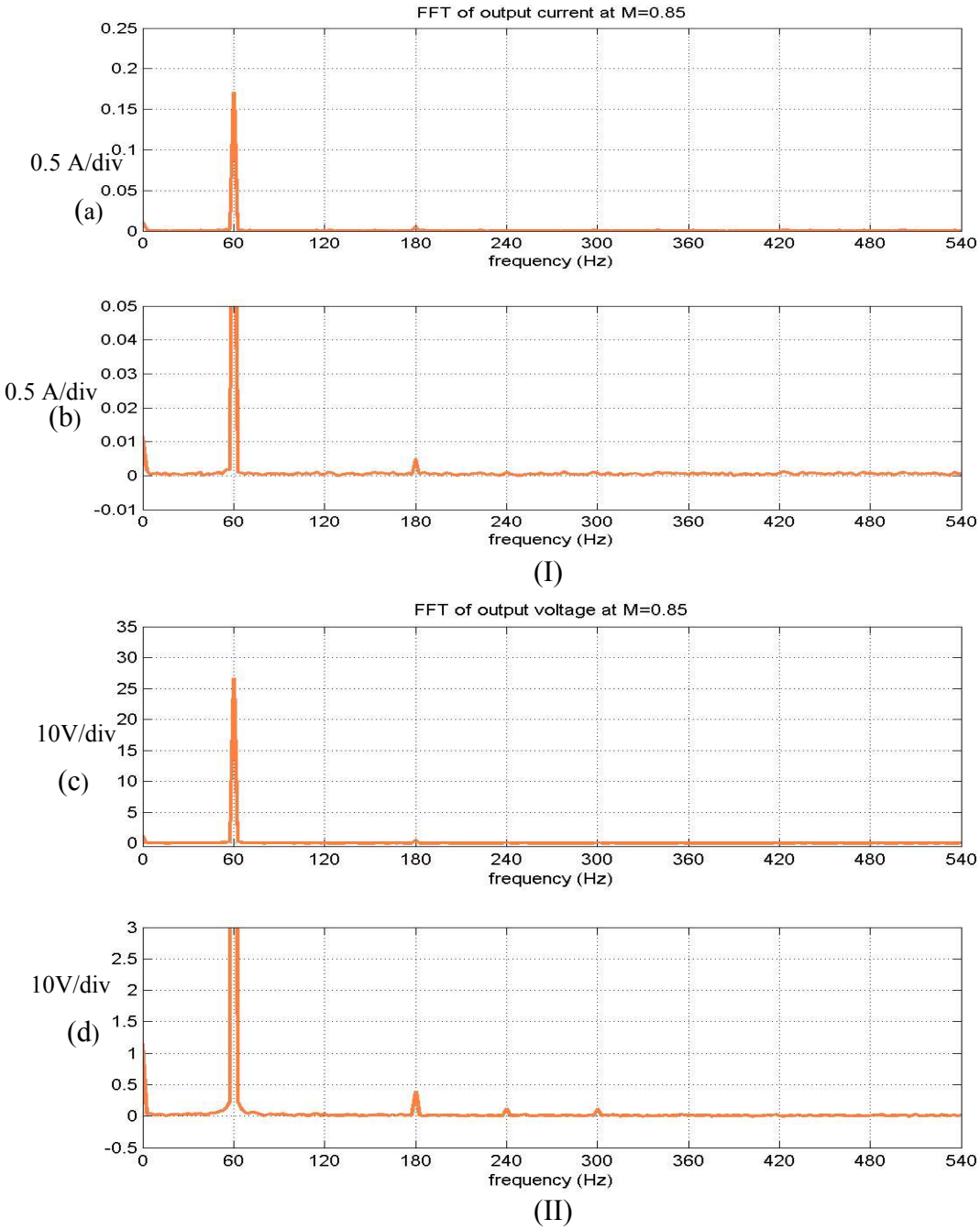


Figure 4.28 (I) and (II) FFT of the filtered output voltage and current for GDPWM modulating signals δ = -60 at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current, (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.

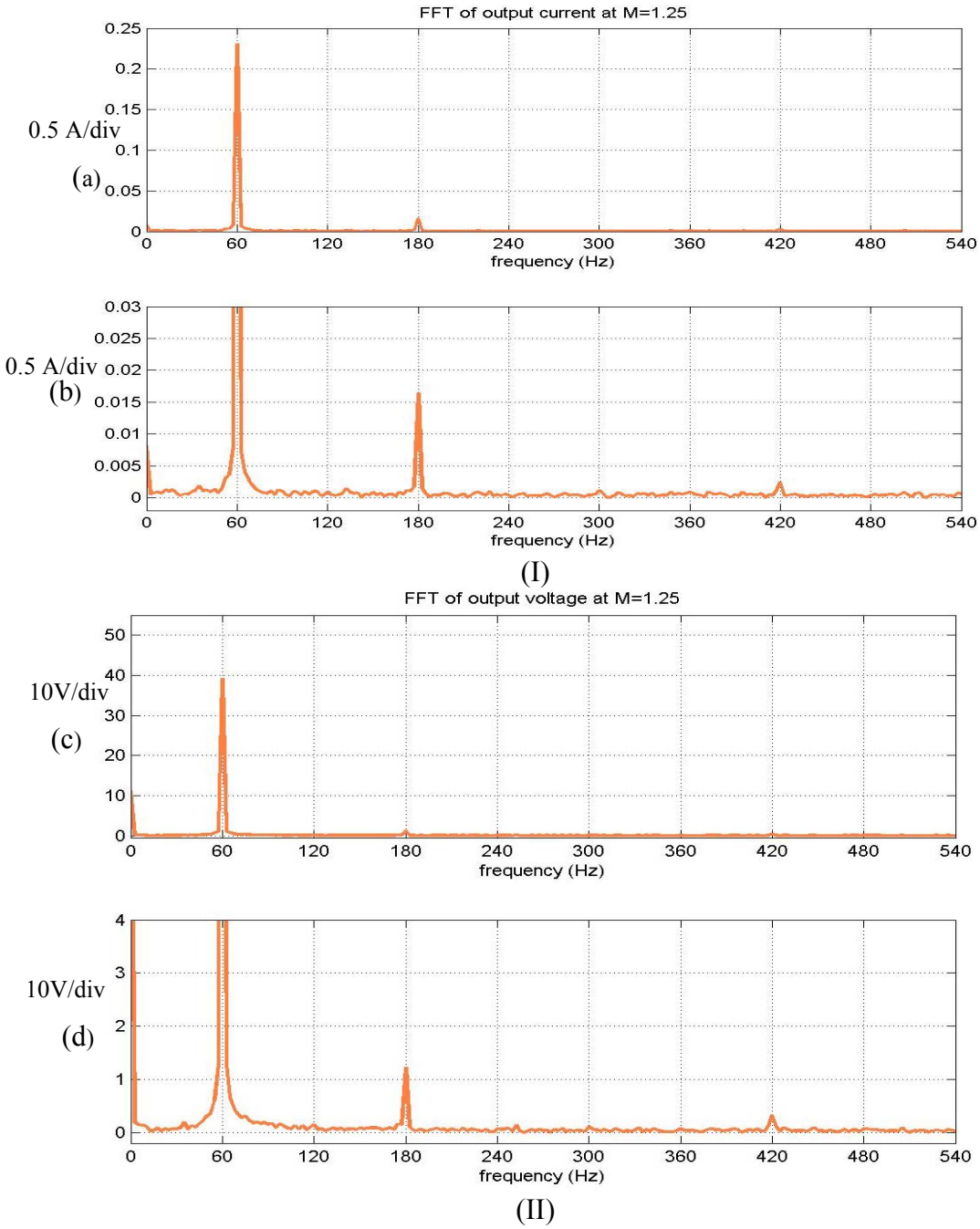
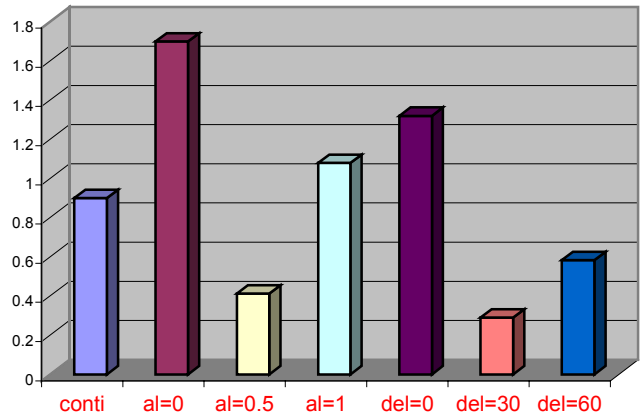
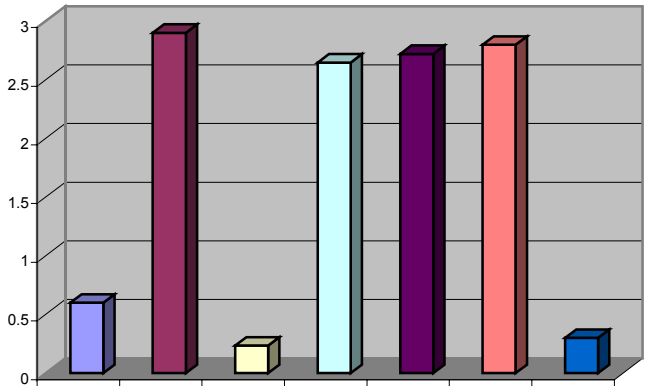


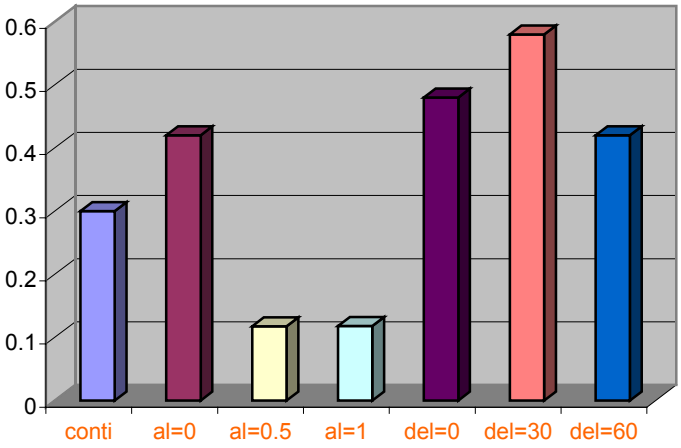
Figure 4.29 (I) and (II) FFT of the filtered output voltage and current for GDPWM modulating signals δ = -60 at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current, (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.



(I)



(II)



(III)

Figure 4.30 Comparison of the harmonics obtained from FFT of output current for various modulating schemes at M = 0.85 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic, (III) Comparison of the 5th harmonic

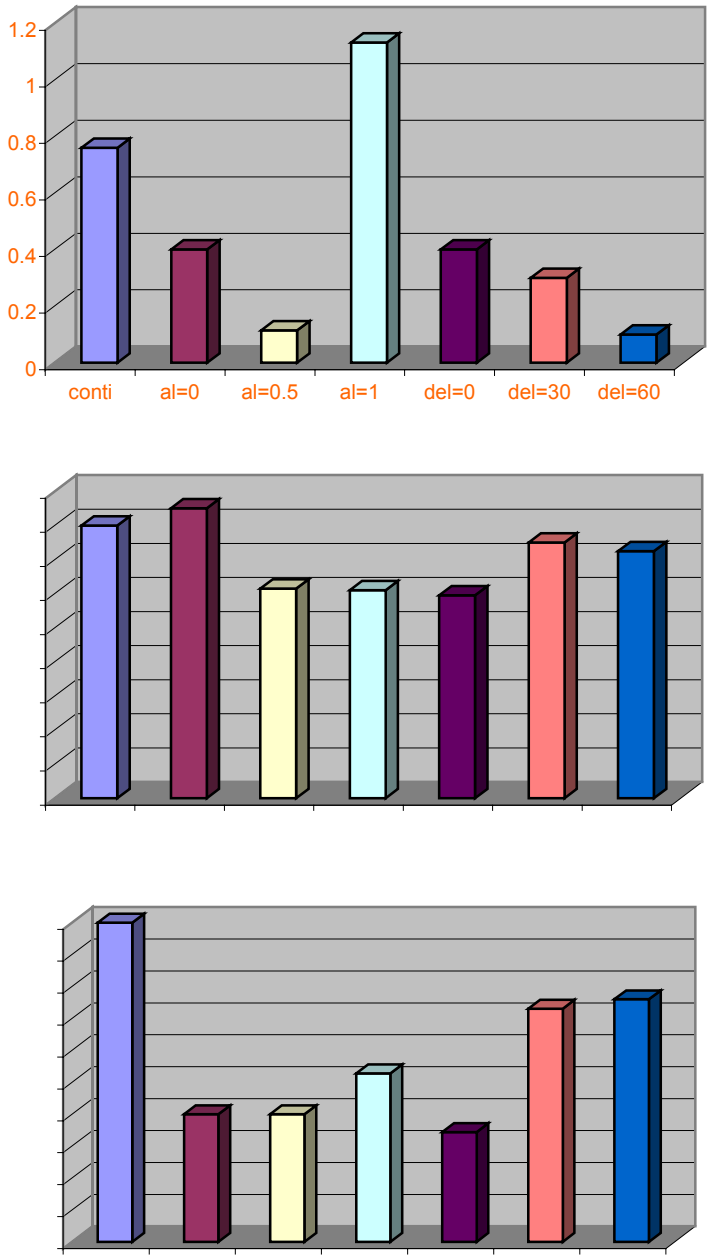
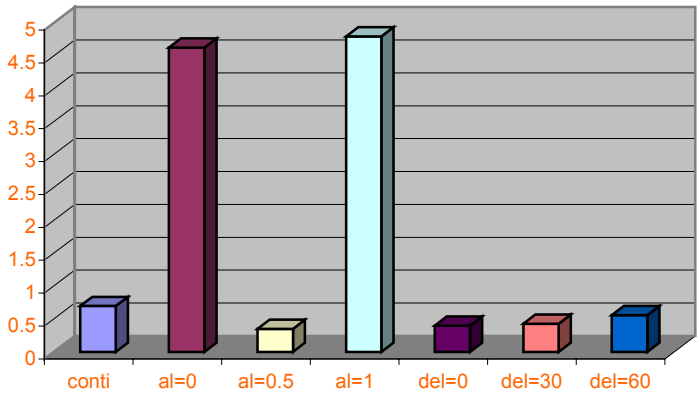
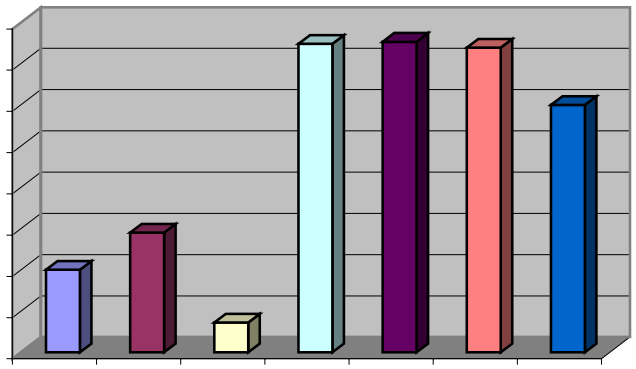


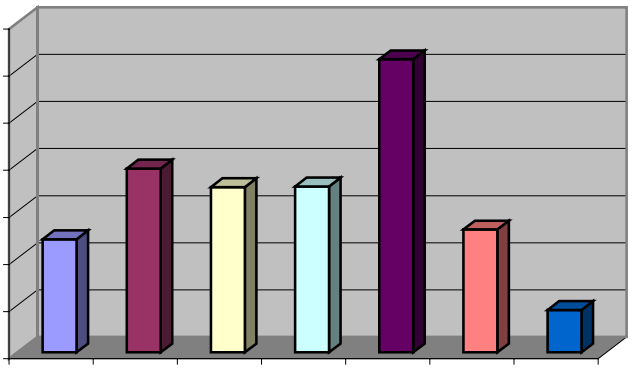
Figure 4.31 Comparison of the harmonics obtained from FFT of output voltages for various modulating schemes at M = 0.85 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic (III) Comparison of the 5th harmonic



(I)

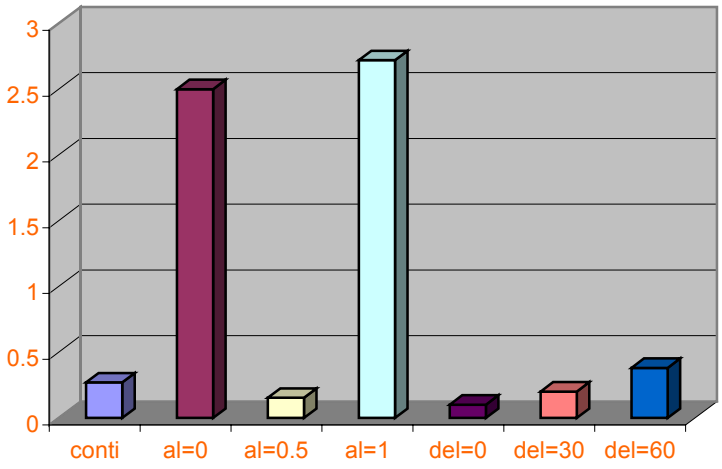


(II)

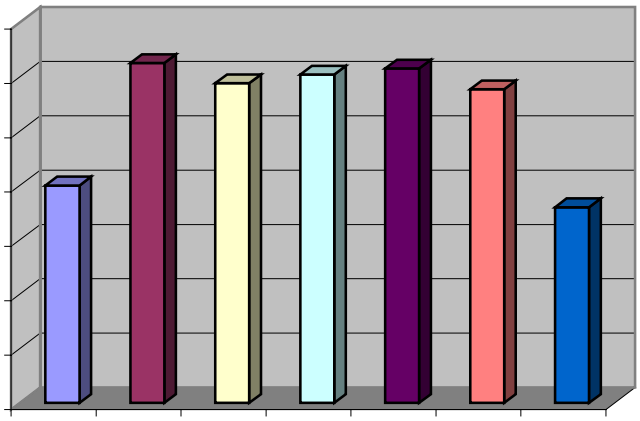


(III)

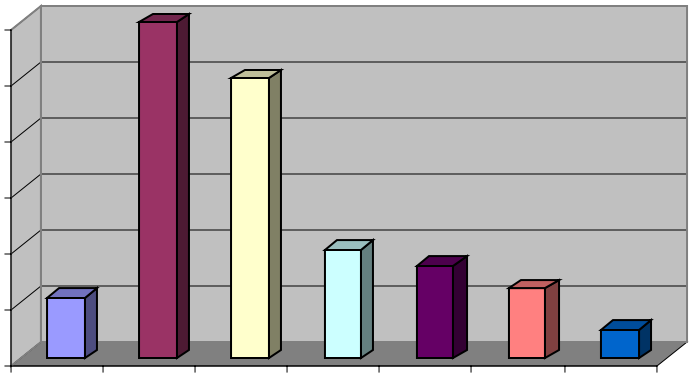
Figure 4.32 Comparison of the harmonics obtained from FFT of output currents for various modulating schemes at M = 1.25 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic, (III) Comparison of the 5th harmonic



(I)

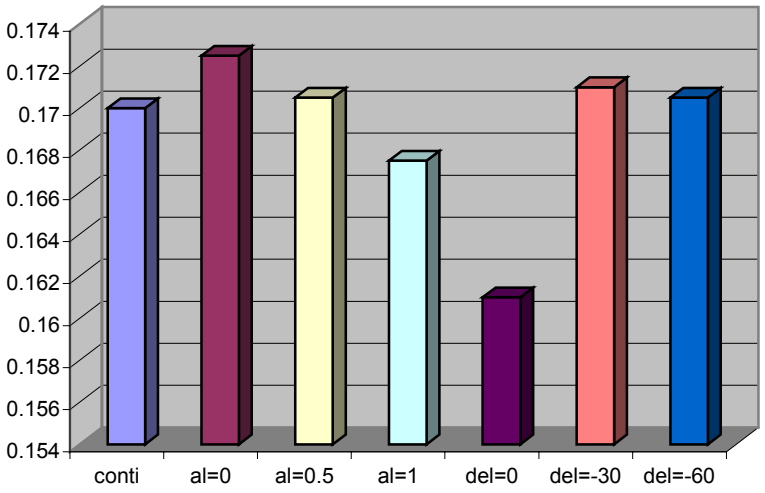


(II)

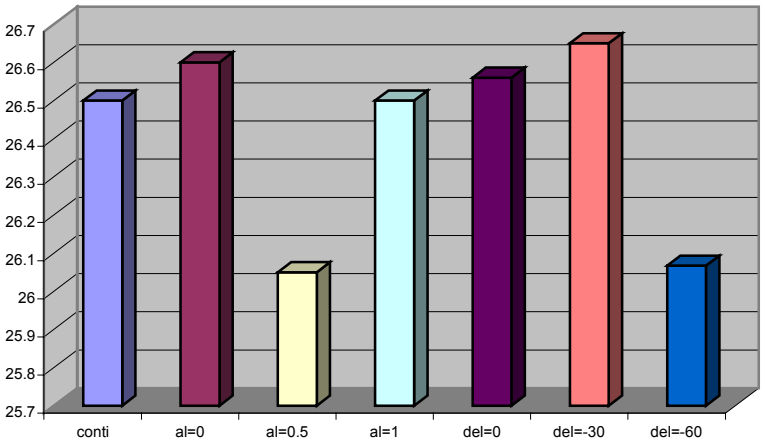


(III)

Figure 4.33 Comparison of the harmonics obtained from FFT of output currents for various modulating schemes at M = 1.25 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic, (III) Comparison of the 5th harmonic

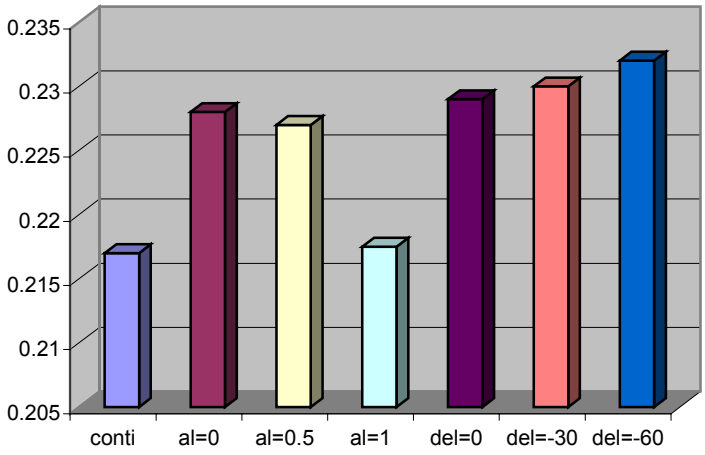


(I)

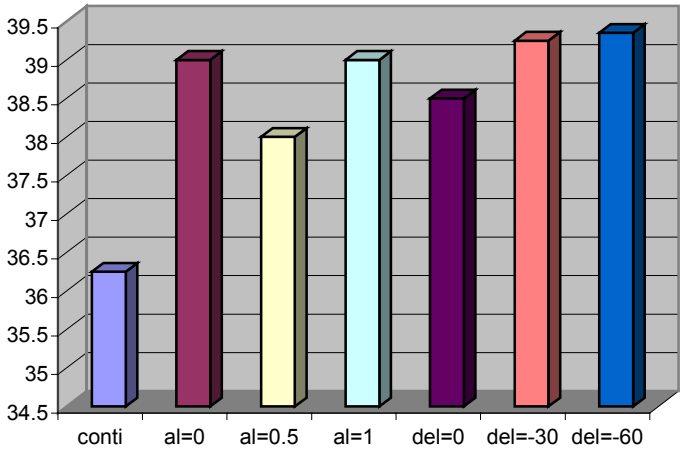


(II)

Figure 4.34 Comparison of the fundamental components obtained from FFT for different modulating signals M = 0.85 (I) output current (II) output voltage



(I)



(II)

Figure 4.35 Comparison of the fundamental components obtained from FFT for different modulating signals at M = 1.25 (I) output current (II) output voltage

4.7 Observations on the Simulation and Experimental Results

Figures 4.10 to 4.33 show the simulation and experimental results for CSI using the modulation scheme developed in this chapter. Plots for all continuous and discontinuous modulating signals in linear region and over modulation region are presented. Figures from 4.10 to 4.21 illustrate the simulation and experimental results using continuous set of modulating signals in linear modulation region. From Figure 4.9 (I) (c) it is seen that in the final switching pattern the positive DC rail is clamped for 60^{o} and the negative DC rail clamping of 120^{O}. Figures 4.10 to 4.15 gives the simulation and experimental results for various kinds of GDPWM waveforms, which have been reported in the literature [B.20, B.21]. These GDPWM waveforms are obtained by different values of β and δ. When $\beta = 0$ and $\beta = 1$ DPWMAX and DPWMIN are obtained and for $\beta = 0.5$ SPVWM is obtained and for the values of $\delta = 0, -30, -60$ DPWM1, DPWM2, and DPWM3 are obtained. All these GDPWM waveforms are used in linear region of operation. It is seen that in the final switching pattern the positive DC rail is clamped for 60^{O} and the negative DC rail is clamped for 120^{O}. Hence the amount of clamping the devices for all the modulators is almost the same but different modulators show different amount of harmonics in the synthesized currents. Figures 4.12 and 4.13 illustrates the FFT of the output currents and the voltages synthesized for continuous modulation at M = 0.85 and M = 1.25. Figures 4.20 and 4.21 shows the FFT of the output voltages and output currents for a GDPWM modulating signals at $\beta = 0.5$ and Figures 4.28 and 4.29 shows the FFT of the output current and voltages waveforms for a DPWM3 in both the linear and overmodulation region. The percentage of 2^{nd}, 3^{rd}, and 5^{th} Harmonic

components present in each of these waveforms is compared using a bar diagram as shown in Figures 4.30 to 4.33. Figures 4.34 and 4.35 gives comparison of the amount of fundamental voltage and current synthesized by different modulators, and it is seen that the all modulators show almost the same amount of gain. But the amount of gain in the linear region is more then in overmodulation region. All these FFT and harmonic comparison plots concludes that continuous modulation scheme give superior high quality waveform especially in linear operation region when compared to the other GDWPM signals and also in terms of current gain, continuous modulation scheme gives high current gain. From the FFT of the currents and voltages with continuous modulation it is seen that there are less number of 3^{rd} and 5^{th} harmonic components. As in the case of discontinuous modulation scheme the amount clamping time for all the modulator remains the same. There is no much difference in the sense of switching loss. But the only difference can be made in terms of harmonic content in each of the waveform synthesized and the amount of current gain with these modulators. It is seen that the SVPWM wave form i.e. for $\beta = 0.5$ show some good performance output waveforms in linear region of operation. The amount of harmonic content in the synthesized current is very much less in linear region. Hence this SVPWM waveform can be considered as the high performance modulator. SVPWM shows similar characteristics in the synthesized current and voltage waveform as compared to a continuous modulation scheme. But in case of over modulation, all the modulator performances are similar. Hence it is difficult to decide which is the best operating modulator in over modulation region. But in common it is observed that in the over modulation amount of harmonics increases and also the overall current gain decreases but the only advantage of operating in over

modulation is that the amount of switching loss decreases and the devices are clamped for some extra time, which reduces the effective switching loss.

CHAPTER 5

A NEW GENERALIZED DISCONTINUOUS PWM STRATEGY FOR THE CURRENT SOURCE INVERTER

5.1 Introduction

This chapter presents a new modulation strategy adopted for the current source inverters. In the previous chapter it was shown that the states of the VSI are mapped to the active and null states of the CSI, which is an indirect way of modulating the current source inverter [B.18, B.22, B.23, B.24]. This section deals with a direct modulation scheme, which uses the active and null states of the CSI itself to formulate the modulation scheme [B.25]. Simulation results are presented and experimental results are provided to validate the simulation results. The main objective of this scheme is to have a direct methodology for the current source inverters. It is seen that this direct modulation of the CSI can be achieved with both

- Sine Triangle Modulation Scheme (SPWM).
- Space Vector Modulation Scheme (SVPWM).

5.2 Carrier–Based Modulation Scheme

This chapter makes a novel contribution to the development of the carrier-based generalized discontinuous modulation scheme for the three phase current source

inverters. Through intensive analyses and experimental results, the modulation possibilities are opened up and the relation between the new carrier-based technique and the 3-D space vector [B.17] are explicated. In this scheme a new algorithm is proposed for online carrier based modulation for the CSI, which is a direct method of synthesizing the three phase reference currents.

5.2.1 Derivation of Discontinues Modulating Signals

Figure 5.1 shows the schematic diagram of the three-phase current source inverter connected to an R-L load. The possible active and null states of the inverter are shown in Table 5.1.

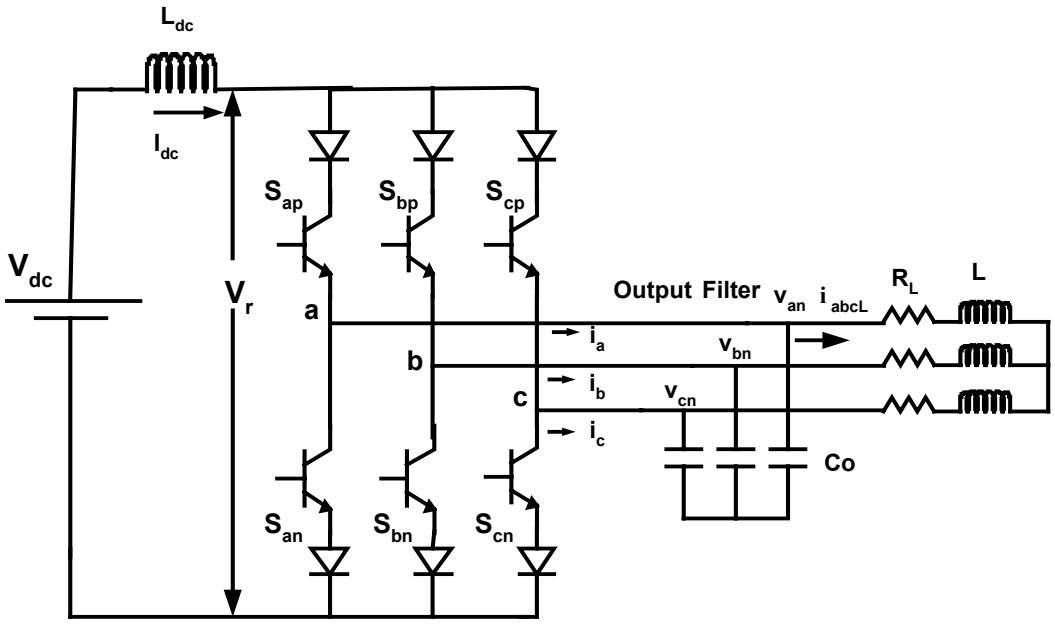


Figure 5.1 Circuit diagram of the three-phase CSI feeding an R-L Load

Table 5.1 Switching States in Three-phase CSI

	State	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
ACTIVE	I_1	1	1	0	0	0	0
	I_2	0	1	1	0	0	0
	I_3	0	0	1	1	0	0
	I_4	0	0	0	1	1	0
	I_5	0	0	0	0	1	1
	I_6	1	0	0	0	0	1
NULL	I_7	1	0	0	1	0	0
	I_8	0	1	0	0	1	0
	I_9	0	0	1	0	0	1

Table 5.1 gives the devices, which are turned ON during the active and null modes of operation. There are six active states [$I_1 \ldots I_6$] and three null states I_7, I_8, I_9. Table 5.2 gives the amount of current flowing in each phase during the active and null modes of operation. The transformed currents in q-d-o stationary reference frame are listed. The q-d-o currents are obtained using the following expressions of transformations

$$I_q = \frac{1}{3}[2i_{ap} - i_{bp} - i_{cp}] \tag{5.1}$$

$$I_d = \frac{1}{\sqrt{3}}[i_{cp} - i_{bp}] \tag{5.2}$$

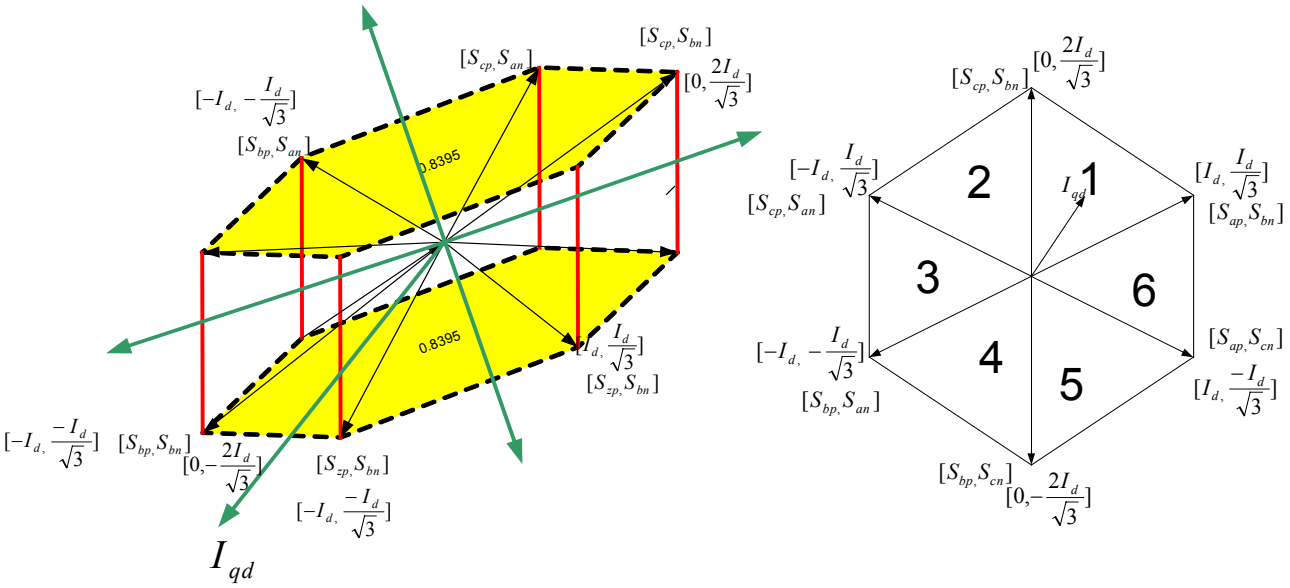
$$I_o = \frac{1}{3}[i_{ap} + i_{bp} + i_{cp}]. \tag{5.3}$$

For balanced condition $i_{ap} + i_{bp} + i_{cp} = 0$.

Table 5.2 Switching modes of three phase CSI and corresponding stationary reference frame q-d-o currents.

ON Device	**ON Device**	$\mathbf{i_{as}}$	$\mathbf{i_{bs}}$	$\mathbf{i_{cs}}$	$\mathbf{I_{qq}}$	$\mathbf{\sqrt{3}\ I_{dd}}$
S_{ap}	S_{bn}	I_d	$-I_d$	0	I_d	I_d
S_{ap}	S_{cn}	I_d	0	$-I_d$	I_d	$-I_d$
S_{bp}	S_{an}	$-I_d$	I_d	0	$-I_d$	$-I_d$
S_{bp}	S_{cn}	0	I_d	$-I_d$	0	$-2I_d$
S_{cp}	S_{an}	$-I_d$	0	I_d	$-I_d$	I_d
S_{cp}	S_{bn}	0	$-I_d$	I_d	0	$2I_d$
S_{ap}	S_{an}	0	0	0	0	0
S_{bp}	S_{bn}	0	0	0	0	0
S_{cp}	S_{cn}	0	0	0	0	0

In order to derive an expression for the modulating signals, a space vector approach is followed. Space vector scheme is to approximate the reference current (I^*_{qd}) with the two adjacent nonzero vectors (I_i and I_{i+1}) and one zero vector (I_7, I_8, I_9). Space vector is a regular hexagon with active states [$I_1 \ldots I_6$] placed around the six corners and the null states [I_7, I_8, I_9] placed at the center of the hexagon.



(a) (b)

Figure 5.2 Space vector diagram of CSI in (a) 3-D plane (b) 2-D plane to show the q-d-o currents produced by the switching states

Figure 5.2 (a) shows the 3-D plane of the space vector diagram with vectors projecting out of all the six edges of the hexagon Figure 5.2 (b) shows the 2-D plane of the projection of the six active states and the null states.

With a combination of some of the nine switching modes given in Table 5.1, an efficient solution is achieved by approximating I_{qd}^* with two nearest nonzero modes (vectors) and one of the null vectors. If $\mathbf{I_{qd}}^*$ lies in sector I

$$\mathbf{I_{qd}}^* = I_{qda}\, t_a + I_{qdb}\, t_b + I_{qd7}\, t_7 + I_{qd8}\, t_8 + I_{qd9}\, t_9 \qquad (5.4)$$

$$t_a + t_b + t_7 + t_8 + t_9 = 1 \text{ where } t_7 + t_8 + t_9 = t_0$$

$$\text{where } t_7 = \alpha\,(1 - t_a - t_b),\ t_8 = \beta(1 - t_a - t_b),\ t_9 = \gamma\,(1 - t_a - t_b), \qquad (5.5)$$

$$\alpha + \beta + \gamma = 1,\ \alpha\beta = \alpha\gamma = \beta\gamma = 0.$$

For Modulation index (M) $\leq$ 1 (linear modulation region), $t_a + t_b + t_o \leq 1$.

For Modulation index (M) $\geq$ 1 (Over modulation region), $t_a + t_b + t_o \geq 1$.

where t_a, t_b, t_7, t_8, t_9 represents the normalized times (with respect to the device switching period) and α, β, γ are the weighting factors. However, to avoid short-circuiting the input or output capacitor(s)–only one converter leg can be shorted at any time hence α, β, γ can either take values of one or zero.

5.2.2 Calculation of Switching Timing in each Sector

The time duration of the two adjacent nonzero vectors in each sector is calculated depending upon the magnitude and phase of the reference current.

Figure 5.3 shows the projections of two nonzero vectors in sector I and also gives the magnitude of the vectors in q-d-o reference frame. Since, the magnitude of the current synthesized by null state is zero hence from Equation (5.4) term $I_{qd7}\ t_7 + I_{qd8}\ t_8 + I_{qd9}\ t_9$ can be neglected and by separating Equation (5.4) into real and imaginary parts the expressions for t_a and t_b given as

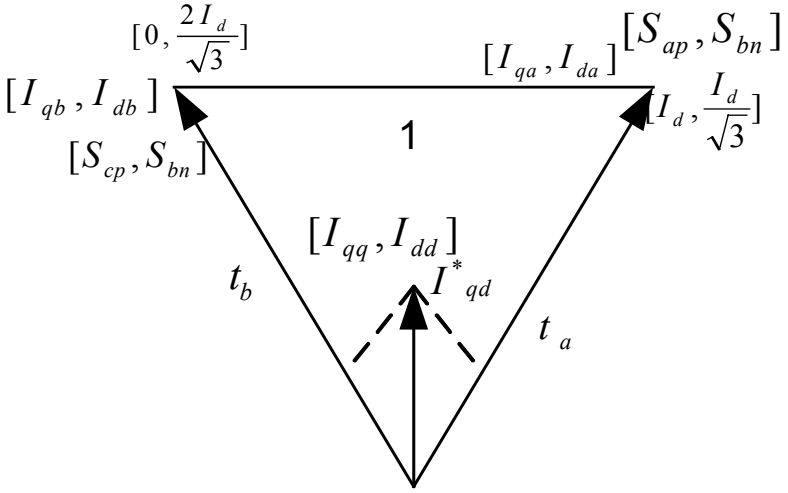


Figure 5.3 Sector I from the space vector of CSI.

$$\begin{bmatrix} I_{qq} \\ I_{dd} \end{bmatrix} = \begin{bmatrix} I_{qa} & I_{qb} \\ I_{da} & I_{db} \end{bmatrix} \begin{bmatrix} t_a \\ t_b \end{bmatrix}. \tag{5.6}$$

Now $\Delta = I_{qa} I_{db} - I_{da} I_{qb}$.

Hence

$$t_a = \frac{1}{\Delta} \begin{bmatrix} I_{qq} & I_{qb} \\ I_{dd} & I_{db} \end{bmatrix} = \frac{I_{qq} I_{db} - I_{qd} I_{dd}}{\Delta} \tag{5.7}$$

$$t_b = \frac{1}{\Delta} \begin{bmatrix} I_{qa} & I_{qq} \\ I_{da} & I_{dd} \end{bmatrix} = \frac{I_{qa} I_{dd} - I_{qq} I_{da}}{\Delta}. \tag{5.8}$$

It has been observed that the null states do not influence the values of t_a and t_b. Expressions for the normalized times (t_a, t_b) in each sector is derived as follows:

In sector I: Magnitude of currents in state I_1 are considered as I_{qa} and I_{da} and the next corresponding currents in state I_2 are taken as $I_{qb,}$ and I_{db} and the reference current to be generated is taken as $I_{qq,}$ and I_{dd}. If the current to be synthesized is in first sector Equations (5.7) and (5.8) are used to calculate the timings t_a and t_b.

Sector I

$$I_{qa} = I_d, \; I_{da} = \frac{I_d}{\sqrt{3}} \text{ , } I_{qb} = 0, I_{db} = \frac{2I_d}{\sqrt{3}}.$$

Now $\Delta = I_{qa} I_{db} - I_{da} I_{qb} = I_d . \frac{2I_d}{\sqrt{3}} - 0$, therefore $\Delta = \frac{2I_d^{\,2}}{\sqrt{3}}$

$$t_a = \frac{1}{\Delta}(I_{qq} I_{db} - I_{dd} I_{qb}) = \frac{(\frac{2I_d}{\sqrt{3}} I_{qq} - I_{dd}.0)}{\frac{2I_d^{\,2}}{\sqrt{3}}}, \; t_a = \frac{I_{qq}}{I_d}$$

and $t_b = [-\frac{I_{qq}}{2} + \frac{\sqrt{3}}{2} I_{dd}] \frac{1}{I_d}$

Sector II

$I_{qa} = 0,\ I_{da} = \frac{2I_d}{\sqrt{3}}$, $I_{qb} = -I_d, I_{db} = \frac{I_d}{\sqrt{3}}$.

Now $\Delta = I_{qa} I_{db} - I_{da} I_{qb} = 0 + I_d . \frac{2I_d}{\sqrt{3}}$, therefore $\Delta = \frac{2I_d^{\ 2}}{\sqrt{3}}$

$t_a = \frac{1}{\Delta}(I_{qq} I_{db} - I_{dd} I_{qb}) = \frac{(\frac{I_d}{\sqrt{3}} I_{qq} + I_{dd} I_d)}{\frac{2I_d^{\ 2}}{\sqrt{3}}}$, $t_a = [\frac{I_{qq}}{2} + \frac{\sqrt{3}}{2} I_{dd}] \frac{1}{I_d}$

and $t_b = [-I_{qq}] \frac{1}{I_d}$

Sector III

$I_{qa} = -I_d,\ I_{da} = \frac{I_d}{\sqrt{3}}, I_{qb} = -I_d,\ I_{db} = -\frac{I_d}{\sqrt{3}}$.

Now $\Delta = I_{qa} I_{db} - I_{da} I_{qb} = \frac{I_d^{\ 2}}{\sqrt{3}} + I_d . \frac{I_d}{\sqrt{3}}$, therefore $\Delta = \frac{2I_d^{\ 2}}{\sqrt{3}}$

$t_a = \frac{1}{\Delta}(I_{qq} I_{db} - I_{dd} I_{qb}) = \frac{(-\frac{I_d}{\sqrt{3}} I_{qq} + I_{dd} I_d)}{\frac{2I_d^{\ 2}}{\sqrt{3}}}$, $t_a = [-\frac{I_{qq}}{2} + \frac{\sqrt{3}}{2} I_{dd}] \frac{1}{I_d}$

and $t_b = [-\frac{I_{qq}}{2} - \frac{\sqrt{3}}{2} I_{dd}] \frac{1}{I_d}$

Sector IV

$I_{qa} = -I_d,\ I_{da} = -\frac{I_d}{\sqrt{3}}$, $I_{qb} = 0,\ I_{db} = -\frac{2I_d}{\sqrt{3}}$.

Now $\Delta = I_{qa}I_{db} - I_{da}I_{qb} = \frac{2I_d^{\,2}}{\sqrt{3}} + 0$, therefore $\Delta = \frac{2I_d^{\,2}}{\sqrt{3}}$

$$t_a = \frac{1}{\Delta}(I_{qq}I_{db} - I_{dd}I_{qb}) = \frac{(-\frac{2I_d}{\sqrt{3}}I_{qq} + I_{dd}.0)}{\frac{2I_d^{\,2}}{\sqrt{3}}} \text{ Simplifying } t_a = [-I_{qq}]\frac{1}{I_d}$$

and $t_b = [\frac{I_{qq}}{2} - \frac{\sqrt{3}}{2}I_{dd}]\frac{1}{I_d}$

Sector V

$I_{qa} = 0,\ I_{da} = -\frac{2I_d}{\sqrt{3}}$, $I_{qb} = I_d,\ I_{db} = -\frac{I_d}{\sqrt{3}}$.

Now $\Delta = I_{qa}I_{db} - I_{da}I_{qb} = 0 + \frac{2I_d^{\,2}}{\sqrt{3}}$, therefore $\Delta = \frac{2I_d^{\,2}}{\sqrt{3}}$

$$t_a = \frac{1}{\Delta}(I_{qq}I_{db} - I_{dd}I_{qb}) = \frac{(-\frac{I_d}{\sqrt{3}}I_{qq} + I_{dd}.I_d)}{\frac{2I_d^{\,2}}{\sqrt{3}}},\ t_a = [-\frac{I_{qq}}{2} + \frac{\sqrt{3}}{2}I_{dd}]\frac{1}{I_d}$$

and $t_b = [I_{qq}]\frac{1}{I_d}$

Sector VI

$I_{qa} = I_d,\ I_{da} = -\frac{I_d}{\sqrt{3}}$, $I_{qb} = I_d,\ I_{db} = \frac{I_d}{\sqrt{3}}$.

Now $\Delta = I_{qa}I_{db} - I_{da}I_{qb} = \frac{I_d}{\sqrt{3}} + \frac{I_d}{\sqrt{3}}$ therefore $\Delta = \frac{2I_d^{\,2}}{\sqrt{3}}$

$$t_a = \frac{1}{\Delta}(I_{qq}I_{db} - I_{dd}I_{qb}) = \frac{(\frac{I_d}{\sqrt{3}}I_{qq} - I_{dd}.I_d)}{\frac{2I_d^{\,2}}{\sqrt{3}}},\ t_a = [\frac{I_{qq}}{2} - \frac{\sqrt{3}}{2}I_{dd}]\frac{1}{I_d}$$

and $t_b = [-\frac{I_{qq}}{2} + \frac{\sqrt{3}}{2} I_{dd}] \frac{1}{I_d}$

The above calculated values of t_a and t_b times in all the six sectors are listed in Table 5.3.

Table 5.3 Device Switching times expressed in terms of q-d-o reference voltage.

	t_a	**t_b**
1	$\left[I_{qq}\right]\frac{1}{I_d}$	$\left[-\frac{I_{qq}}{2}+\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$
2	$\left[\frac{I_{qq}}{2}+\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$	$\left[-I_{qq}\right]\frac{1}{I_d}$
3	$\left[-\frac{I_{qq}}{2}+\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$	$\left[-\frac{I_{qq}}{2}-\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$
4	$\left[-I_{qq}\right]\frac{1}{I_d}$	$\left[\frac{I_{qq}}{2}-\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$
5	$\left[-\frac{I_{qq}}{2}+\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$	$\left[I_{qq}\right]\frac{1}{I_d}$
6	$\left[\frac{I_{qq}}{2}-\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$	$\left[-\frac{I_{qq}}{2}+\frac{\sqrt{3}}{2}I_{dd}\right]\frac{1}{I_d}$

5.2.3 Generalized Expression for t_a and t_b

Switching timings calculated in Table 5.3 can be expressed in a generalized form as in Equation (5.9) and (5.10) where I_m and γ are the magnitude and angle of the reference current.

$$t_a = \frac{I_m}{2}(\sqrt{3}\cos\xi - \sin\xi) \tag{5.9}$$

$$t_b = I_m \sin\xi \tag{5.10}$$

$\gamma = 60(n - \frac{1}{2}) + \xi$ Where $I_m = abs(I^*_{qd})$ and $\gamma = angle\left(I^*_{qd}\right)$ for n=1, 2, 3, 4, 5, 6

Switching times calculated in Table 5.3 can be expressed in terms of three phase reference currents after inverse transformation from stationary reference frame to a-b-c coordinates using the following equations:

$$f_a = f_q + f_o \tag{5.11}$$

$$f_b = \frac{-f_q}{2} - \frac{\sqrt{3}f_d}{2} - f_o \tag{5.12}$$

$$f_c = \frac{-f_q}{2} + \frac{\sqrt{3}f_d}{2} + f_o . \tag{5.13}$$

Substituting the values of t_a and t_b from Table 5.3 in Equations (5.11) to (5.13), Table 5.4 is obtained.

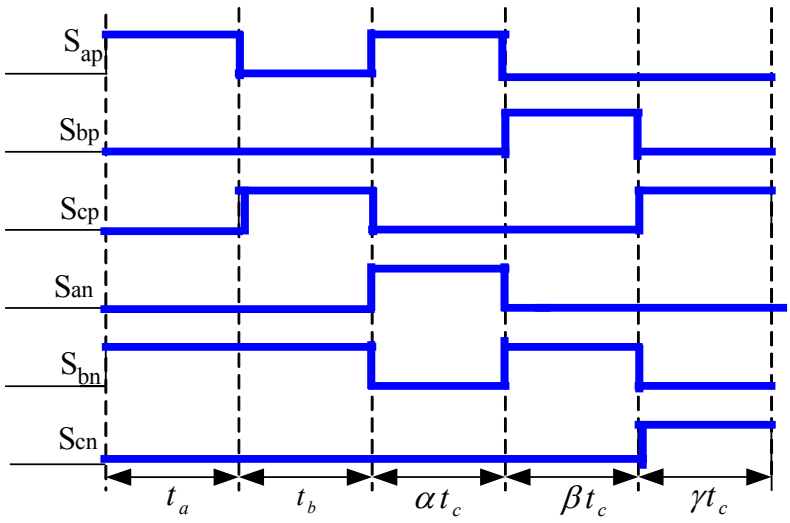
Table 5.4: Device switching times expressed in terms of reference line currents.

	$\mathbf{t_a}$	$\mathbf{t_b}$
1	$\frac{i_a}{I_d}$	$\frac{i_c}{I_d}$
2	$\frac{-i_b}{I_d}$	$\frac{-i_a}{I_d}$
3	$\frac{i_c}{I_d}$	$\frac{i_b}{I_d}$
4	$\frac{-i_a}{I_d}$	$\frac{-i_c}{I_d}$
5	$\frac{i_b}{I_d}$	$\frac{i_a}{I_d}$
6	$\frac{-i_c}{I_d}$	$\frac{-i_b}{I_d}$

Using the existence function of all the devices of the inverter from Figures 5.4 to 5.6 the expression for normalized switching times for which the devices will be turned ON in each sector is given. In other words it is defined as the duty ratio for the active states and the null states. These duty ratios for active and null states determine the time spend by a reference vector to generate the given current. Thus Table 5.5 expresses the normalized times for the device to be switched in each sector. Figure 5.5 shows the existence functions of all the six devices of the inverter when operating in first sector and the available times of each device. It observed that the average (the first term of the Fourier series expansion) of an existence function is equal to the sum of the normalized times each device is turned ON to realize a reference current.

Table 5.5 Normalized times for which the devices are on

Sectors	τ_{ap}	τ_{bp}	τ_{cp}	τ_{an}	τ_{bn}	τ_{cn}
1	$t_a + \alpha t_c$	βt_c	$t_b + \gamma t_c$	αt_c	$t_a + t_b + \beta t_c$	γt_c
2	αt_c	βt_c	$t_a + t_b + \gamma t_c$	$t_b + \alpha t_c$	$t_a + \beta t_c$	γt_c
3	αt_c	$t_b + \beta t_c$	$t_a + \gamma t_c$	$t_a + t_b + \alpha t_c$	βt_c	γt_c
4	αt_c	$t_a + t_b + \beta t_c$	γt_c	$t_a + \alpha t_c$	βt_c	$t_b + \gamma t_c$
5	$t_b + \alpha t_c$	$t_a + \beta t_c$	γt_c	αt_c	βt_c	$t_a + t_b + \gamma t_c$
6	$t_a + t_b + \alpha t_c$	βt_c	γt_c	αt_c	$t_b + \beta t_c$	$t_a + \gamma t_c$



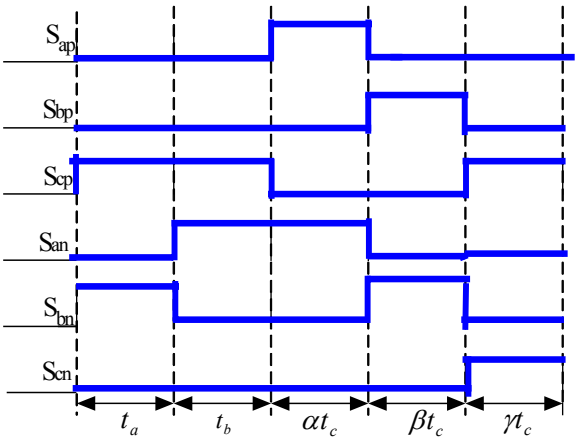
(I)

	S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}
t_a	1	0	0	0	1	0
t_b	0	0	1	0	1	0
αt_c	1	0	0	1	0	0
βt_c	0	1	0	0	1	0
γt_c	0	0	1	0	0	1

(II)

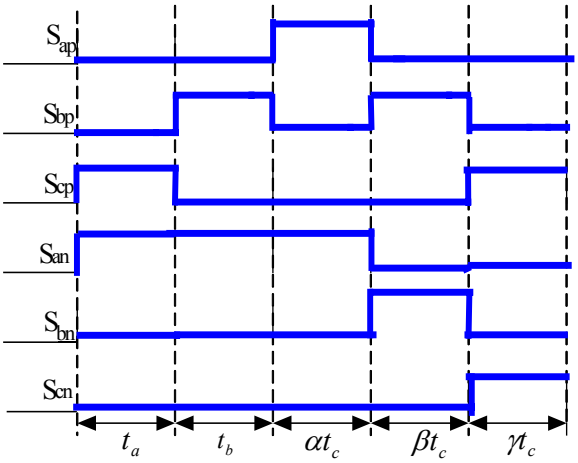
Figure 5.4 (I) and (II) Existence function of all the devices for operation in sector I

Sector II



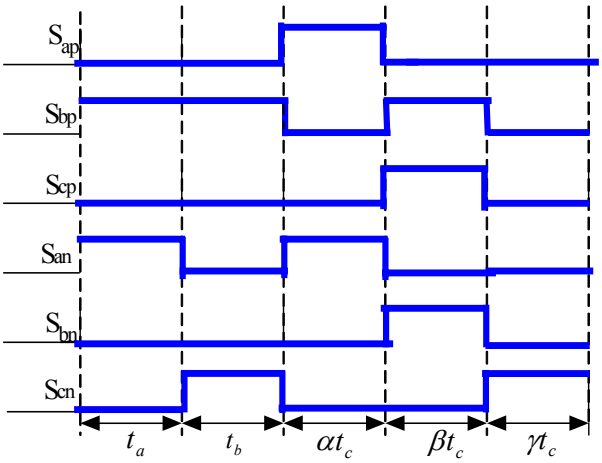
	Sap	Sbp	Scp	San	Sbn	Scn
t_a	0	0	1	0	1	0
t_b	0	0	1	1	0	0
αt_c	1	0	0	1	0	0
βt_c	0	1	0	0	1	0
γt_c	0	0	1	0	0	1

Sector III



	Sap	Sbp	Scp	San	Sbn	Scn
t_a	0	0	1	1	0	0
t_b	0	1	0	1	0	0
αt_c	1	0	0	1	0	0
βt_c	0	1	0	0	1	0
γt_c	0	0	1	0	0	1

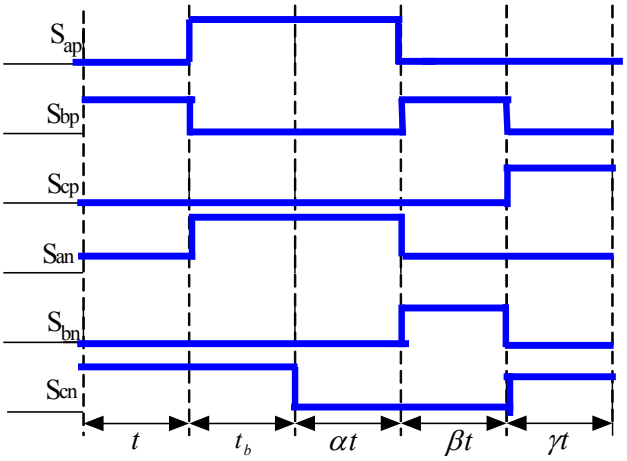
Sector IV



	Sap	Sbp	Scp	San	Sbn	Scn
t_a	0	1	0	1	0	0
t_b	0	1	0	0	0	1
αt_c	1	0	0	1	0	0
βt_c	0	1	0	0	1	0
γt_c	0	0	1	0	0	1

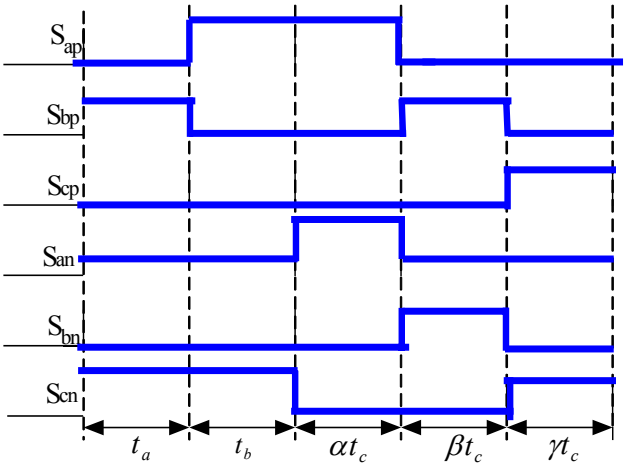
Figure 5.5 Existence functions of all the devices operating in sector II, III, IV

Sector V



	Sap	Sbp	Scp	San	Sbn	Scn
t_a	0	1	0	0	0	1
t_b	1	0	0	0	0	1
αt_c	1	0	0	1	0	0
βt_c	0	1	0	0	1	0
γt_c	0	0	1	0	0	1

Sector VI



	Sap	Sbp	Scp	San	Sbn	Scn
t_a	0	1	0	0	1	0
t_b	1	0	0	0	0	1
αt_c	1	0	0	1	0	0
βt_c	0	1	0	0	1	0
γt_c	0	0	1	0	0	1

Figure 5.6 Existence functions of all the devices operating in sector V, VI

5.2.4 Expressions for Modulating Signals

From the expressions in Table 5.5 the expressions of modulating signals for each device in each sector can be written by substituting the values of switching time from Table 5.4.

Sector I

Expressions for the existence function is given as

$$\tau_{ap} = t_a + \alpha t_c \,. \tag{5.14}$$

By substituting the values of t_a and t_c in Equation (5.14) expression for the modulating signal in Sector I for phase 'a' top device as

$$M_{ap} = i_{as} + \alpha(1 + i_{bs}) \tag{5.15}$$

where values of t_a and t_b are given from Table 5.4 and using $t_c = 1 - t_a - t_b$.. Expressions for modulating signals for other devices in sector I are given.

$\tau_{bp} = \beta t_c$ $\quad M_{bp} = \beta(1 + i_{bs})$

$\tau_{cp} = t_b + \gamma t_c$ $\quad M_{cp} = i_{cs} + \gamma(1 + i_{bs})$

$\tau_{an} = \alpha t_c$ $\quad M_{an} = \alpha(1 + i_{bs})$

$\tau_{bn} = t_a + t_b + \beta t_c$ $\quad M_{bn} = -i_{bs} + \beta(1 + i_{bs})$

$\tau_{cn} = \gamma t_c$ $\quad M_{cn} = \gamma(1 + i_{bs})$

Table 5.6 Expression for modulating signals for all the devices in all the six sectors

Sector	$\mathbf{M_{ap}}$ (τ_{ap})	$\mathbf{M_{an}}$ (τ_{an})	$\mathbf{M_{bp}}$ (τ_{bp})	$\mathbf{M_{bn}}$ (τ_{bn})	$\mathbf{M_{cp}}$ (τ_{cp})	$\mathbf{M_{cn}}$ (τ_{cn})
I	$i_{as} + \alpha\ (1+ i_{bs})$ $t_a + \alpha\ t_c$	$\alpha\ (1+ i_{bs})$ $\alpha\ t_c$	$\beta\ (1+ i_{bs})$ $\beta\ t_c$	$-i_{bs} + \beta\ (1+ i_{bs})$ $t_a + t_b + \beta t_c$	$i_{cs} + \gamma\ (1+ i_{bs})$ $t_b + \gamma\ t_c$	$\gamma\ (1+ i_{bs})$ $\gamma\ t_c$
II	$\alpha\ (1- i_{cs})$ $\alpha\ t_c$	$-i_{as} + \alpha\ (1-i_{cs})$ $t_b + \alpha\ t_c$	$\beta\ (1- i_{cs})$ $\beta\ t_c$	$-I_{bs} + \beta\ (1- i_{cs})$ $t_a + \beta t_c$	$i_{cs} + \gamma\ (1- i_{cs})$ $t_a + t_b + \gamma\ t_c$	$\gamma\ (1- i_{cs})$ $\gamma\ t_c$
III	$\alpha\ (1+ i_{as})$ $\alpha\ t_c$	$-i_{as} + \alpha\ (1+ i_{as})$ $t_a + t_b + \alpha\ t_c$	$i_{bs} + \beta(1+ i_{as})$ $t_b + \beta t_c$	$\beta\ (1+ i_{as})$ $\beta\ t_c$	$i_{cs} + \gamma\ (1+ i_{as})$ $t_a + \gamma\ t_c$	$\gamma\ (1+ i_{as})$ $\gamma\ t_c$
IV	$\alpha\ (1- i_{bs})$ $\alpha\ t_c$	$-i_{as} + \alpha\ (1-i_{bs})$ $t_a + \alpha\ t_c$	$i_{bs} + \beta\ (1- i_{bs})$ $t_a + t_b + \beta t_c$	$\beta\ (1- i_{bs})$ $\beta\ t_c$	$\gamma\ (1- i_{bs})$ $\gamma\ t_c$	$-i_{cs} + \gamma\ (1- i_{bs})$ $t_b + \gamma\ t_c$
V	$i_{as} + \alpha\ (1+ i_{cs})$ $t_b + \alpha\ t_c$	$\alpha\ (1+ i_{cs})$ $\alpha\ t_c$	$i_{bs} + \beta\ (1+ i_{cs})$ $t_a + \beta\ t_c$	$\beta\ (1+ i_{cs})$ $\beta\ t_c$	$\gamma\ (1+ i_{cs})$ $\gamma\ t_c$	$-i_{cs} + \gamma\ (1+i_{cs})$ $t_a + t_b + \gamma\ t_c$
VI	$i_{as} + \alpha\ (1- i_{as})$ $t_a + t_b + \alpha\ t_c$	$\alpha\ (1- i_{as})$ $\alpha\ t_c$	$\beta\ (1- i_{as})$ $\beta\ t_c$	$-I_{bs} + \beta\ (1- i_{as})$ $t_b + \beta\ t_c$	$\gamma\ (1- i_{as})$ $\gamma\ t_c$	$-i_s + \gamma\ (1- i_{as})$ $t_a + \gamma\ t_c$

Expression for different Discontinuous Modulators (DCM) for the device in all the six sectors is listed in Table 5.7. It is conspicuous from Table 5.6 that large sets of discontinuous modulation signal waveforms are possible by selecting different values for α, β, γ. Possible combinations of α, β, γ are listed in Table 5.7.

Table 5.7 Possible combination values for α, β, γ

DCM 1	DCM 2	DCM 3
α = 1 in sectors 3 and 6 β = 1 in sectors 1 and 4 γ = 1 in sectors 2 and 5	α = 1 in sectors 2 and 5 β = 1 in sectors 3 and 6 γ = 1 in sectors 1 and 4	α = 1 in sectors 1 and 4 β = 1 in sectors 2 and 5 γ = 1 in sectors 3 and 6
DCM 4	DCM 5	DCM 6
α = 1 in sectors 3 and 6 β = 1 in sectors 2 and 5 γ = 1 in sectors 1 and 4	α = 1 in sectors 2 and 5 β = 1 in sectors 1 and 4 γ = 1 in sectors 3 and 6	α = 1 in sectors 1 and 4 β = 1 in sectors 3 and 6 γ = 1 in sectors 2 and 5

Table 5.8 Expressions for M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} for $\alpha = 1$ in sectors 3 & 6 $\beta = 1$ in 1 & 4 $\gamma = 1$ in 2 & 5 (DCM 1)

Sector	M_{ap}	M_{an}	M_{bp}	M_{bn}	M_{cp}	M_{cn}
0- 60 °	i_{as}	0	$1+i_{bs}$	1	i_{cs}	0
60° - 120 °	0	$-i_{as}$	0	$-i_{bs}$	1	$1-i_{cs}$
120°- 180 °	$1+i_{as}$	1	i_{bs}	0	i_{cs}	0
180 °- 240 °	0	$-i_{as}$	1	$1-i_{bs}$	0	$-i_{cs}$
240 °- 300 °	i_{as}	0	i_{bs}	0	$1+i_{cs}$	1
300°- 360 °	1	$1-i_{as}$	0	$-i_{bs}$	0	$-i_{cs}$

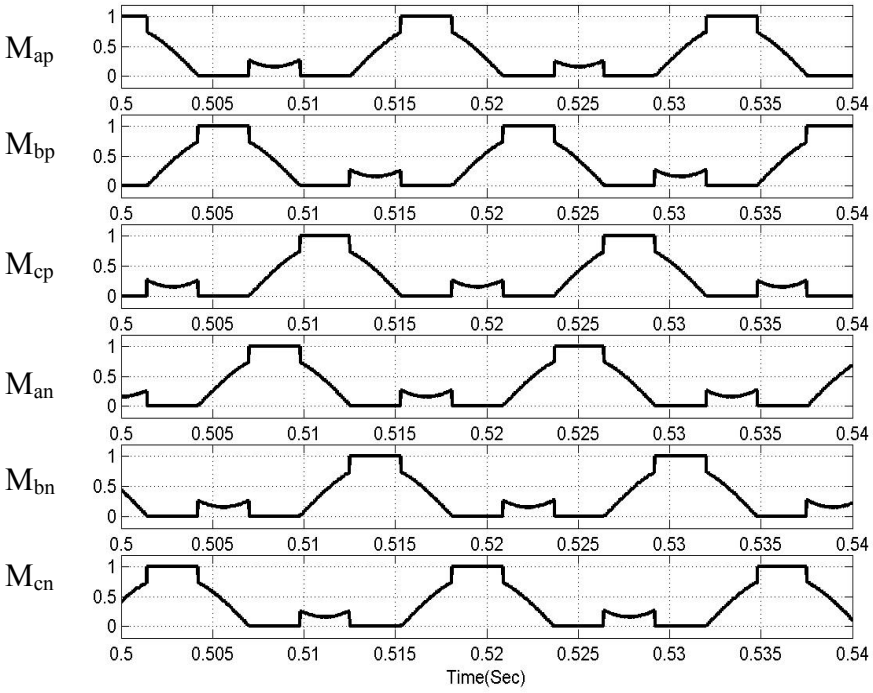


Figure 5.7 Modulating signal for six devices at $\alpha = 1$ in sectors 3 & 6, $\beta = 1$ in 2 & 5, $\gamma = 1$ in 1 & 4 (DCM 1)

Table 5.9 Expressions for M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} for $\alpha = 1$ in sectors 2 & 5 $\beta = 1$ in 3 & 6 $\gamma = 1$ in 1 & 4 (DCM 2)

Sector	M_{ap}	M_{an}	M_{bp}	M_{bn}	M_{cp}	M_{cn}
0- 60 °	i_{as}	0	0	$-I_{bs}$	$1-i_{as}$	$1+i_{bs}$
60° - 120 °	$1-i_{cs}$	$1+i_{bs}$	0	$-I_{bs}$	i_{cs}	0
120°- 180 °	0	$-i_{as}$	$1-i_{cs}$	$1+I_{as}$	i_{cs}	0
180 °- 240 °	0	$-i_{as}$	i_{bs}	0	$1-i_{bs}$	$1+i_{as}$
240 °- 300 °	$1-i_{bs}$	1+ics	i_{bs}	0	0	$-i_{cs}$
300°- 360 °	i_{as}	0	$1-i_{as}$	$1+i_{cs}$	0	$-i_{cs}$

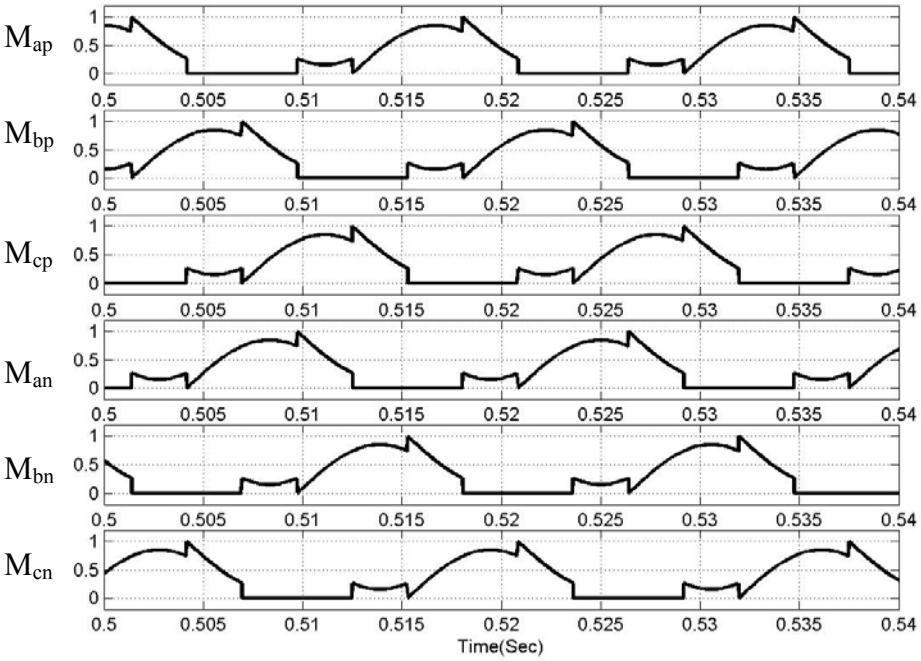


Figure 5.8 Modulating signals for six devices at $\alpha = 1$ in sectors 2 and 5, $\beta = 1$ in sectors 3 and 6, $\gamma = 1$ in sectors 1 and 4 (DCM 2)

Table 5.10 Expressions for M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} for $\alpha = 1$ in sectors 1 & 4 $\beta = 1$ in 2 & 5 $\gamma = 1$ in 3 & 6 (DCM 3)

Sector	$\mathbf{M_{ap}}$	$\mathbf{M_{an}}$	$\mathbf{M_{bp}}$	$\mathbf{M_{bn}}$	$\mathbf{M_{cp}}$	$\mathbf{M_{cn}}$
0- 60 °	$1-i_{cs}$	$1+i_{bs}$	0	$-i_{bs}$	i_{cs}	0
60° - 120 °	0	$-i_{as}$	$1-i_{cs}$	$1+i_{as}$	i_{cs}	0
120°- 180 °	0	$-i_{as}$	i_{bs}	0	$1-i_{bs}$	$1+i_{as}$
180 °- 240 °	$1-i_{bs}$	$1+i_{cs}$	i_{bs}	0	0	$-i_{cs}$
240 °- 300 °	i_{as}	0	$1-I_{as}$	$1+i_{cs}$	0	$-i_{cs}$
300°- 360 °	i_{as}	0	0	$-i_{bs}$	$1-i_{as}$	$1+i_{bs}$

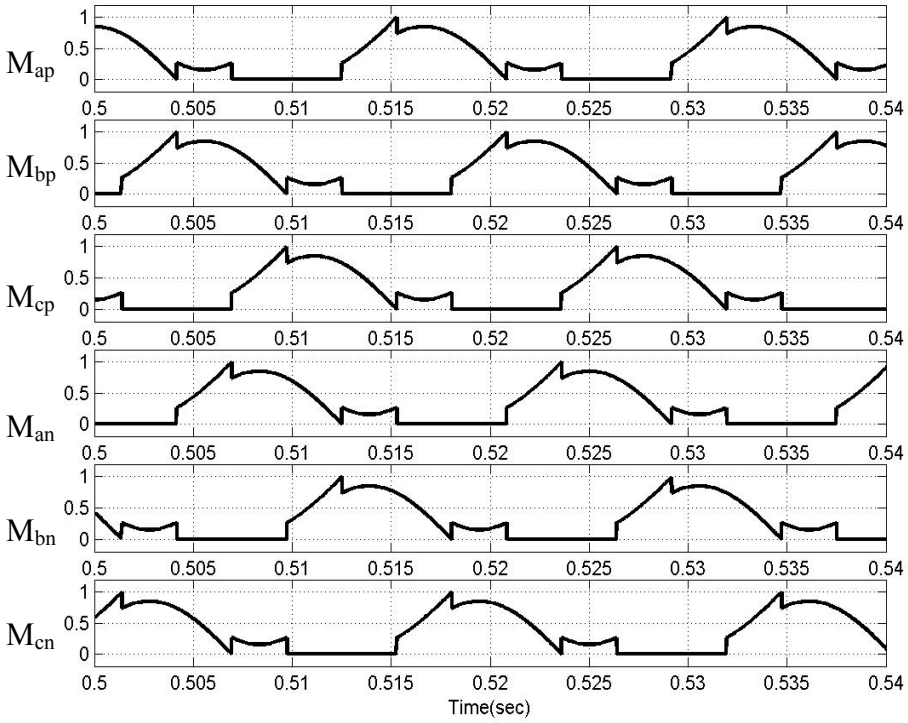


Figure 5.9 Modulating signals for six devices at $\alpha = 1$ in sectors 1 and 4, $\beta = 1$ in sectors 2 and 5, $\gamma = 1$ in sectors 3 and 6 (DCM 3)

Table 5.11 Expressions for M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} for $\alpha = 1$ in sectors 3 & 6 $\beta = 1$ in 2 & 5 $\gamma = 1$ in 1 & 4 (DCM 4)

Sector	M_{ap}	M_{an}	M_{bp}	M_{bn}	M_{cp}	M_{cn}
0- 60 °	i_{as}	0	0	$-i_{bs}$	$1-i_{as}$	$1+i_{bs}$
60° - 120 °	0	$-i_{as}$	$1-i_{cs}$	$1+i_{as}$	i_{cs}	0
120°- 180 °	$1+i_{as}$	1	i_{bs}	0	i_{cs}	0
180 °- 240 °	0	$-i_{as}$	i_{bs}	0	$1-i_{bs}$	$1+i_{as}$
240 °- 300 °	i_{as}	0	$1-i_{as}$	$1+i_{cs}$	0	$-i_{cs}$
300°- 360 °	1	$1-i_{as}$	0	$-i_{bs}$	0	$-i_{cs}$

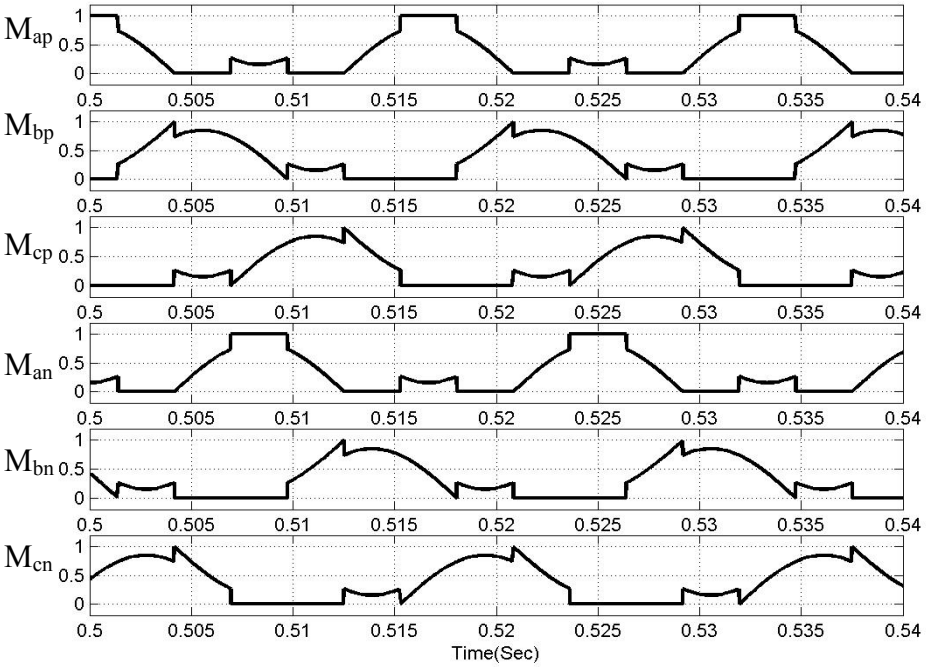


Figure 5.10 Modulating signals for six devices at $\alpha = 1$ in sectors 3 and 6 $\beta = 1$ in sectors 2 and 5, $\gamma = 1$ in sectors 1 and 4 (DCM 4)

Table 5.12 Expressions for M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} for $\alpha = 1$ in sectors 2 & 5 $\beta = 1$ in 1 & 4 $\gamma = 1$ in 3 & 6 (DCM 5)

Sector	M_{ap}	M_{an}	M_{bp}	M_{bn}	M_{cp}	M_{cn}
0- 60 °	i_{as}	0	$1+i_{bs}$	1	i_{cs}	0
60° - 120 °	$1-i_{cs}$	$1+i_{bs}$	0	$-i_{bs}$	i_{cs}	0
120°- 180 °	0	$-i_{as}$	i_{bs}	0	$1-i_{bs}$	$1+i_{as}$
180 °- 240 °	0	$-i_{as}$	1	$1-i_{bs}$	0	$-i_{cs}$
240 °- 300 °	$1-i_{bs}$	$1+i_{cs}$	i_{bs}	0	0	$-i_{cs}$
300°- 360 °	i_{as}	0	0	$-i_{bs}$	$1-i_{as}$	$1+i_{bs}$

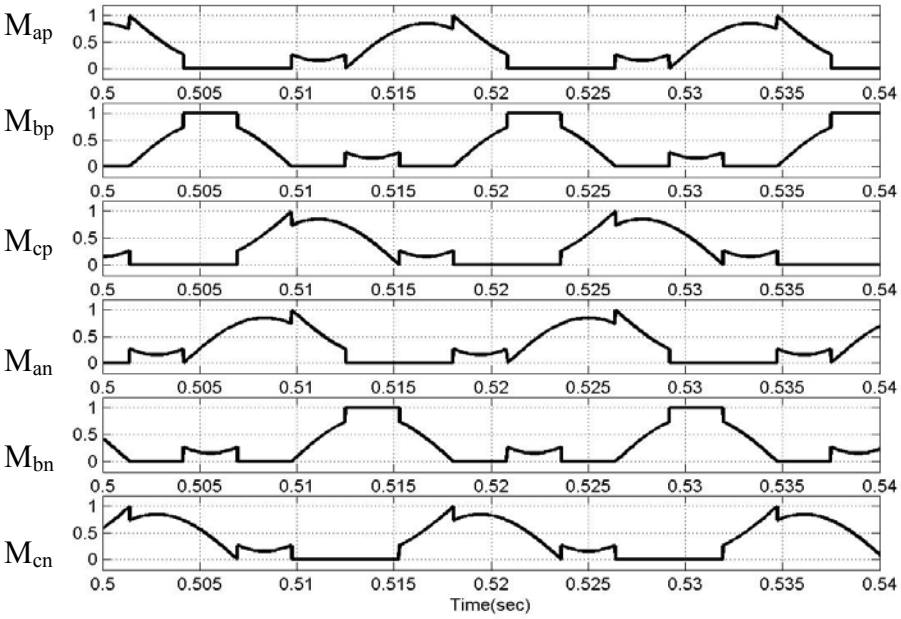


Figure 5.11 Modulating signal for six devices at $\alpha = 1$ in sectors 2 and 5, $\beta = 1$ in sectors 1 and 4, $\gamma = 1$ in sectors 3 and 6n (DCM 5)

Table 5.13 Expressions for M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} for $\alpha = 1$ in sectors 1 & 4 $\beta = 1$ in 3 & 6 $\gamma = 1$ in 2 & 5 (DCM 6)

Sector	$\mathbf{M_{ap}}$	$\mathbf{M_{an}}$	$\mathbf{M_{bp}}$	$\mathbf{M_{bn}}$	$\mathbf{M_{cp}}$	$\mathbf{M_{cn}}$
0- 60 °	$1-i_{cs}$	$1+i_{bs}$	0	$-i_{bs}$	i_{cs}	0
60° - 120 °	0	$-i_{as}$	0	$-i_{bs}$	1	$1-i_{cs}$
120°- 180 °	0	$-i_{as}$	$1-i_{cs}$	$1+i_{as}$	i_{cs}	0
180 °- 240 °	$1-i_{bs}$	$1+i_{cs}$	i_{bs}	0	0	$-i_{cs}$
240 °- 300 °	i_{as}	0	i_{bs}	0	$1+i_{cs}$	1
300°- 360 °	i_{as}	0	$1-i_{as}$	$1+i_{cs}$	0	$-i_{cs}$

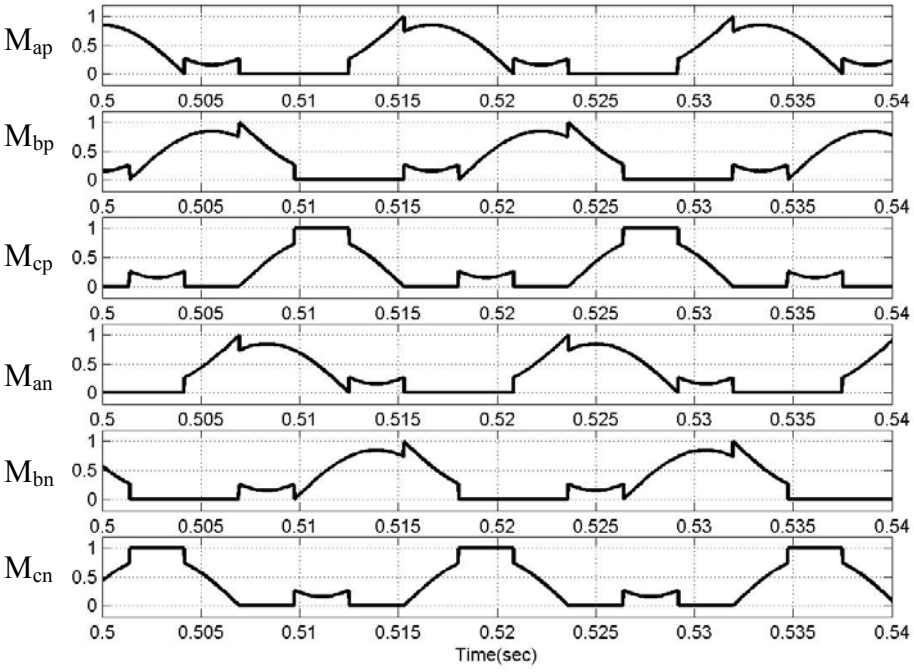


Figure 5.12 Modulating signal for six devices at $\alpha = 1$ in sectors 3 & 6 $\beta = 1$ in 2 & 5 $\gamma = 1$ in 1 & 4 (DCM 6)

Figures 5.7 to 5.12 show different sets of modulating signals generated using Table 5.7. It can be seen that first three sets of modulating signals DCM1, DCM2, DCM3 show symmetry among all the six signals. In each of these set of modulating signals the top and the bottom three signals are having a phase difference of 120^{o} in between them and the there is a difference of 180^{o} between the top and the bottom device of the same phase.

But the other three set of signals DCM4, DCM5, DCM6 does not show any symmetry among them only the signals in the same leg are phase shifted by 180^{0}, but the signals for the top three devices and the bottom devices does not show any sought of symmetry hence these set of modulating signals are discarded in using for sine triangle implementation. It is seen that switching pattern obtained by comparison of the DCM1, DCM2, DCM3 modulating signals with a high frequency triangle definitely will not satisfy the constraints for a CSI as mentioned in Chapter 3. An algorithm is proposed for using the above modulating signals through sine triangle comparison technique in order to modulate current source inverter.

5.3 Algorithm for Removing Device Shorting

The main aim of this algorithm is to make the switching pattern suitable to modulate the current source inverter; i.e., they have to satisfy constrains of CSI.

$$S_{ap} + S_{bp} + S_{cp} = 1 \ , \ S_{an} + S_{bn} + S_{cn} = 1 \tag{5.16}$$

$$S_{ap}.S_{bp} = 0 \, , \; S_{bp}.S_{cp} = 0 \, , \; S_{ap}.S_{cp} = 0 \text{ also } S_{an}.S_{bn} = 0 \, , \; S_{bn}.S_{cn} = 0 \, , \; S_{an}.S_{cn} = 0 \tag{5.17}$$

The proposed algorithm uses the maximum, minimum, and medium of the reference signals to sort the states in order to attain the desired objective [B.26].

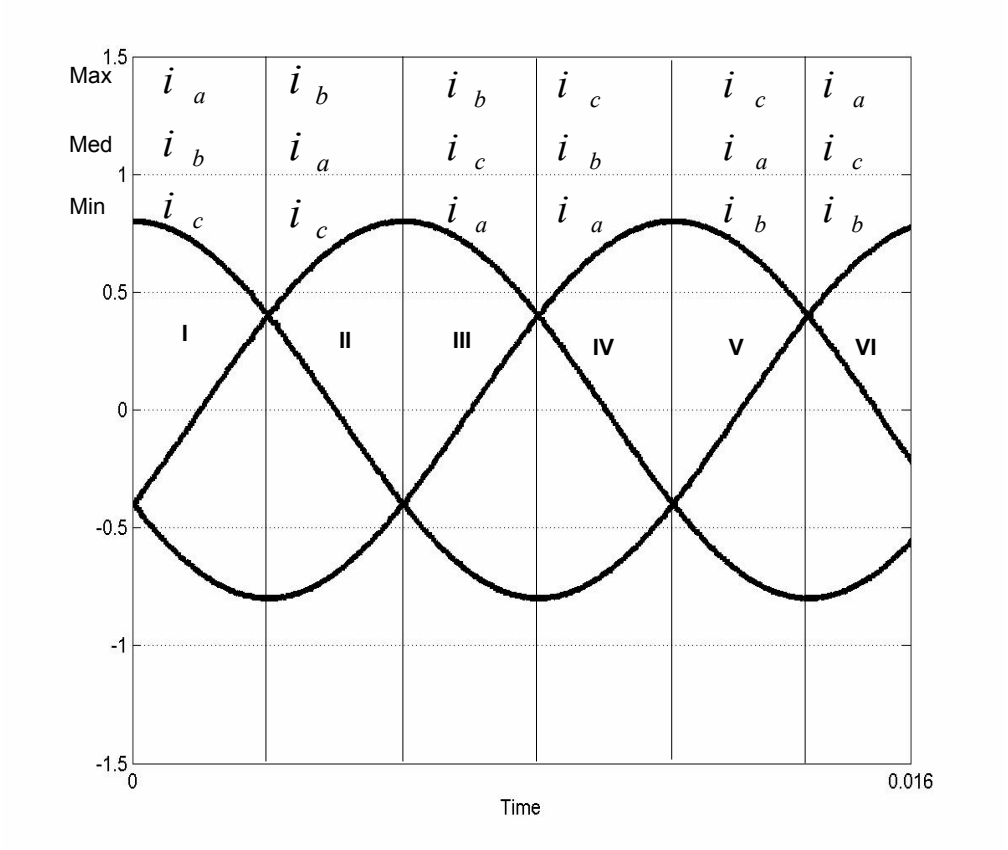


Figure 5. 13 The Maximum, Medium, Minimum regions of the reference currents.

Let M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} represent the modulating signals and S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn} , S_{cn} represent the switching function of all the six devices, let's consider the region I in which i_a is maximum among the three reference currents, and i_b is medium and i_c is minimum.

As i_a is the maximum value in this sector $S_{ap} = 1$ if M_{ap} is greater than the triangle, and $S_{ap} = 0$ if M_{ap} is less than the triangle. As i_b is the medium value in this sector then $S_{bp} = 1$ if M_{ap} is less than the triangle and $S_{bp} = 0$ if M_{ap} is greater than triangle, $S_{cp} = 0$. And for the bottom devices since i_c is the minimum value in this sector $S_{cn} = 1$ if M_{cn} is greater than the triangle and $S_{cn} = 0$ if M_{cn} is less than the triangle. As i_b is the medium value $S_{bn} = 1$ if the M_{cn} is less the triangle and $S_{bn} = 1$ if M_{cn} is greater than the triangle, and $S_{an} = 0$. This procedure is followed in all the regions. Table 5.14 shows the currents that are maximum, medium, and minimum in all the sectors for one period. The above algorithm takes care of the condition that no two devices in the top and no two devices in the bottom are switched at the same time and at least one device is switched ON in both top and bottom.

Table 5.14 Maximum, Minimum and Medium values of reference current in all the sectors.

	Sector I	Sector II	Sector III	Sector IV	Sector V	Sector VI
Maximum	i_a	i_b	i_b	i_c	i_c	i_a
Medium	i_b	i_a	i_c	i_b	i_a	i_c
Minimum	i_c	i_c	i_a	i_a	i_b	i_b

The above stated algorithm can be represented in the form of a flowchart as shown in Figures 5.14 and 5.15.

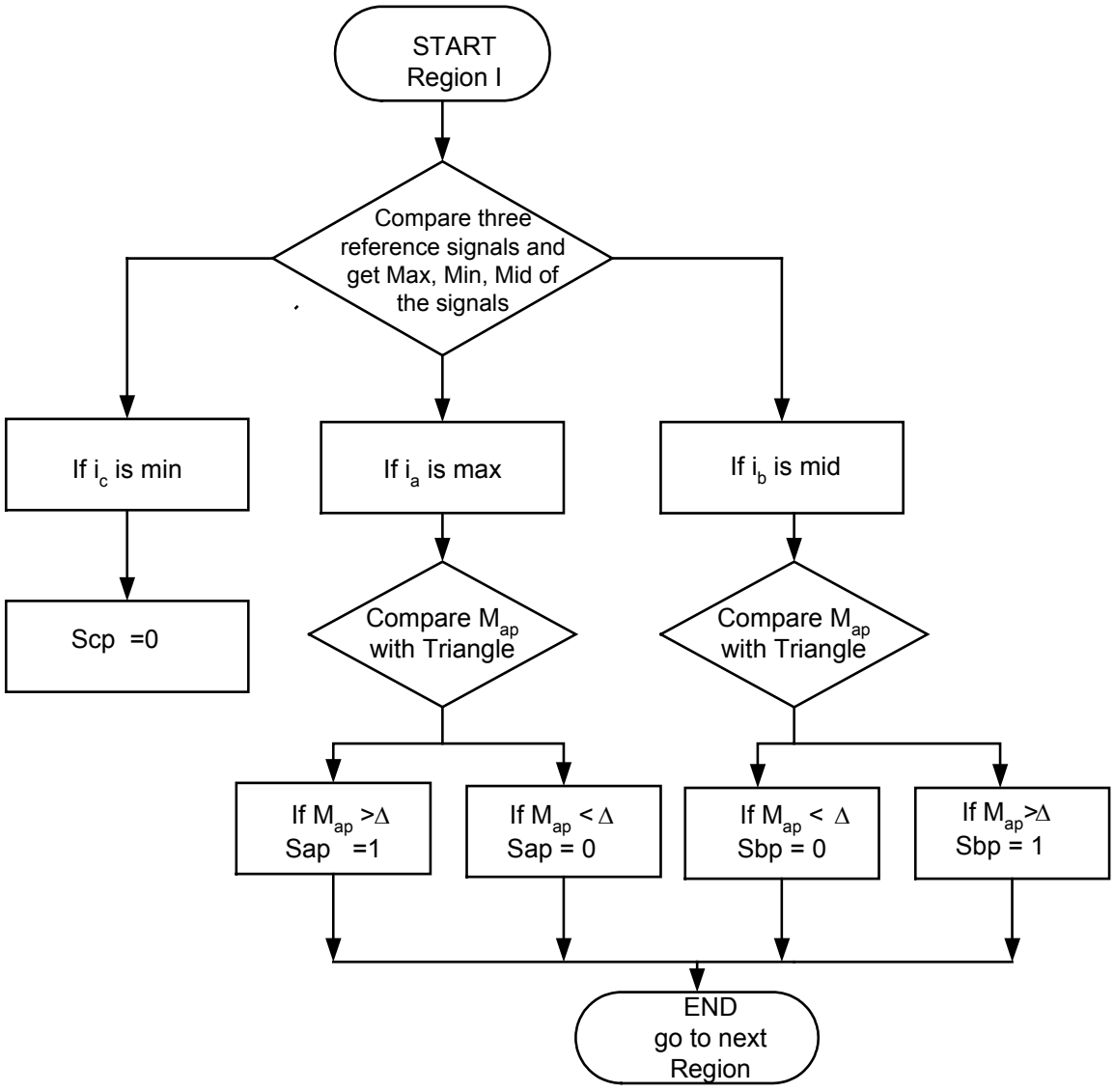


Figure 5.14 Flowchart of the proposed algorithm for top devices.

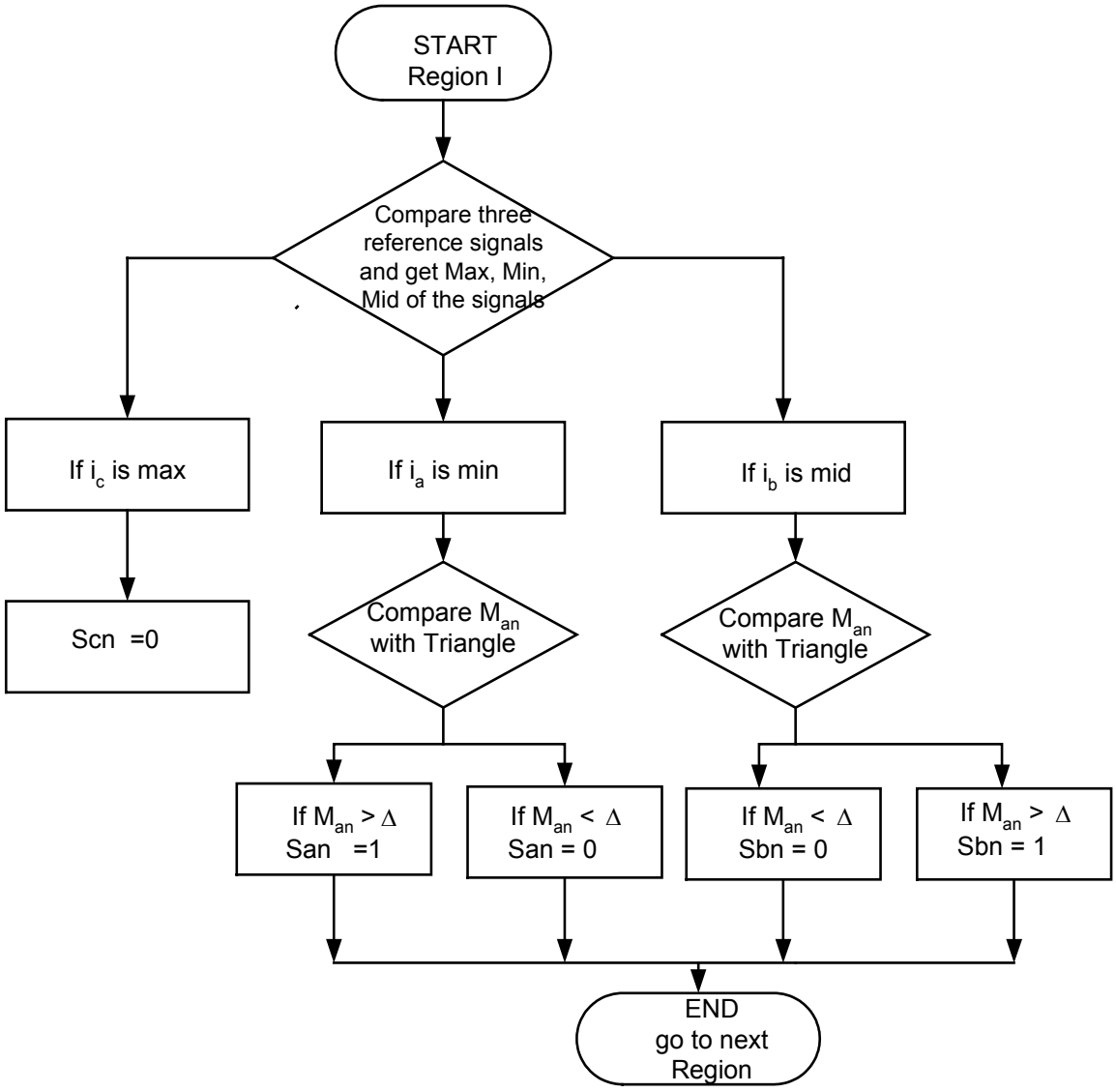


Figure 5.15 Flowchart of the proposed algorithm for bottom devices.

Table 5.15 Possible active and null states using above algorithm

Sap	Sbp	Scn	Sbn	STATE
1	0	0	1	Active
0	1	0	1	NULL
1	0	1	0	Active
0	1	1	0	Active

The algorithm can be summarized as follows:

In region I

I_{as} is maximum then $S_{ap} = 1$ if $M_{ap} > \Delta$ else $S_{an} = 0$.

I_{bs} is medium then $S_{bp} = 1$ if $M_{ap} < \Delta$ else $S_{bn} = 0$.

I_{cs} is minimum then $S_{cn} = 1$ if $M_{cn} > \Delta$ else $S_{cp} = 0$.

I_{bs} is medium then $S_{bn} = 1$ if $M_{cn} < \Delta$ else $S_{bp} = 0$.

The possible states that can be attained using the above-mentioned algorithm are listed in Table 5.15. It is seen that there is a possibility of a null state in between two active states, which is an acceptable combination.

5.4 Layout of the Practical Scheme

Figure 5.16 shows the design layout for implementation algorithm proposed in section 5.3. The six independent switching pattern obtained from the PWM generators, EVA and EVB event managers of the DSP, are recombined to attain the switching pattern, which satisfies the CSI constraints as explained in Chapter 3. The switching

output from the DSP, are passed through the simple OR, AND gates to follow the algorithm proposed in section 5.4. In order to implement the above algorithm nine high pulses are used to sort switching pattern. These pulses are high depending upon the reference signals maximum medium, minimum values. Sa_{max}, Sb_{max}, $Sc_{max,}$ are the maximum pulses, these pulses are high when the reference a-b-c currents are maximum. Similarly Sa_{mid}, Sb_{mid}, Sc_{mid}, Sa_{min}, Sb_{min}, Sc_{min} are high with the reference a-b-c currents maximum and minimum values. Since the Digital to Analog converter of the DSP has only four output ports, an external hardware to generate all nine pulses is used ; i.e., Sa_{max} , $Sb_{max,}$ $Sb_{max,}$ Sa_{min} , and Sb_{min} are generated using the following conditions:

$Sa_{max} + Sb_{max} + Sc_{max} = 1$ and $Sa_{min} + Sb_{min} + Sc_{min} = 1$ and using the maximum and medium pulses, medium pulses are generated using the external logic gates. These pulses are multiplied by the switching pattern and added together according to the algorithm to sort the feasible states.

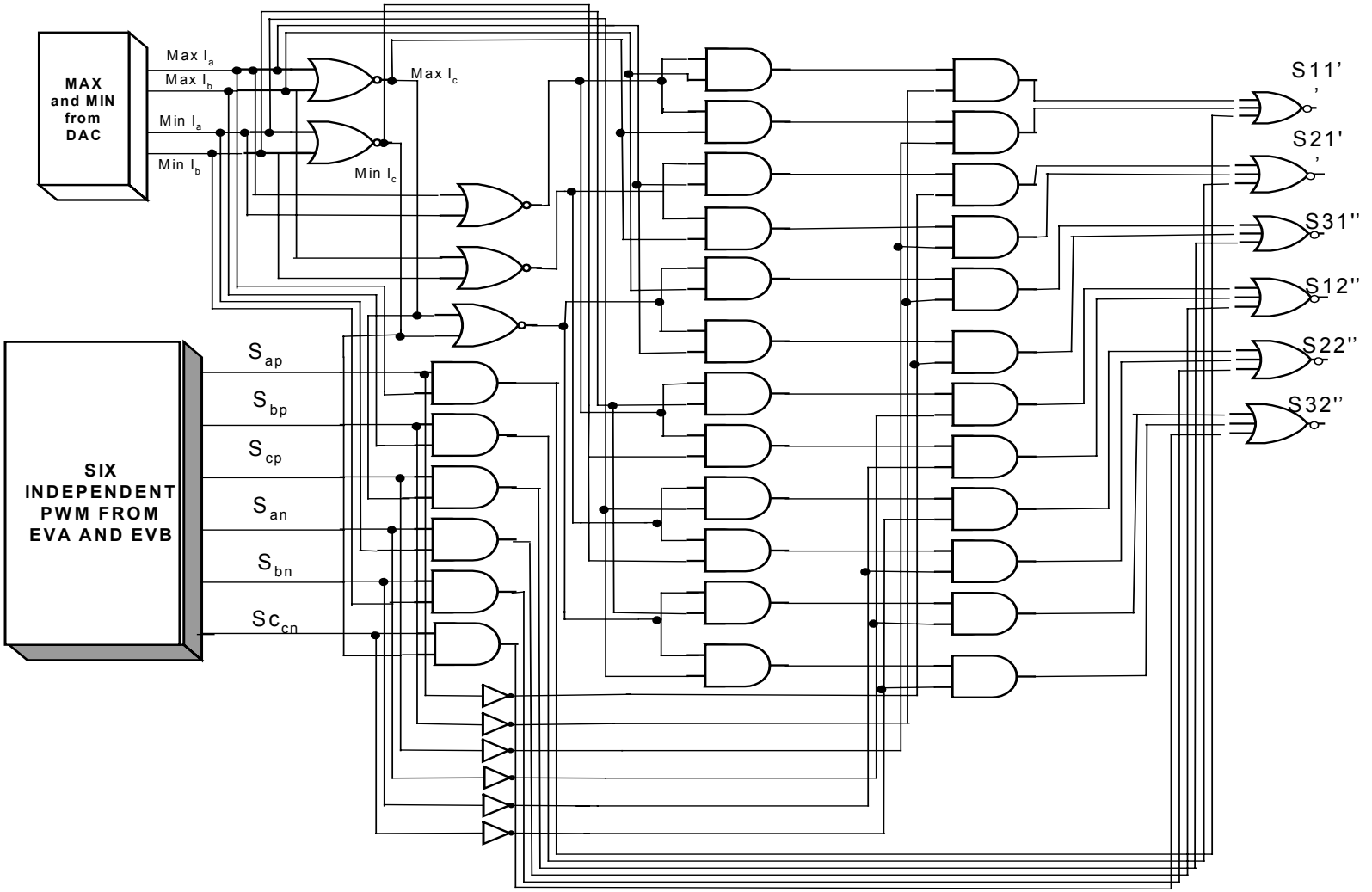


Figure 5.16 Circuit layouts for the practical implementation of the proposed algorithm.

5.5 Space Vector Modulation SVPWM

This modulation scheme directly determines the time duration of each devices, which has to be turned ON, so as to synthesis desired reference currents. From Table 5.1 there are six active states and three null states for a CSI. The stationary reference frame q-d-o currents of the switching modes are given in Table 5.2. It can be visualized as a regular hexagon by dividing it into six equal sectors denotes by I, II, III, IV, V, VI in Figure 5.17 The reference current vector in any sector can be referred to as $I^*_{qd.}$

The space vector modulation technique is based on the fact that every vector I_{qd}^* inside the hexagon can be expressed as a weighted average combination of the two adjacent active space vectors and the null-state vector I_7, I_8, I_9. Therefore, in each cycle the desired reference vector may be achieved by switching between these five states.

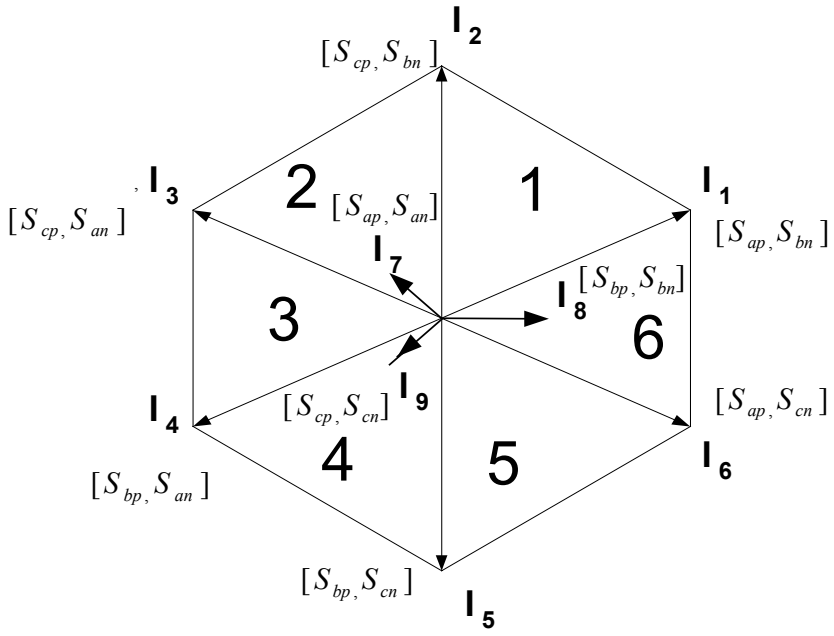


Figure 5.17 Space vector diagram of the CSI showing all the six active states.

From Figure 5.17, assuming I_{qd}^* to be lying in sector k, the adjacent active vectors are I_k and I_{k+1}, where K+1 is set to 1 for K = 6. In order to obtain an optimum harmonic performance and the minimum switching frequency for each of the power devices, the state sequence is arranged such that switching of only one inverter leg performs the transition from one state to the next. This condition is met if the sequence begins with one zero-state and the inverter switches are reversed, ending with the first zero –state. If for instance, the reference vector sits in sector I, the state sequence has to be I_7 I_1 I_2 I_8 I_2 I_1 I_0…. whereas in sector IV it is …I_8 I_5 I_4 I_9 I_4 I_5 I_0 … .The central part of the space vector modulation strategy is the computation of both the active and zero state switching times for each modulation cycle, which may be calculated by equating the average current to the desired value. Null times t_o have to be sequenced in every sector, this sequencing is not necessary in carrier-based PWM technique. Synthesizing the reference current I_{qd}^* it can be defined as in equations (5.4) and (5.5). Active states spend t_a, and t_b time and the null state spend the times t_7, t_8, t_9. The duration of the different null states is depended upon the values of α, β, γ.

Different values of α, β, γ give different possible switching sequences. Hence from Tables 5.7 six different modulators for different possibilities of α, β, γ.can be obtained. Switching times in all these possibilities and number of switch transitions in one cycle are listed in Tables 5.16-5.27.

Table 5.16 Switching times of the devices which are turned ON for DCM 1

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	t_c	t_b	0	1	0
2	0	0	1	t_b	t_a	t_c
3	t_c	t_b	t_a	1	0	0
4	0	1	0	t_a	t_c	t_b
5	t_b	t_a	t_c	0	0	1
6	1	0	0	t_c	t_b	t_a

Table 5.17 Number of switch transitions for DCM 1

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_c	0	1	0	0	1	0	1
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_c	0	0	1	0	0	1	1
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_c	1	0	0	1	0	0	1
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_c	0	1	0	0	1	0	1
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_c	0	0	1	0	0	1	1
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_c	1	0	0	1	0	0	1
t_b	1	0	0	0	1	0	1

Table 5.18 Switching times of the devices, which are turned ON for DCM 2

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b+t_c	0	t_a+t_b	t_c
2	t_c	0	t_a+t_b	t_b+t_c	t_a	0
3	0	t_b+t_c	t_a	t_a+t_b	t_c	0
4	0	t_a+t_b	t_c	t_a	0	t_b+t_c
5	t_b+t_c	t_a	0	t_c	0	t_a+t_b
6	t_a+t_b	t_c	0	0	t_b+t_c	t_a

Table 5.19 Number of switch transitions for DCM 2

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_c	0	0	1	0	0	1	2
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_c	1	0	0	1	0	0	2
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_c	0	1	0	0	1	0	2
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_c	0	0	1	0	0	1	2
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_c	1	0	0	1	0	0	2
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_c	0	1	0	0	1	0	2
t_b	1	0	0	0	1	0	1

Table 5.20 Switching times of the devices, which are turned ON for DCM 3

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a+tc	0	t_b	t_c	t_a+t_b	0
2	0	t_c	t_a+t_b	t_b	t_a+t_c	0
3	0	t_b	t_a+t_c	t_a+t_b	0	t_c
4	t_c	t_a+t_b	0	t_a+t_c	0	t_b
5	t_b	t_a+t_c	0	0	t_c	t_a+t_b
6	t_a+t_b	0	t_c	0	t_b	t_a+t_c

Table 5.21 Number of switch transitions for DCM 3

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_c	1	0	0	1	0	0	1
t_b	0	0	1	0	1	0	2
t_a	0	0	1	0	1	0	0
t_c	0	1	0	0	1	0	1
t_b	0	0	1	1	0	0	2
t_a	0	0	1	1	0	0	0
t_c	0	0	1	0	0	1	1
t_b	0	1	0	1	0	0	2
t_a	0	1	0	1	0	0	0
t_c	1	0	0	1	0	0	1
t_b	0	1	0	0	0	1	2
t_a	0	1	0	0	0	1	0
t_c	0	1	0	0	1	0	1
t_b	1	0	0	0	0	1	2
t_a	1	0	0	0	0	1	0
t_c	0	0	1	0	0	1	1
t_b	1	0	0	0	1	0	2

Table 5.22 Switching times of the devices which are turned ON in DCM 4

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b+t_c	0	t_a+t_b	t_c
2	0	t_c	t_a+t_b	t_b	t_a+t_c	0
3	t_c	t_b	t_a	1	0	0
4	0	t_a+t_b	t_c	t_a	0	t_b+t_c
5	t_b	t_a+t_c	0	0	t_c	t_a+t_b
6	1	0	0	t_c	t_b	t_a

Table 5.23 Number of switch transitions for DCM 4

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_c	0	0	1	0	0	1	2
t_b	0	0	1	0	1	0	
t_a	0	0	1	0	1	0	0
t_c	0	1	0	0	1	0	1
t_b	0	0	1	1	0	0	2
t_a	0	0	1	1	0	0	0
t_c	1	0	0	1	0	0	1
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_c	0	0	1	0	0	1	2
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_c	0	1	0	0	1	0	1
t_b	1	0	0	0	0	1	2
t_a	1	0	0	0	0	1	0
t_c	1	0	0	1	0	0	1
t_b	1	0	0	0	1	0	1

Table 5.24 Switching times of the devices, which are turned ON for DCM 5

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	t_c	t_b	0	1	0
2	t_c	0	t_a+t_b	t_b+t_c	t_a	0
3	0	t_b	t_a+t_c	t_a+t_b	0	t_c
4	0	1	0	t_a	t_c	t_b
5	t_b+t_c	t_a	0	t_c	0	t_a+t_b
6	t_a+t_b	0	t_c	0	t_b	t_a+t_c

Table 5.25 Number of switch transitions for DCM 5

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_c	0	1	0	0	1	0	1
t_b	0	0	1	0	1	0	
t_a	0	0	1	0	1	0	0
t_c	1	0	0	1	0	0	2
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_c	0	0	1	0	0	1	1
t_b	0	1	0	1	0	0	2
t_a	0	1	0	1	0	0	0
t_c	0	1	0	0	1	0	1
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_c	1	0	0	1	0	0	2
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_c	0	0	1	0	0	1	1
t_b	1	0	0	0	1	0	

Table 5.26 Switching times of the devices, which are turned ON for DCM 6

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a+tc	0	t_b	t_c	t_a+t_b	0
2	0	0	1	t_b	t_a	tc
3	0	t_b+t_c	t_a	t_a+t_b	t_c	0
4	t_c	t_a+t_b	0	t_a+t_c	0	t_b
5	t_b	t_a	t_c	0	0	1
6	t_a+t_b	t_c	0	0	t_b+t_c	t_a

Table 5.27 Number of switch transitions for DCM 6

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_c	1	0	0	1	0	0	1
t_b	0	0	1	0	1	0	2
t_a	0	0	1	0	1	0	0
t_c	0	0	1	0	0	1	1
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_c	0	1	0	0	1	0	2
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_c	1	0	0	1	0	0	1
t_b	0	1	0	0	0	1	2
t_a	0	1	0	0	0	1	0
t_c	0	0	1	0	0	1	1
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_c	0	1	0	0	1	0	2
t_b	1	0	0	0	1	0	1

From Tables 5.16- 5.27 it is seen that different values of α, β, γ give different possibilities of switching transitions. But it has seen that numbers of switching transitions are minimized for DCM1 when compared that of DCM2 and DCM3. DCM 4, DCM5, DCM6 shows the same number of switch transitions but the sequence of switches in a switching cycle is not symmetrical which may result in unbalance switching hence these modulators are inefficient in linear modulation region.

Figures 5.18 to 5.20 give the switching timings for DCM1, DCM2, DCM3, DCM4, DCM5, and DCM6. Figure 5.18 shows the switching times diagram of all the devices in the six sectors for DCM1. These switching timings are useful in implementing the SVPWM using DSP. And also from the state sequence obtained using the condition of DCM1, it is seen that the states are naturally arranged such that there is no non-optimal switching while switch transitions. This set of switching times gives minimum amount of switching to the converter. Hence this is one of the added advantage, this sequence of switching generates better waveforms, this set of normalized switching times can be considered as high performance modulator.

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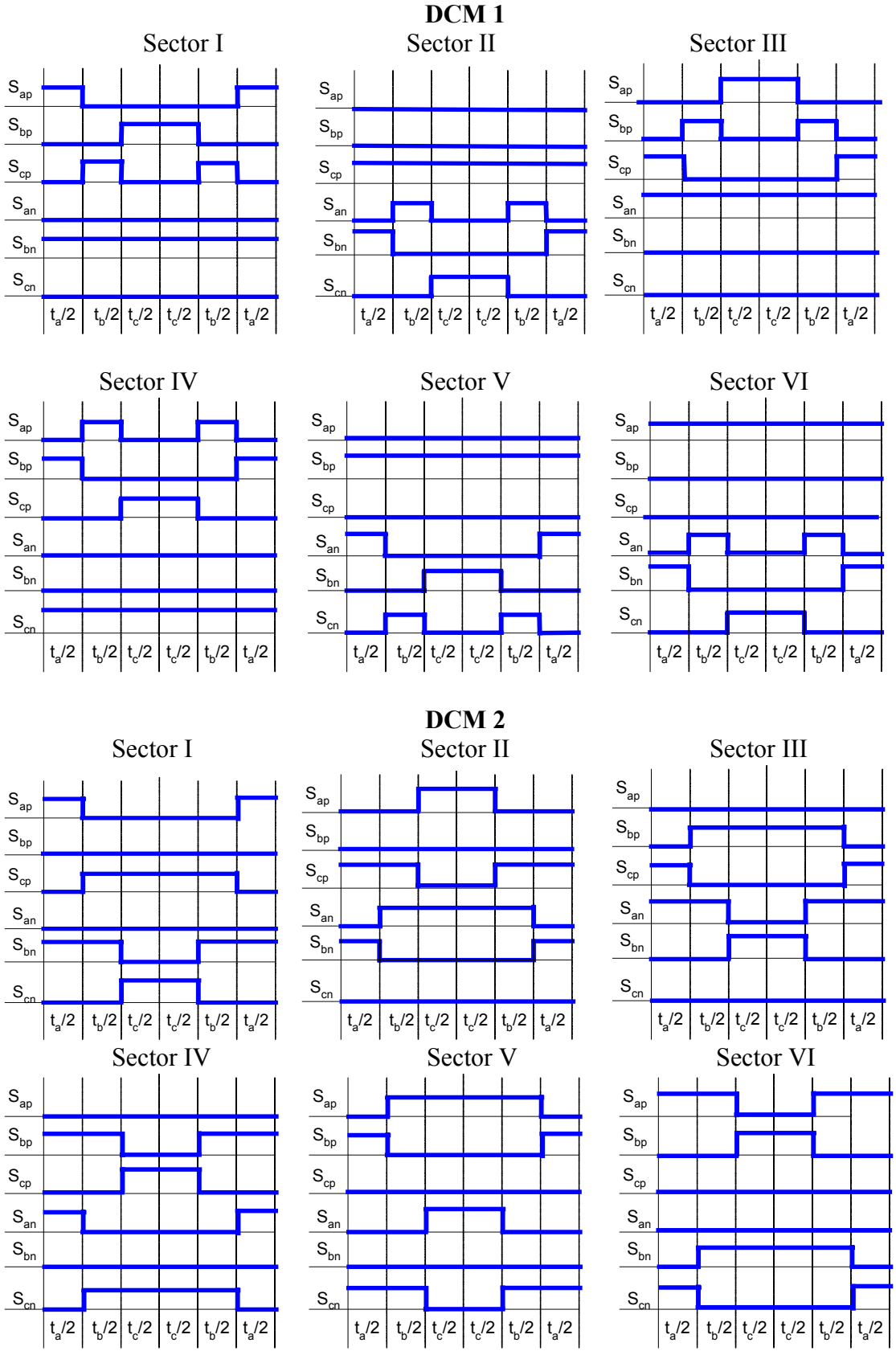


Figure 5.18 Timing diagrams for the devices in all the sectors for DCM 1 and DCM 2

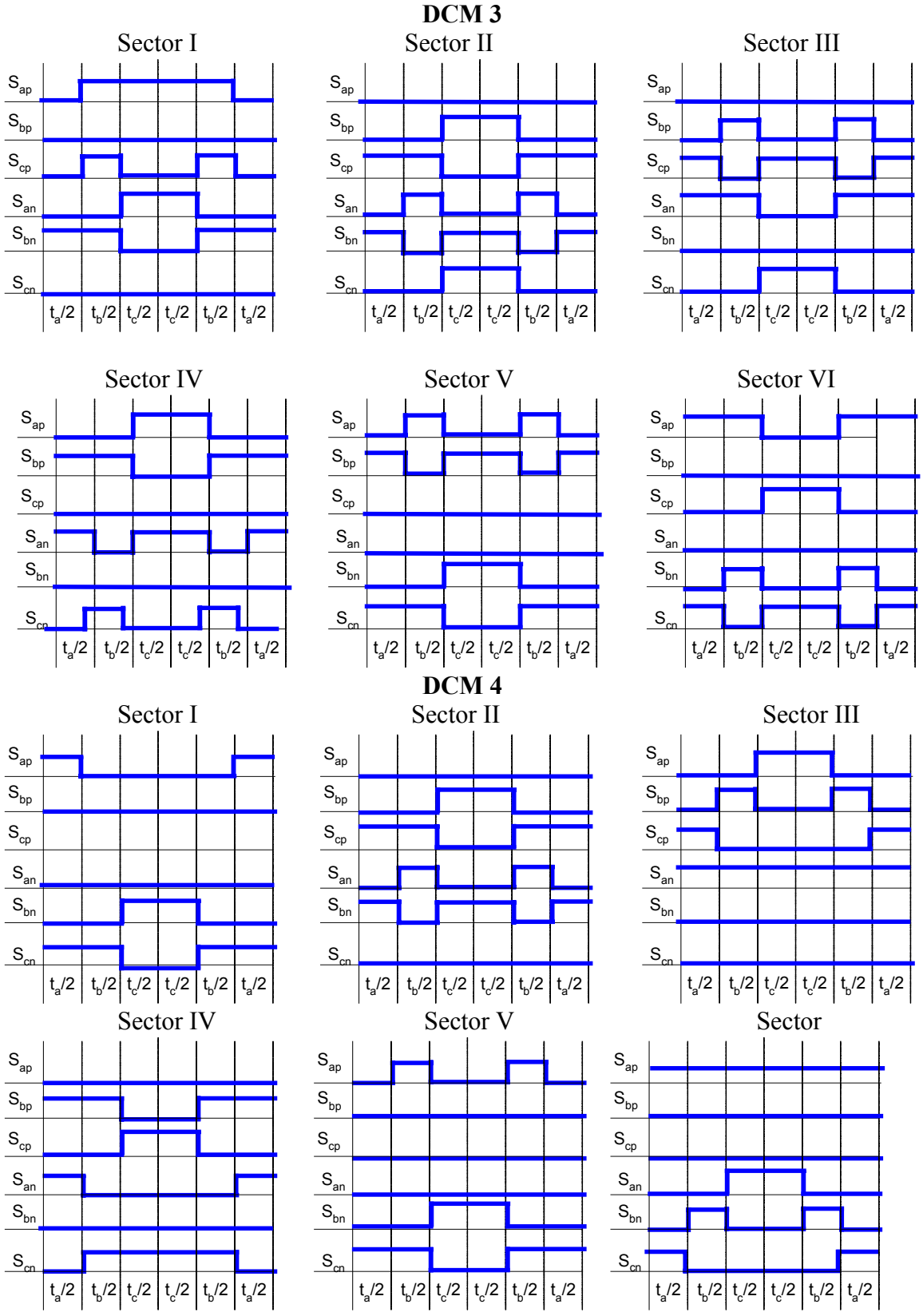


Figure 5.19 Timing diagrams for the devices in all the sectors for DCM 3 and DCM 4

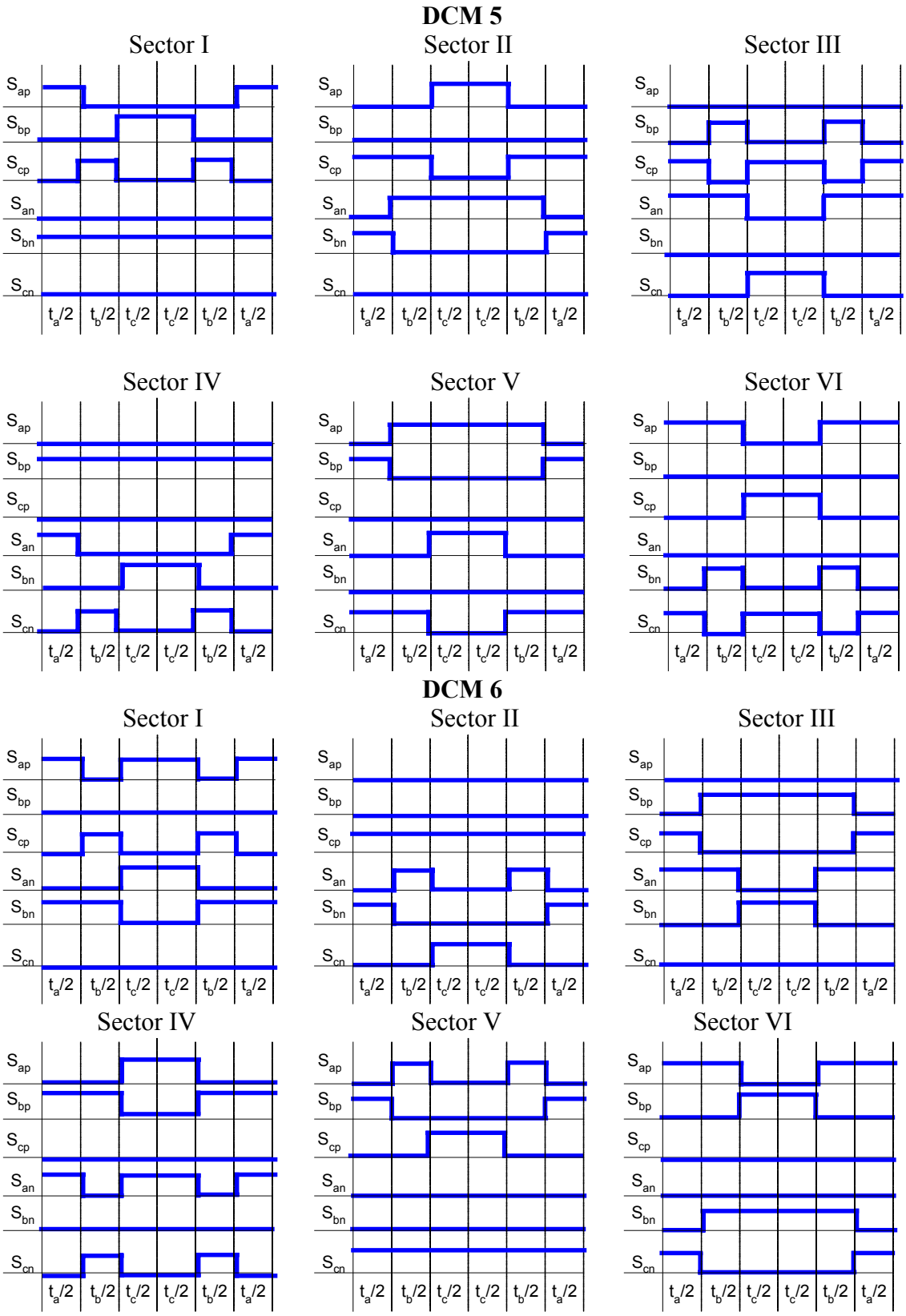


Figure 5.20 Timing diagrams for the devices in all the sectors for DCM 5 and DCM 6

5.6 Over Modulation in CSI Using Space Vector

In linear region of operation of the converter the value of modulation index M ≤ 1, for which the normalized switching timings are $t_a + t_b \leq 1$. Hence the switching time is made equal to 1 by making the null state to spend the remaining time $t_c = 1 - t_a - t_b$. In the case of the over modulation where M ≥ 1 i.e., $t_a + t_b + (\alpha + \beta + \gamma)\, t_c \geq 1$ in over modulation region time for null states (t_o) is made zero. By implicitly removing the null states because null states do not contribute in synthesizing the reference current. Therefore having null time $t_c = 0$ in the above equation and get

$$t_a^* + t_b^* = 1 \quad t_c = 0$$

where t^*_a, t^*_b are the new values of the time duration in order to synthesis the commanded reference vector. The values of the new t^*_a, t^*_b are given as

$$t^*_a = \frac{t_a}{t_a + t_b} \qquad t^*_b = \frac{t_b}{t_a + t_b}. \tag{5.20}$$

Equation (5.20) indicates that the actual times t_a and t_b are proportionally normalized in order to attain the new values t^*_a and t^*_b. This time duration are actually used to synthesize the commanded reference vectors in over modulation region. One of the advantages of the over modulation is that maximum utilization of the input DC voltage takes place.

Table 5.28 Switching times of the devices which are turned ON for DCM 1

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b	0	1	0
2	0	0	1	t_b	t_a	0
3	0	t_b	t_a	1	0	0
4	0	1	0	t_a	0	t_b
5	t_b	t_a	0	0	0	1
6	1	0	0	0	t_b	t_a

Table 5.29 Number of switch transitions for DCM 1

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Transitions
t_a	1	0	0	0	1	0	0
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_b	1	0	0	0	1	0	1

Table 5.30 Switching times of the devices, which are turned ON for DCM 2

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b	0	t_a+t_b	0
2	0	0	t_a+t_b	t_b	t_a	0
3	0	t_b	t_a	t_a+t_b	t_c	0
4	0	t_a+t_b	0	t_a	0	t_b
5	t_b	t_a	0	0	0	t_a+t_b
6	t_a+t_b	0	0	0	t_b	t_a

Table 5.31 Number of switch transitions for DCM 2

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_b	1	0	0	0	1	0	1

Table 5.32 Switching times of the devices, which are turned ON for DCM 3

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b	0	t_a+t_b	0
2	0	t_c	t_a+t_b	t_b	t_a	0
3	0	t_b	t_a	t_a+t_b	0	0
4	0	t_a+t_b	0	t_a	0	t_b
5	t_b	t_a	0	0	t_c	t_a+t_b
6	t_a+t_b	0	0	0	t_b	t_a

Table 5.33 Number of switch transitions for DCM 3

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_b	1	0	0	0	1	0	1

Table 5.34 Switching times of the devices which are turned ON in DCM 4

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b	0	t_a+t_b	0
2	0	0	t_a+t_b	t_b	t_a	0
3	0	t_b	t_a	1	0	0
4	0	t_a+t_b	0	t_a	0	t_b
5	t_b	t_a	0	0	t_c	t_a+t_b
6	1	0	0	0	t_b	t_a

Table 5.35 Number of switch transitions for DCM 4

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_b	1	0	0	0	1	0	1

Table 5.36 Switching times of the devices, which are turned ON for DCM 5

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b	0	1	0
2	0	0	t_a+t_b	t_b	t_a	0
3	0	t_b	t_a	t_a+t_b	0	0
4	0	1	0	t_a	t_c	t_b
5	t_b	t_a	0	0	0	t_a+t_b
6	t_a+t_b	0	0	0	t_b	t_a

Table 5.37 Number of switch transitions for DCM 5

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_b	1	0	0	0	1	0	1

Table 5.38 Switching times of the devices, which are turned ON for DCM 6

Sector	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}
1	t_a	0	t_b	0	t_a+t_b	0
2	0	0	1	t_b	t_a	0
3	0	t_b	t_a	t_a+t_b	0	0
4	0	t_a+t_b	0	t_a	0	t_b
5	t_b	t_a	0	0	0	1
6	t_a+t_b	0	0	0	t_b	t_a

Table 5.39 Number of switch transitions for DCM 5

Timings	T_{ap}	T_{bp}	T_{cp}	T_{an}	T_{bn}	T_{cn}	Switching Transitions
t_a	1	0	0	0	1	0	0
t_b	0	0	1	0	1	0	1
t_a	0	0	1	0	1	0	0
t_b	0	0	1	1	0	0	1
t_a	0	0	1	1	0	0	0
t_b	0	1	0	1	0	0	1
t_a	0	1	0	1	0	0	0
t_b	0	1	0	0	0	1	1
t_a	0	1	0	0	0	1	0
t_b	1	0	0	0	0	1	1
t_a	1	0	0	0	0	1	0
t_b	1	0	0	0	1	0	1

Tables (5.28) to (5.38) gives switch ON times for all the devices in overmodulation in all the sectors and also number of switching transitions in each cycle are given, for all the combinations of α, β, γ. It is seen that the switching sequence and the number switching transitions come out to be same for all the combinations of α, β, γ. Since the switching sequence is same for all the modulators the timing diagram for the devices will be same for all the combinations α, β, γ. Figure 5.21 shows the timing diagram for one set, which is same for other combinations also. Hence it can be concluded that the in overmodulation all the above modulators shows the same performances.

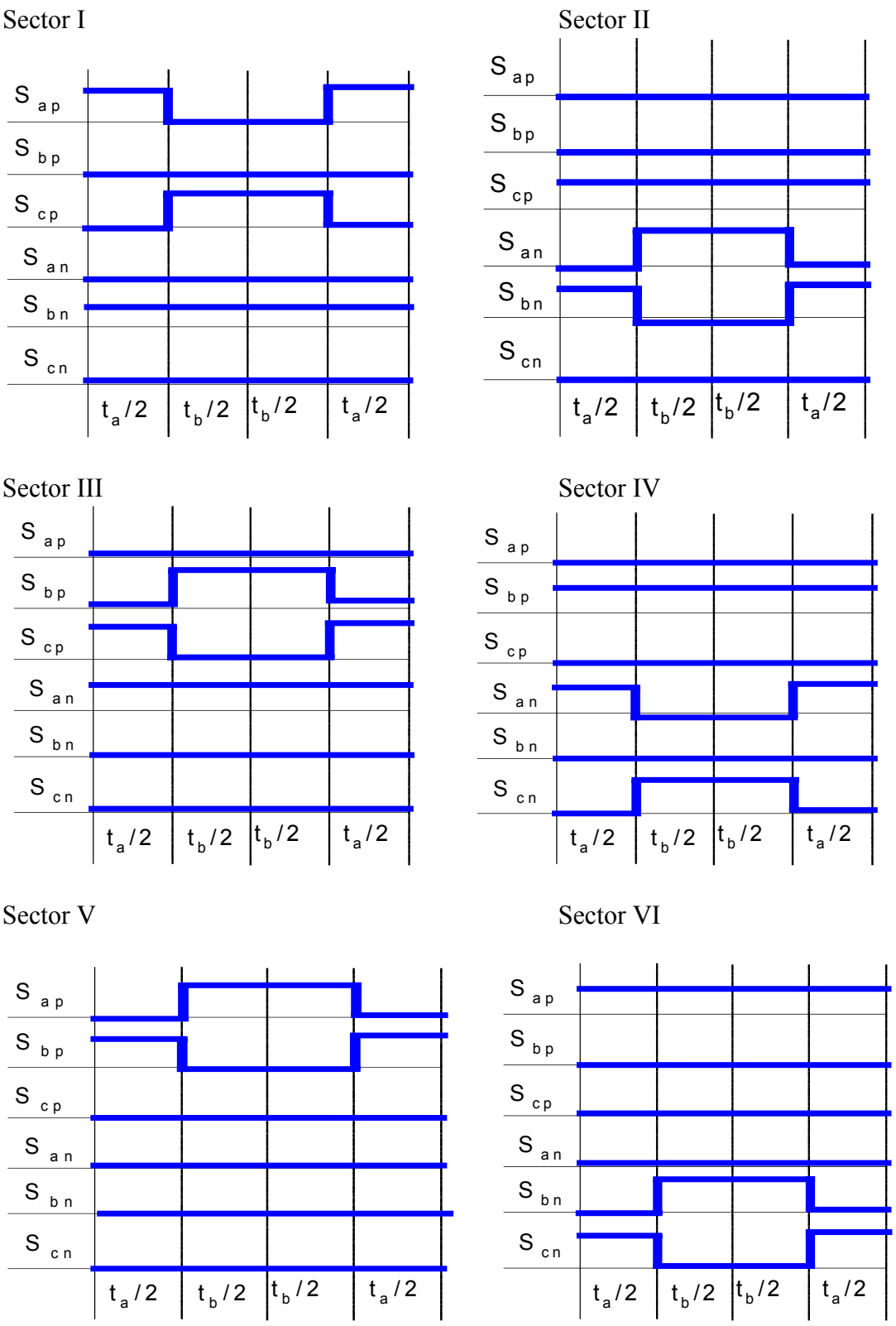


Figure 5.21 Timing diagrams for the devices in all the sectors.

5. 7 Simulation and Experimental Results

Simulation of a current source inverter is performed using the model presented in section 3.9. The direct sine triangle modulation scheme developed in section 5.2 is used to modulate the inverter. The parameters in the simulation are switching frequency of the carrier triangle is taken as 5kHz, the input DC voltage of 100V, input side inductor of 100mH, output side load inductor of 12mH, output side filter capacitor 60μF, three phase resistive load of 30Ω.

An experimental setup is built using the TMS320LF2407a floating point DSP. The PWM ports from both EVA and EVB of the DSP are used to generate the all the independent switching signals [S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn}, S_{cn}] and the maximum pulse, medium pulse, minimum pulse, are generated using the DAC 's of the DSP. The logic explained in section 5.3 is implemented using the simple AND, OR gates. The output-switching pattern from the logic circuit will satisfy the conditions laid out for the CSI. Expressions derived for the continuous modulating signals in section 3.9 are used both in linear and over modulation region. And also different set of discontinuous modulation signals are obtained for different values of α, β, γ as stated in Table 5.9, which are used both in linear and over modulation region. A small amount of overlap time is provided to the switching signals through an external hardware circuit to avoid short circuit of the input side current. And the same parameters as stated above are used with a modulation index of M = 0.85 (linear region) and M = 1.25 (over modulation region). Valid experimental results are given for the above state modulators.

5.7.1 Continuous Modulation in Linear Region

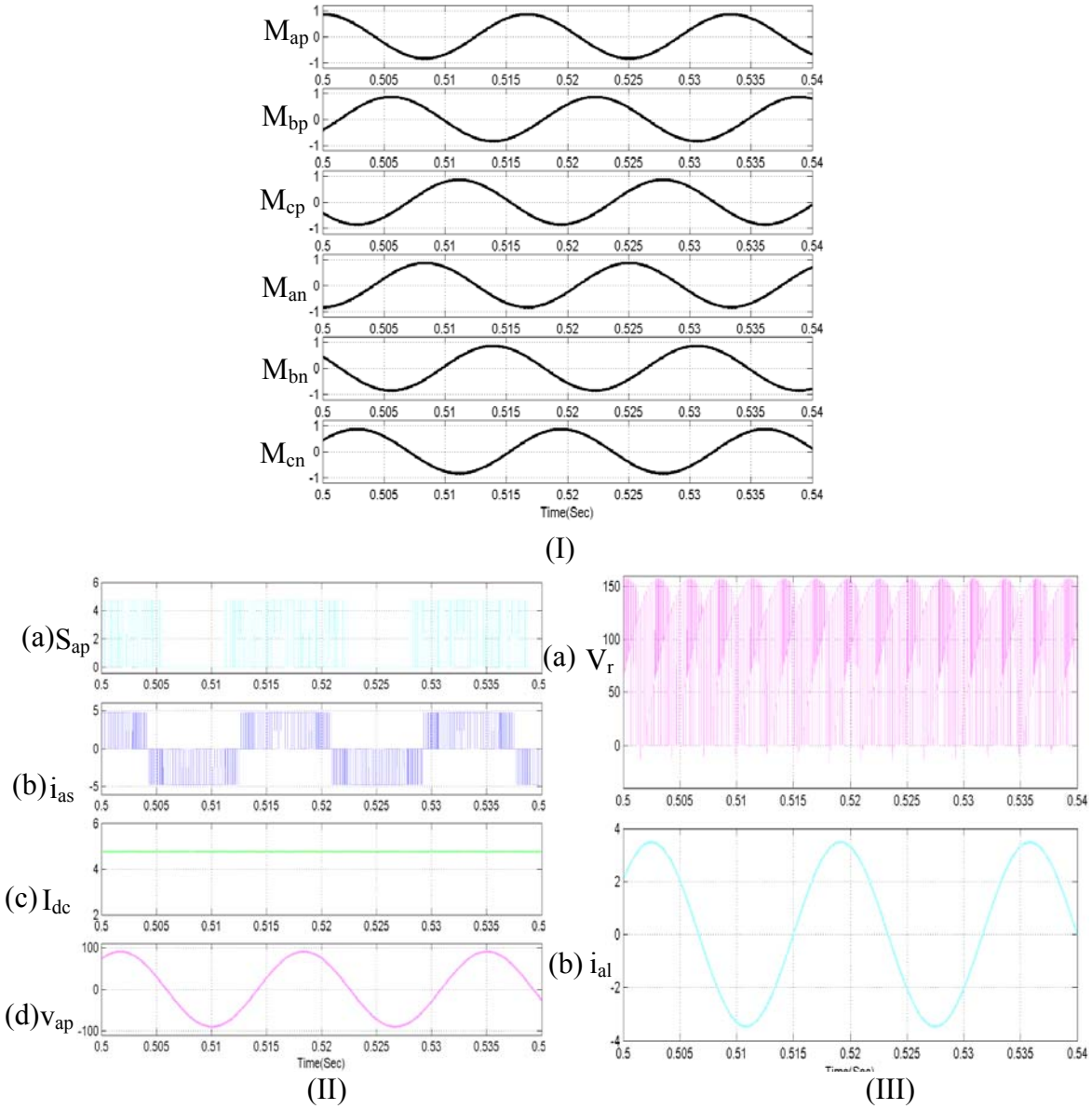


Figure 5.22 Open loop simulation results for Three phase CSI for continuous modulating signals at M = 0.85 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating Signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.

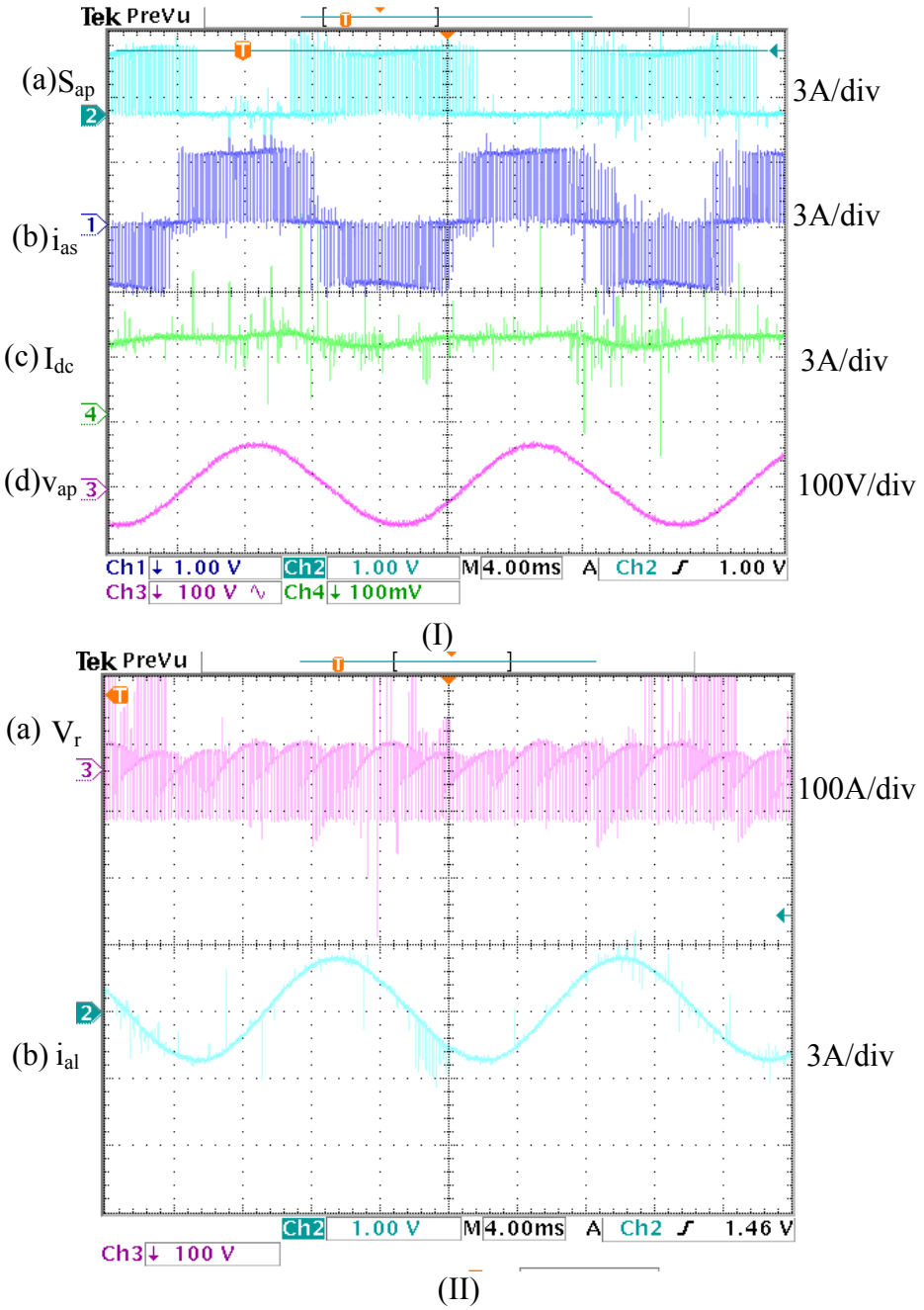


Figure 5.23 Open loop Experimental results for Three phase CSI for continuous modulating signals at M = 0.85 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function (b) phase 'a' line current (c) input DC current, (d) phase 'a' capacitor voltage, (III) (a) inverter DC bus voltage, (b) phase 'a' load line current.

5.7.2 Continuous Modulation in Overmodulation Region

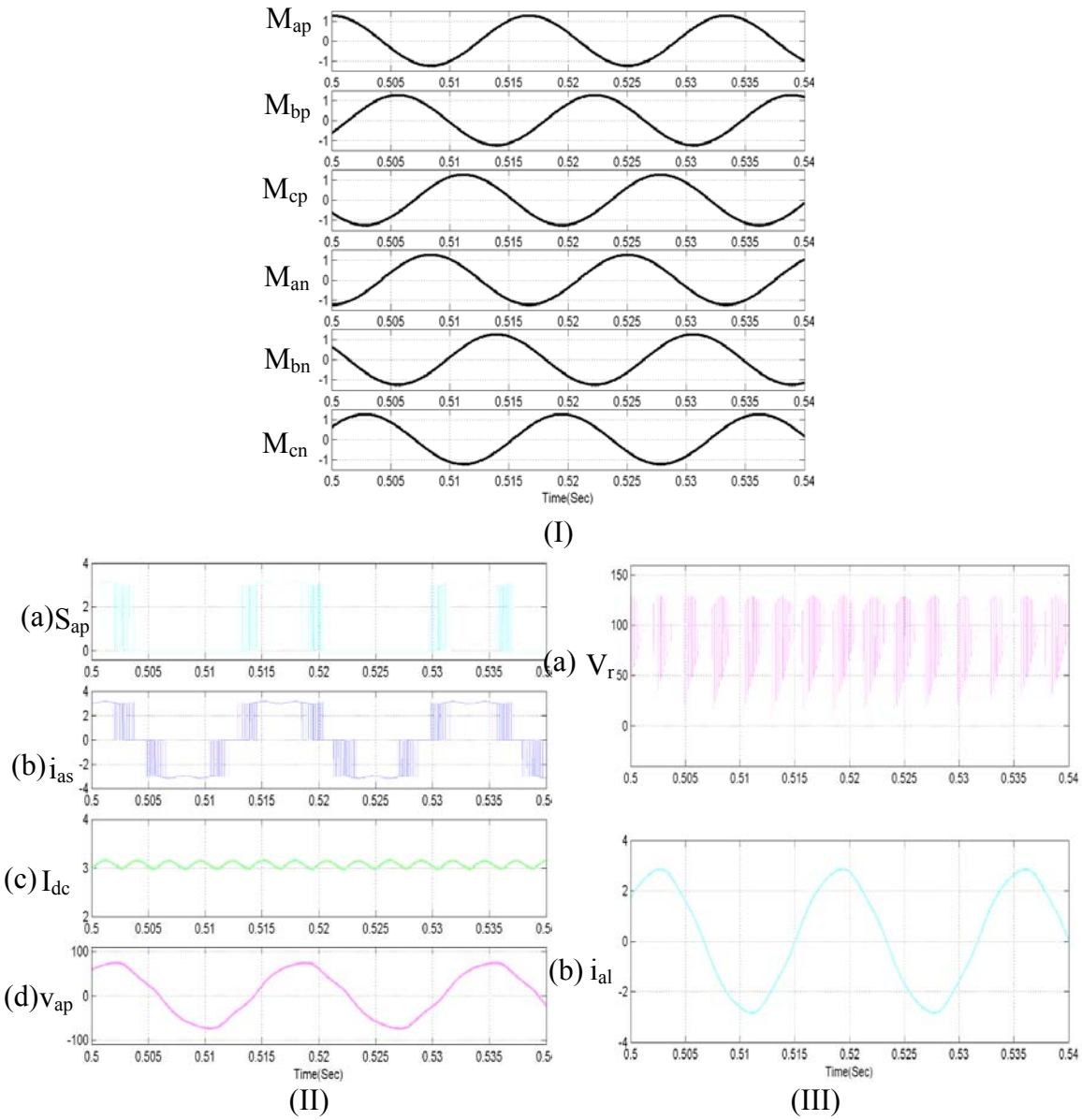
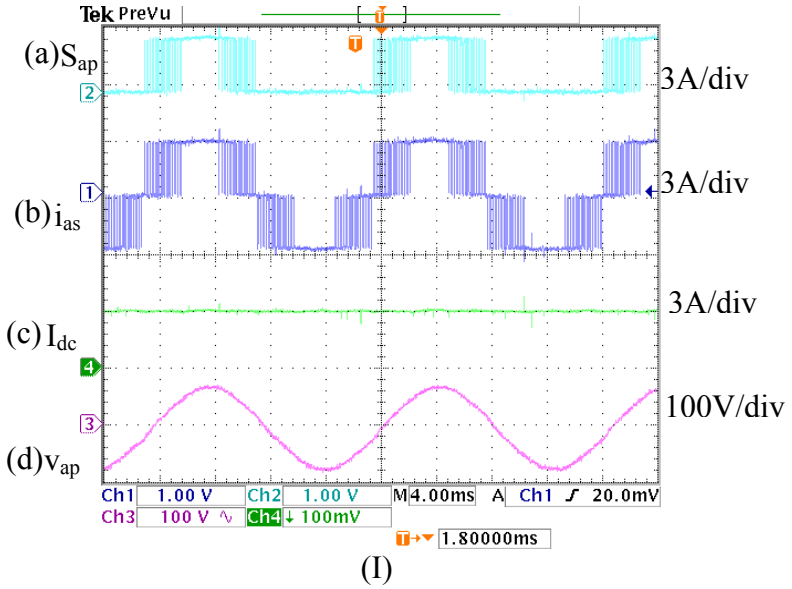
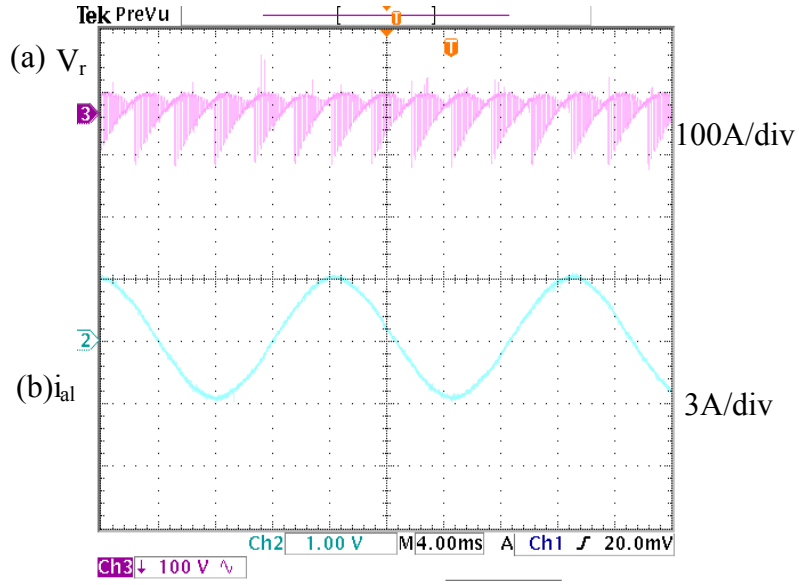


Figure 5.24 Open loop simulation results for Three phase CSI for continuous modulating signals at M = 1.25 at f_s = 5kHz with input DC voltage = 100V, $I_{d\,c}$= 3A, R_L = 25Ω, (I) Modulating Signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function (b) phase 'a' line current, (c) input DC current, (d) phase 'a' Capacitor voltage. (III) (a) DC voltage across the inverter, (b) phase 'a' load line current .



(I)



(II)

Figure 5.25 Open loop Experimental results for Three phase CSI for continuous modulating signals at M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' Capacitor voltage, (III) (a) inverter DC bus voltage, (b) phase 'a' load line current.

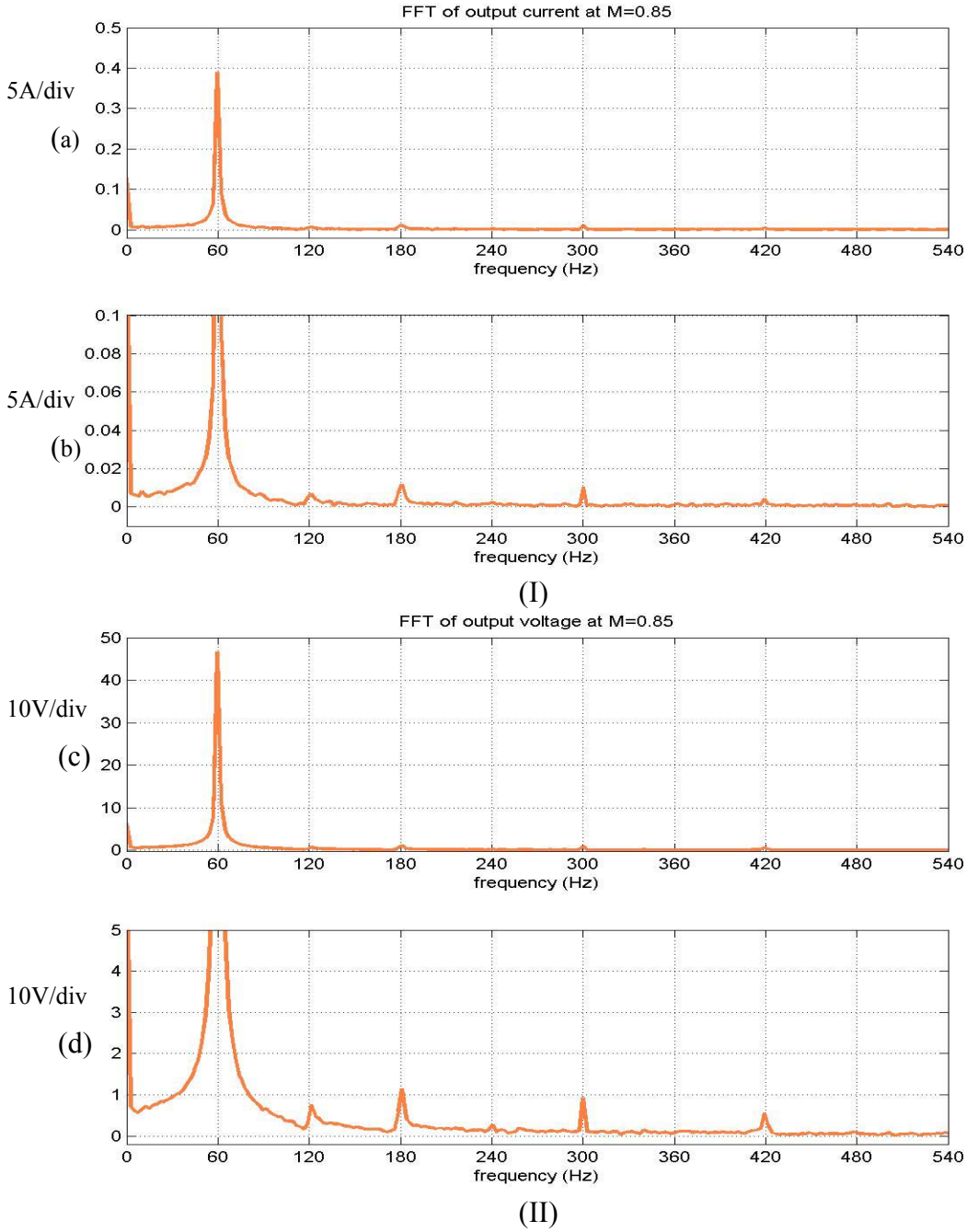
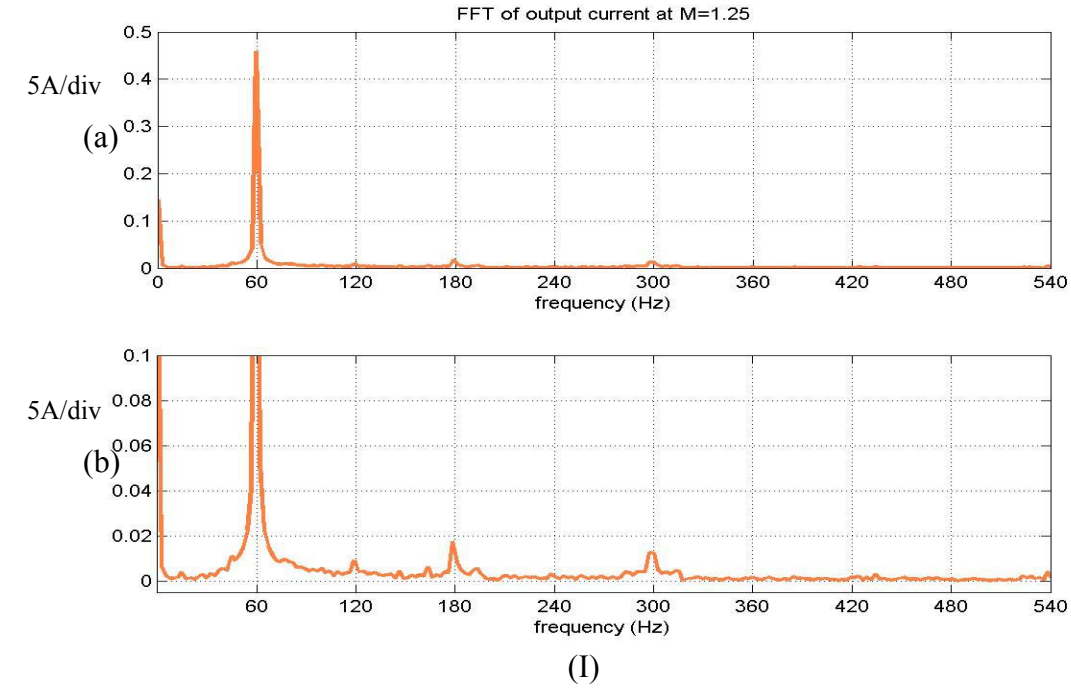
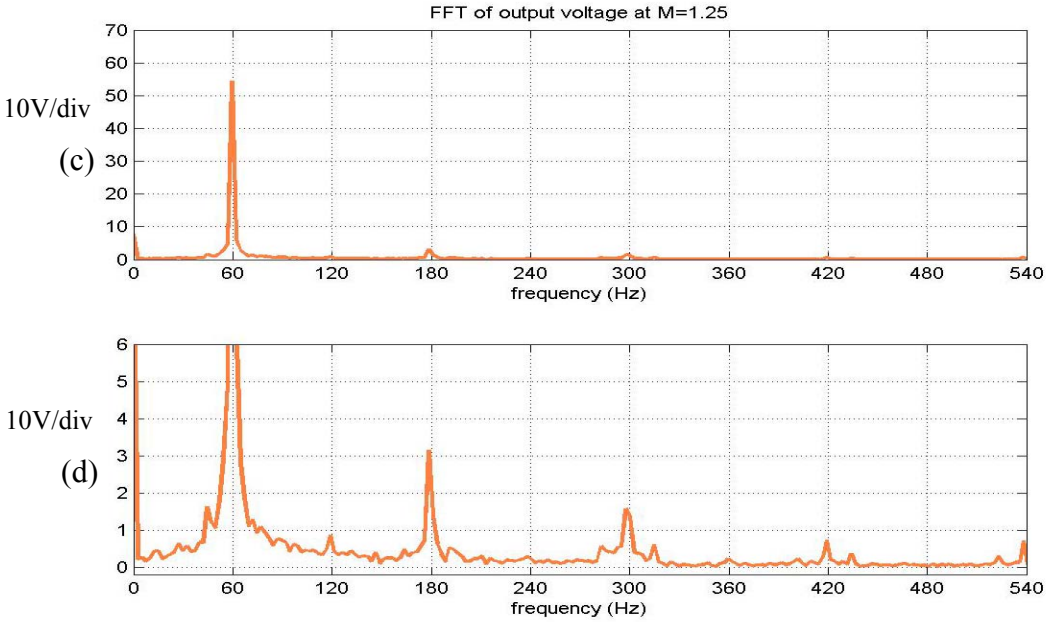


Figure 5.26 (I) and (II) FFT of the filtered output voltage and current continuous modulation at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz, (b) FFT showing other harmonics in the current (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output Voltage.



(I)



(II)

Figure 5.27 (I) and (II) FFT of the filtered output voltage and current for continuous Modulation scheme at M = 1.25 (a) shows the FFT of the output current showing the fundamental component at 60Hz (b) FFT showing other harmonics in the current (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output voltage.

5.7.3 DCM1 in Linear Region

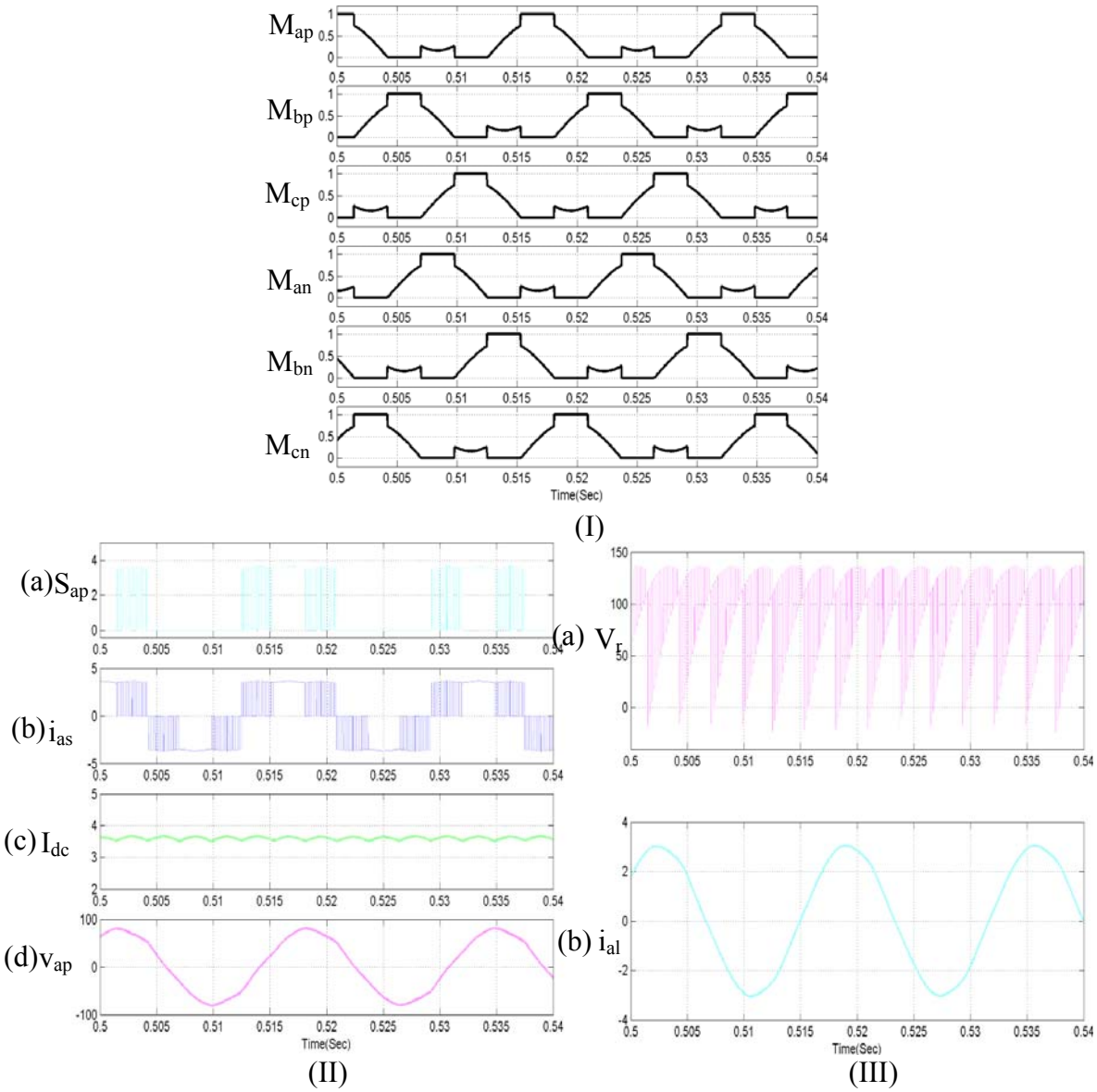
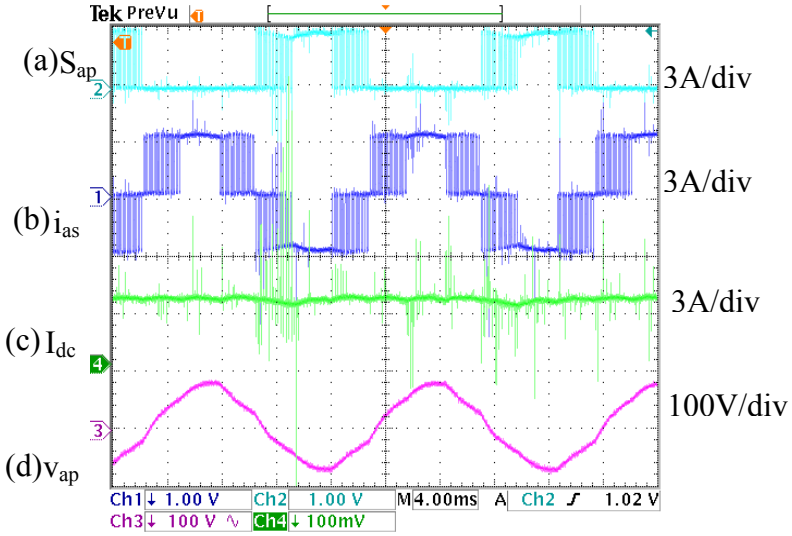
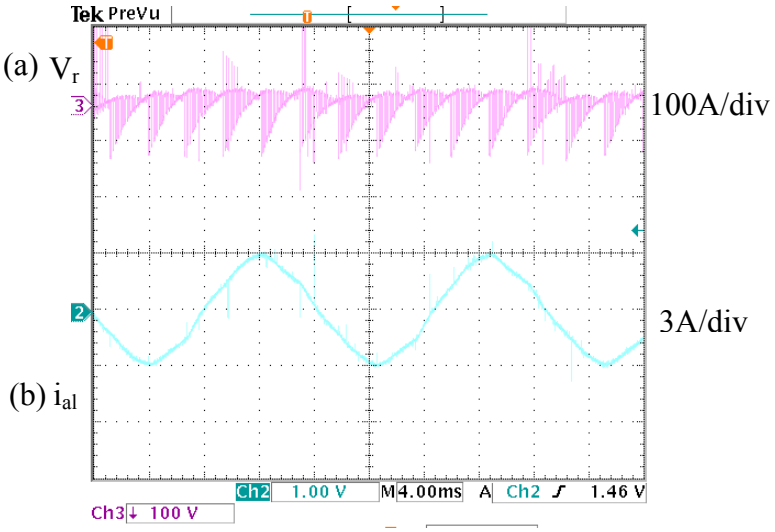


Figure 5.28 Open loop simulation results for Three phase CSI for discontinuous modulating signals DCM 1 at M = 0.85 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current (c) input DC current, (d) phase 'a' Capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.



(I)



(II)

Figure 5.29 Open loop Experimental results for Three phase CSI for discontinuous modulating signals DCM 1 at M = 0.85 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function (b) phase 'a' line current, (c) Input DC current, (d) phase 'a' Capacitor voltage. (III) (a) inverter DC bus voltage, (b) phase 'a' load line current.

5.7.4 DCM1 in Overmodulation Region

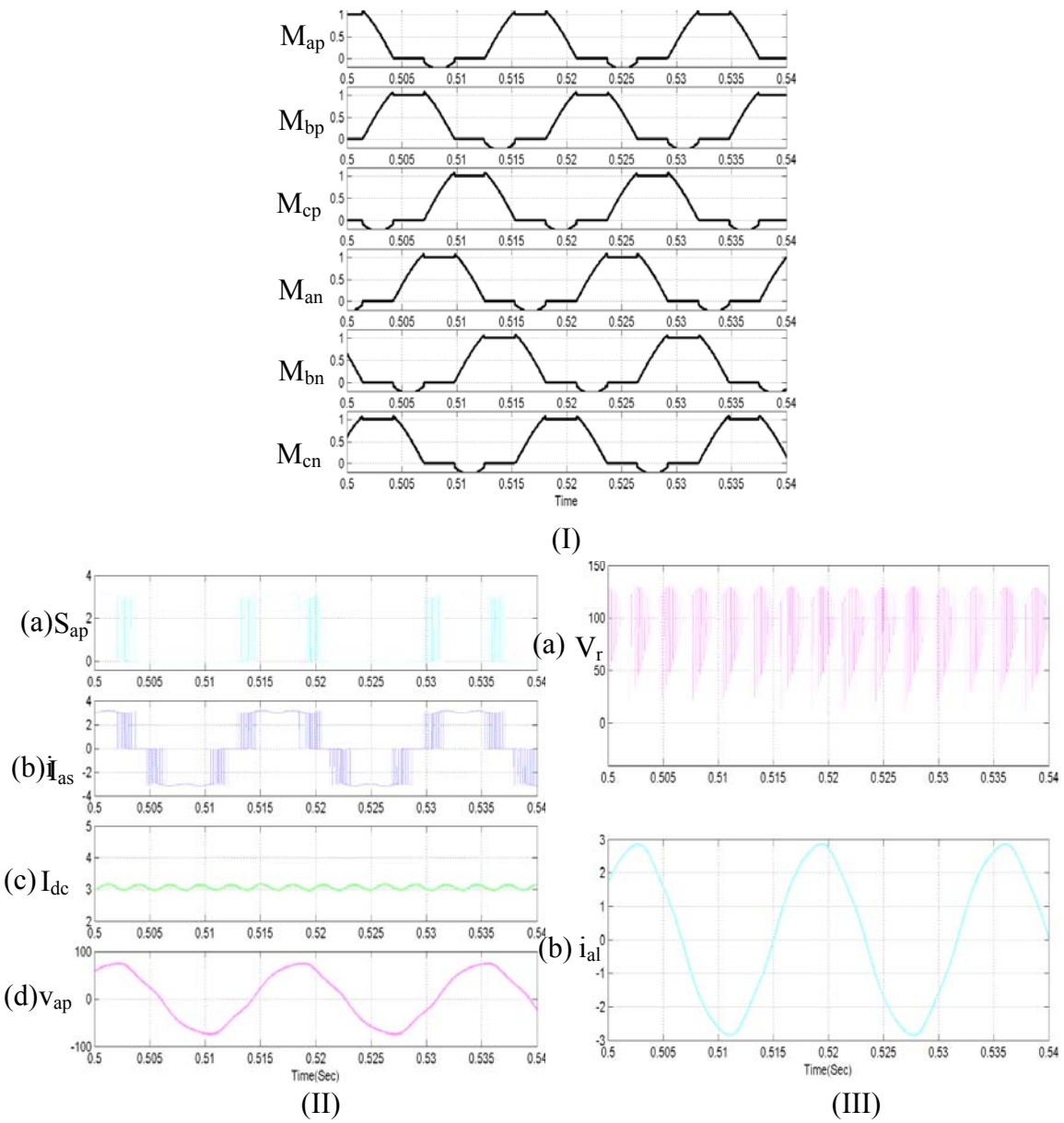


Figure 5.30 Open loop simulation results for Three phase CSI for discontinuous modulating signals DCM 1 with M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating Signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current (d) phase 'a' Capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.

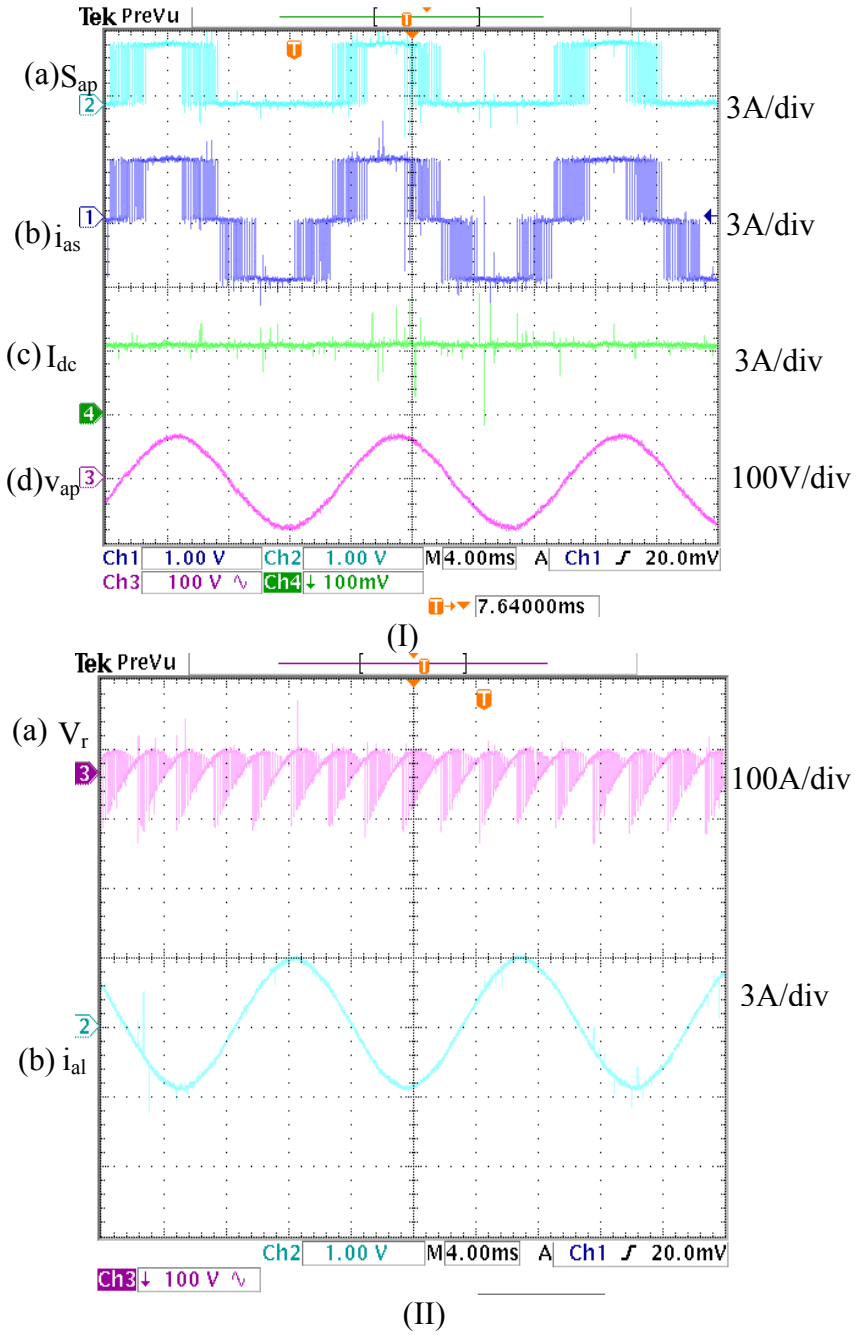


Figure 5.31 Open loop Experimental results for Three phase CSI for discontinuous modulating signals DCM 1 at M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' Capacitor voltage. (III), (a) inverter DC bus voltage, (b) Phase 'a' load line current.

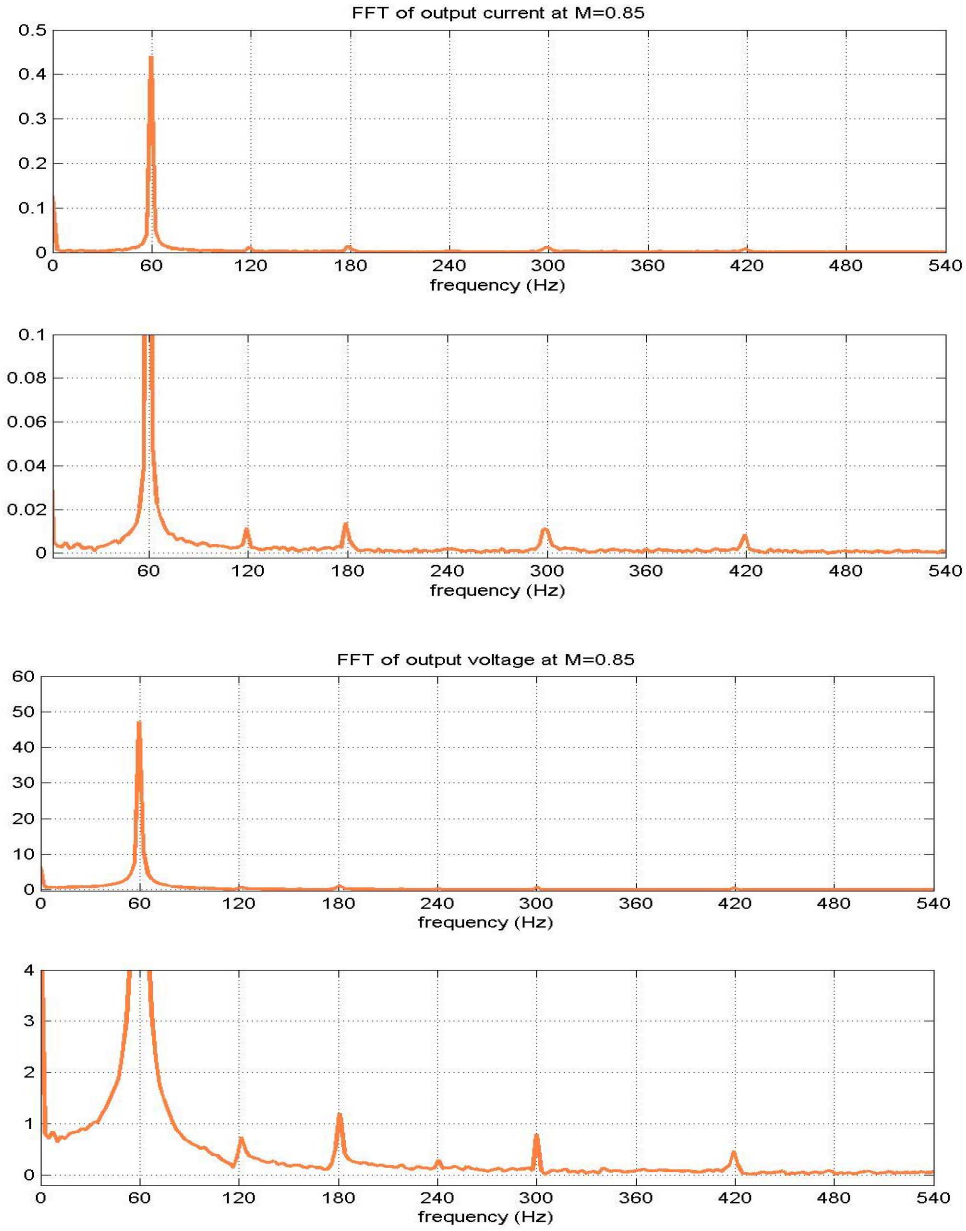


Figure 5.32 (I) and (II) FFT of the filtered output voltage and current DCM 1 modulation at M = 0.85 (a) shows the FFT of the output current showing the fundamental component at 60Hz (b) FFT showing other harmonics in the current (c) FFT of the output voltage with fundamental component at 60Hz, (d) FFT showing other harmonics in output Voltage.

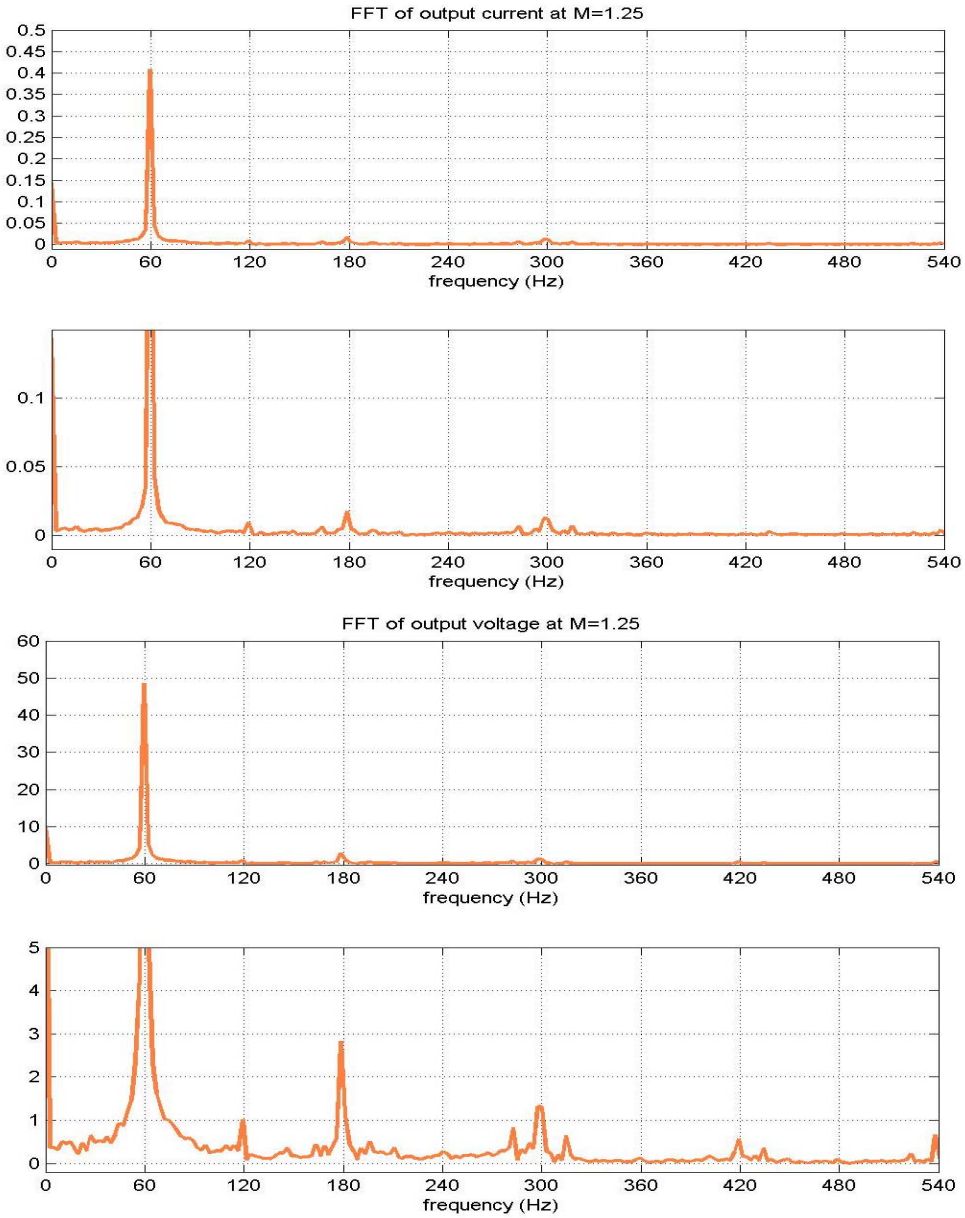


Figure 5.33 (I) and (II) FFT of the filtered output voltage and current DCM1 modulation at M = 1.25 (a) shows the FFT of the output current showing the fundamental component at 60Hz (b) FFT showing other harmonics in the current (c) FFT of the output voltage with fundamental component at 60Hz (d) FFT showing other harmonics in output Voltage.

5.7.5 DCM2 in Linear Region

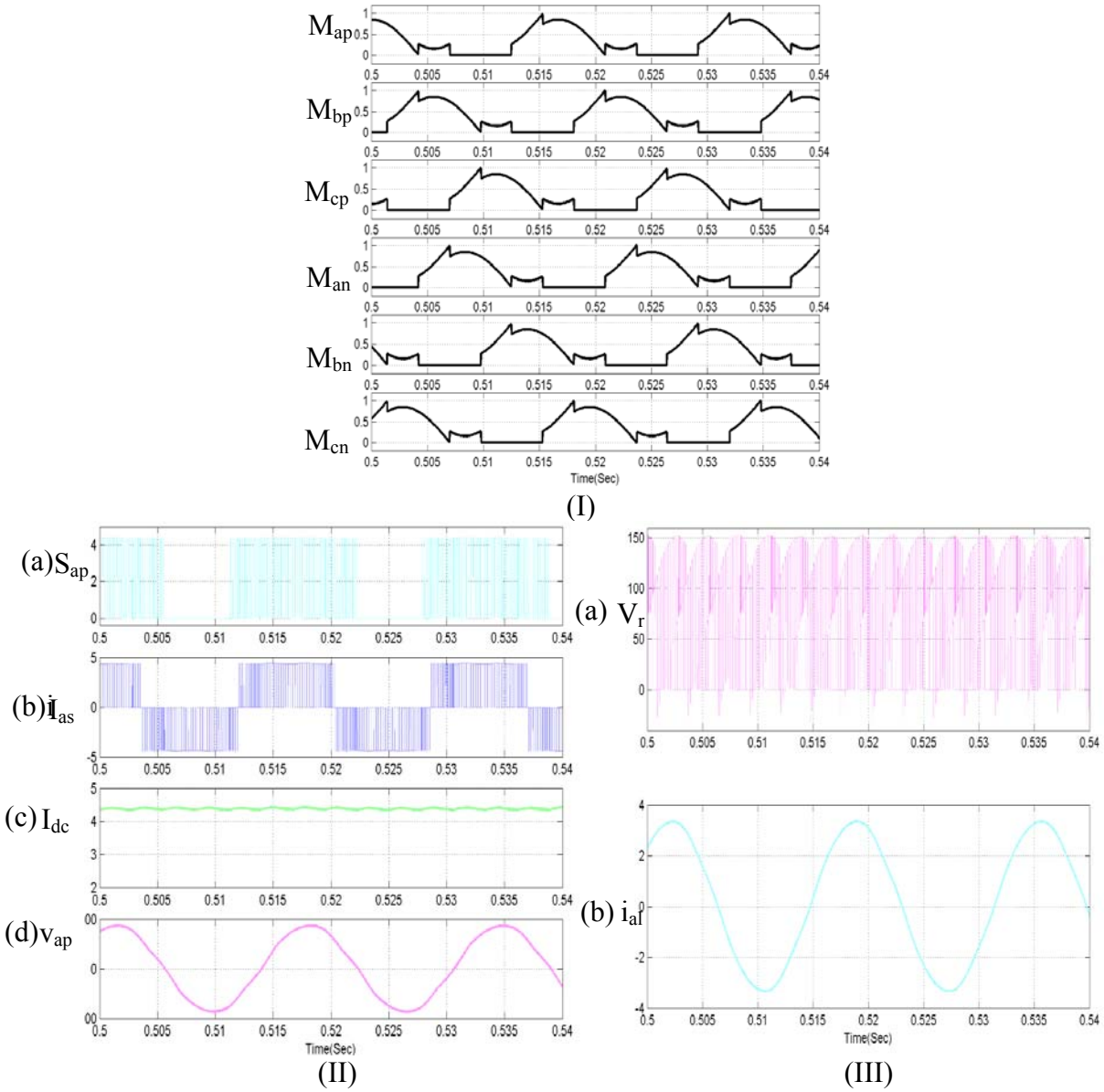
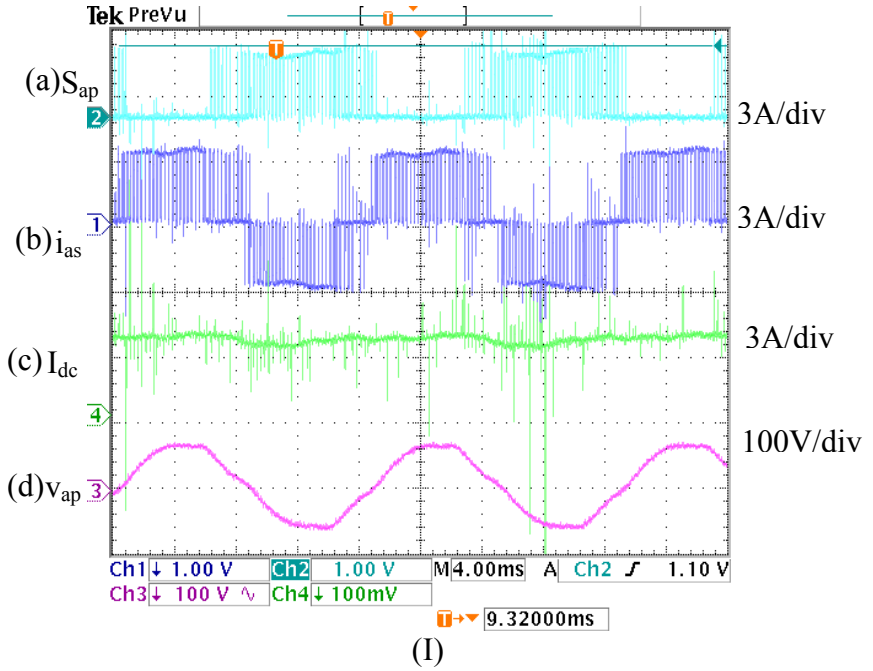
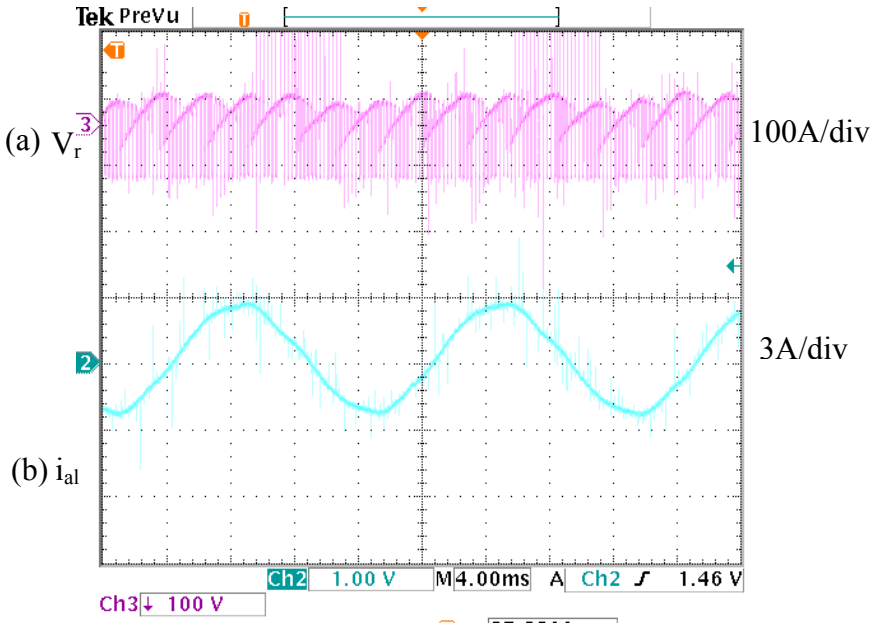


Figure 5.34 Open loop simulation results for Three phase CSI for discontinuous modulating signals DCM 1 at M = 0.85 at f_s = 5KHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' Capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.



(I)



(II)

Figure 5.35 Open loop Experimental results for Three phase CSI for discontinuous modulating signals DCM 2 at M = 0.85 at f_s = 5KHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) Input DC current, (d) phase 'a' capacitor voltage. (III), (a) inverter DC bus voltage, (b) phase 'a' load line current.

5.7.6 DCM 2 in Overmodualtion Region

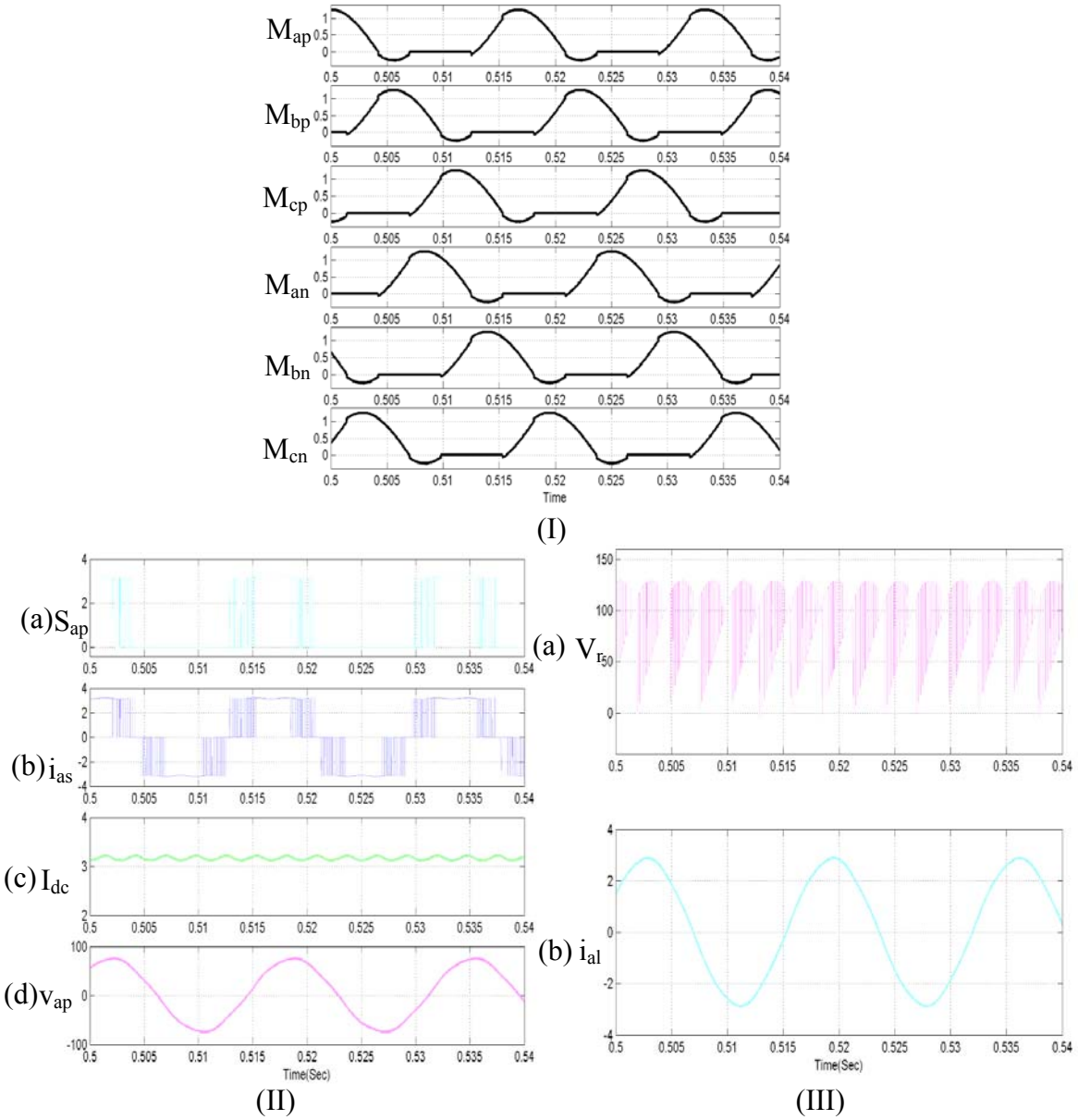
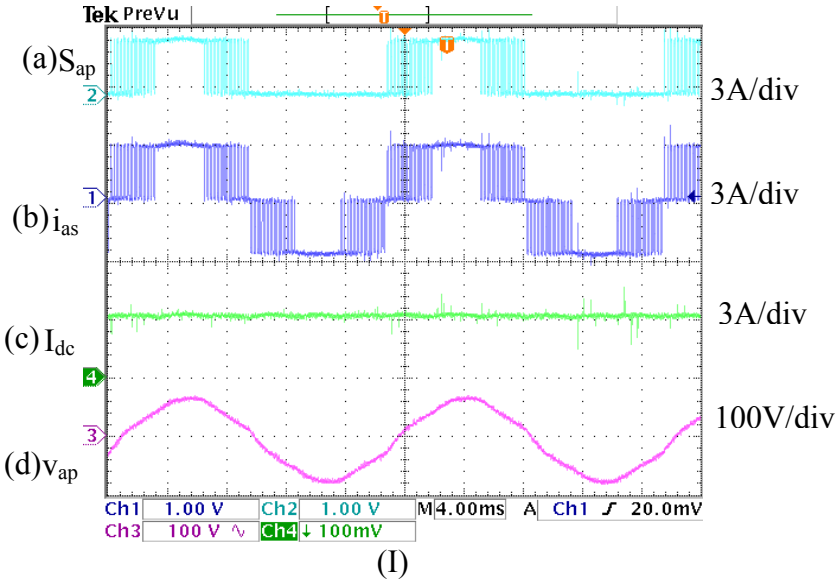
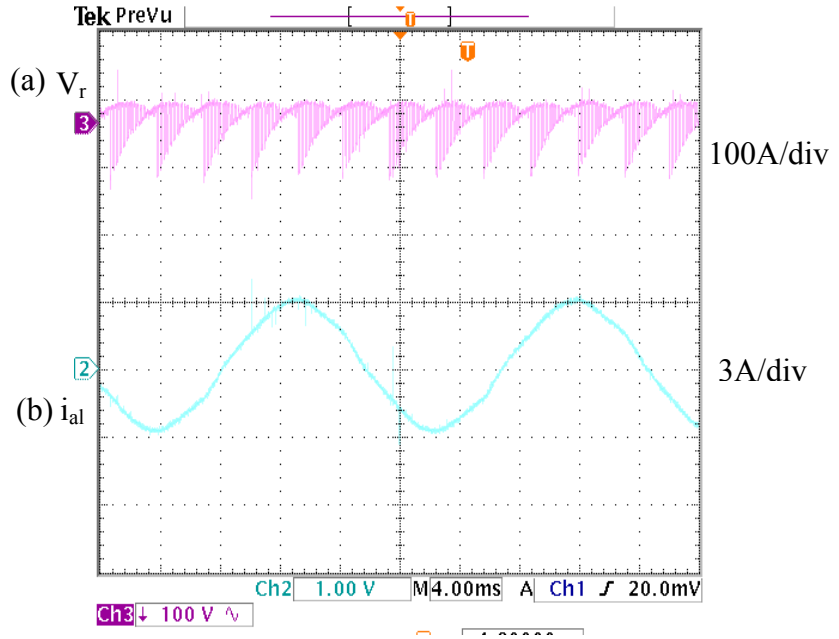


Figure 5.36 Open loop simulation results for Three phase CSI for discontinuous modulating signals DCM 2 with M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating Signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.



(I)



(II)

Figure 5.37 Open loop Experimental results for Three phase CSI for discontinuous modulating signals DCM 2 at M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) inverter DC bus voltage, (b) Phase 'a' load line current.

5.7.7 DCM 3 in Linear Region

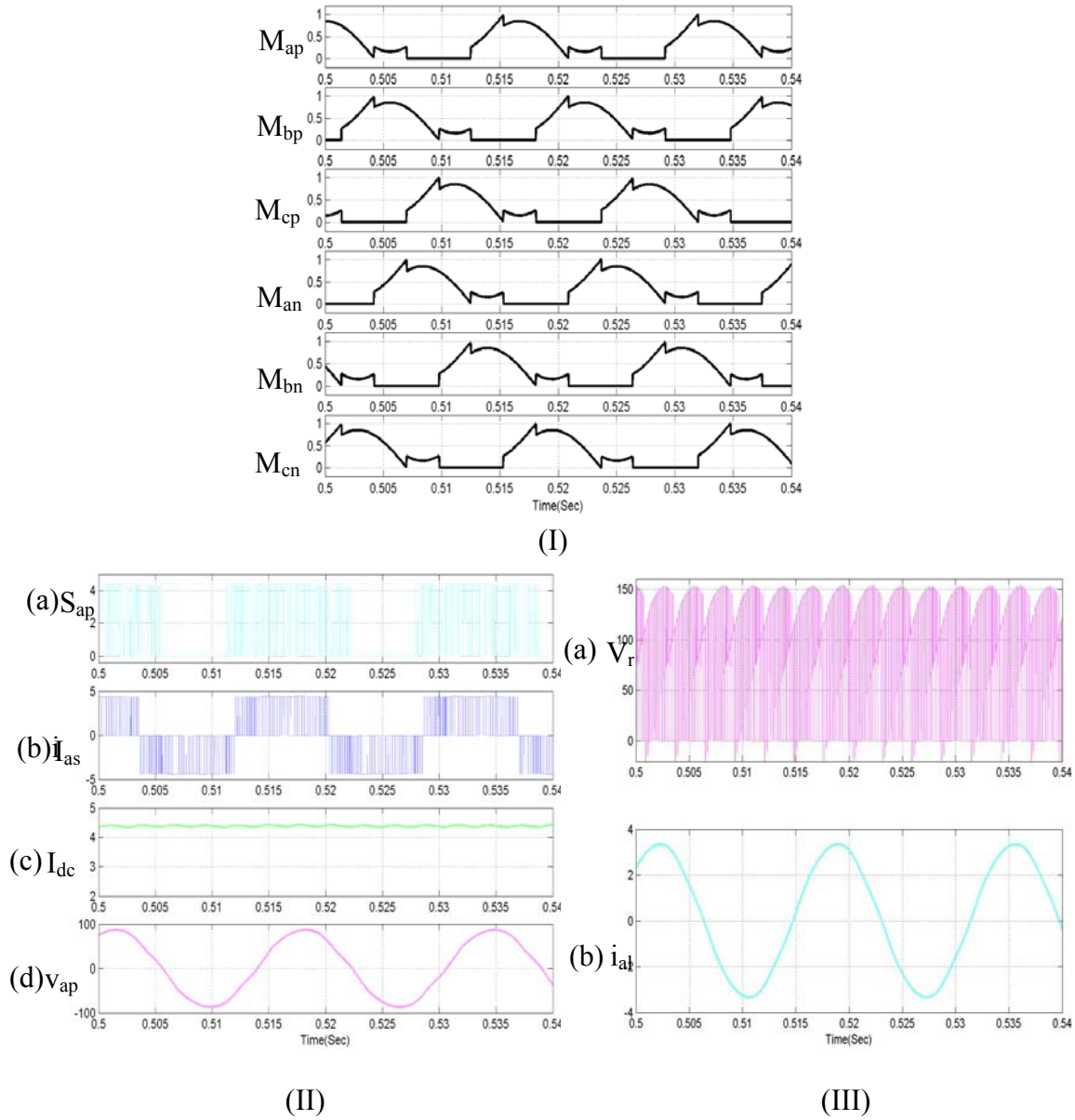


Figure 5.38 Open loop simulation results for Three phase CSI for discontinuous modulating signals DCM 3 with M = 0.85 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating Signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.

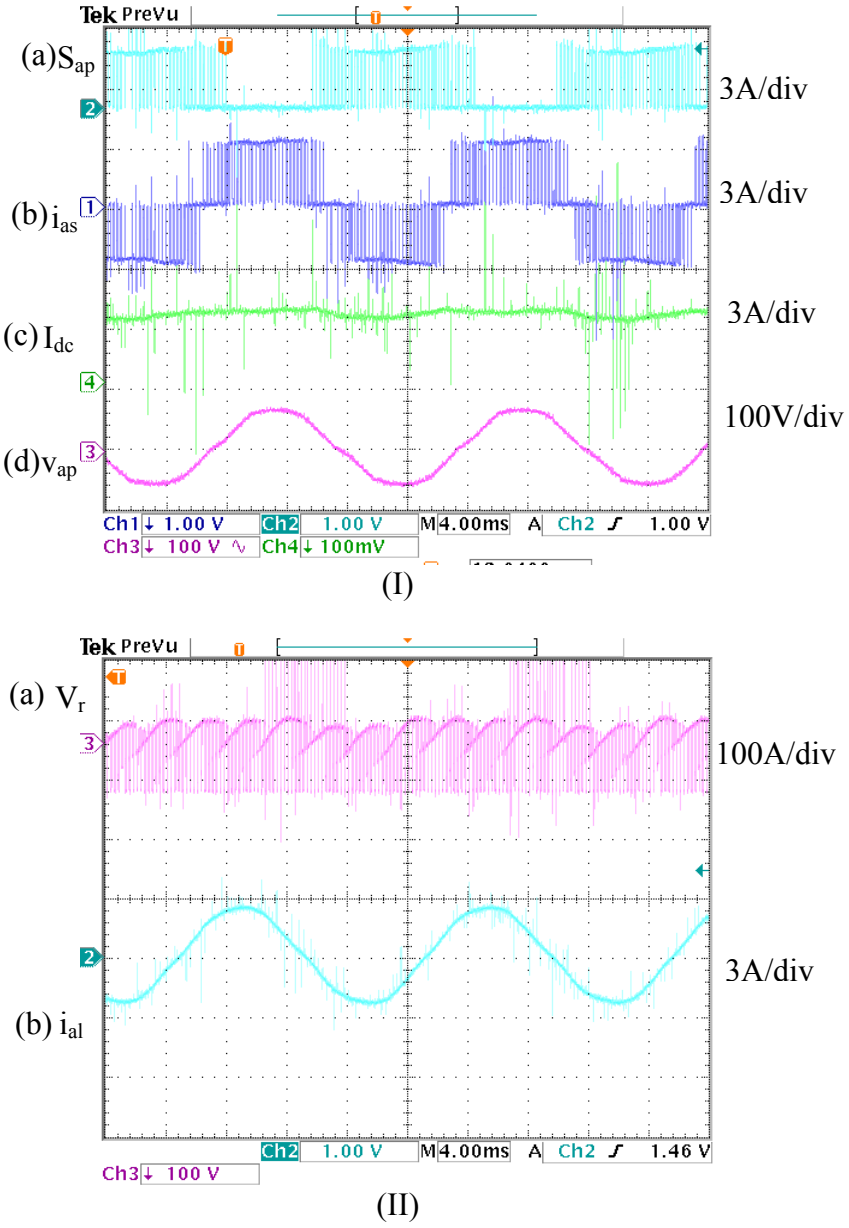


Figure 5.39 Open loop Experimental results for Three phase CSI for discontinuous modulating signals DCM 2 at M = 0.85 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) inverter DC bus voltage, (b) Phase 'a' load line current.

5.7.8 DCM 3 in Overmodulation Region

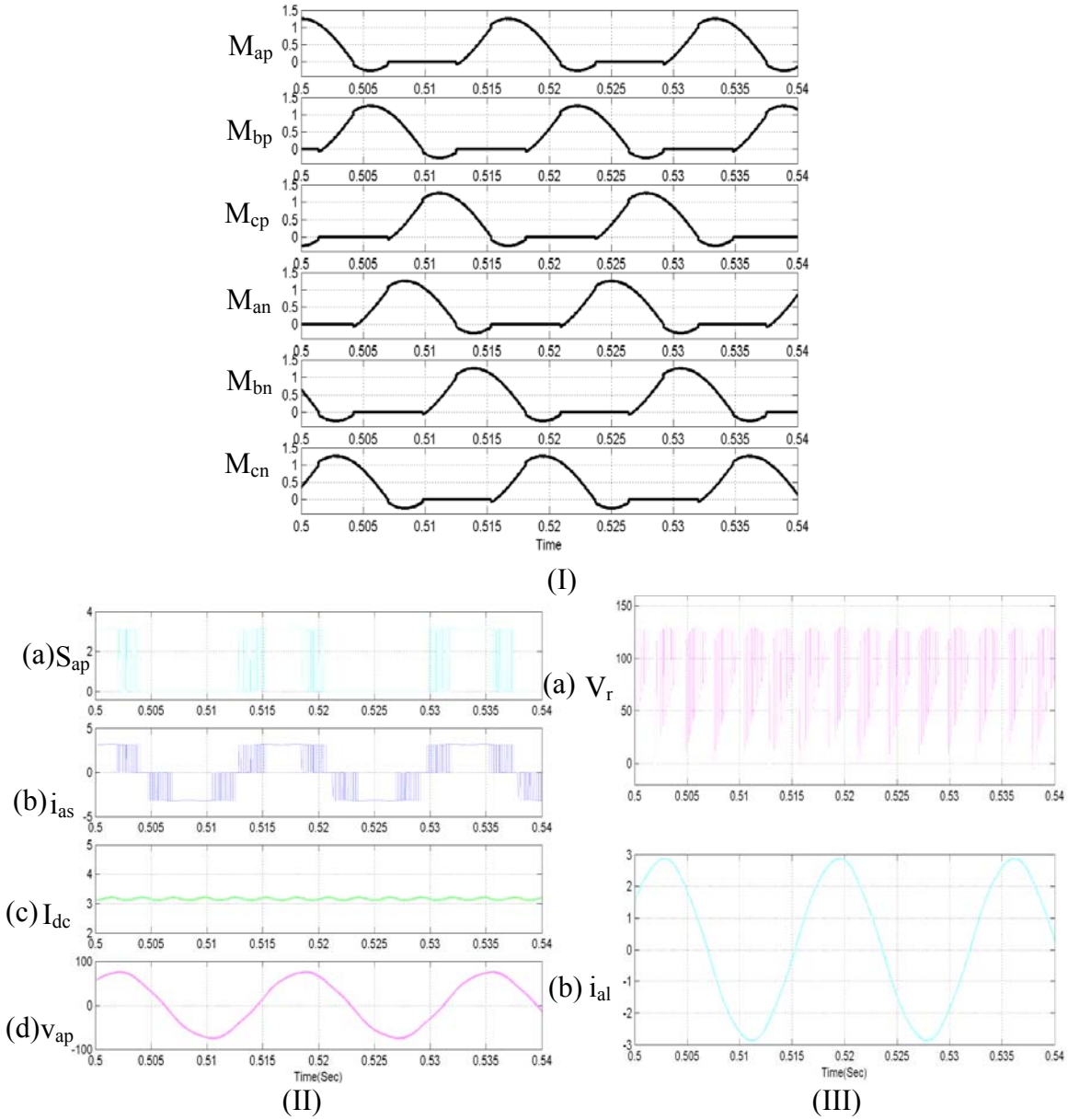
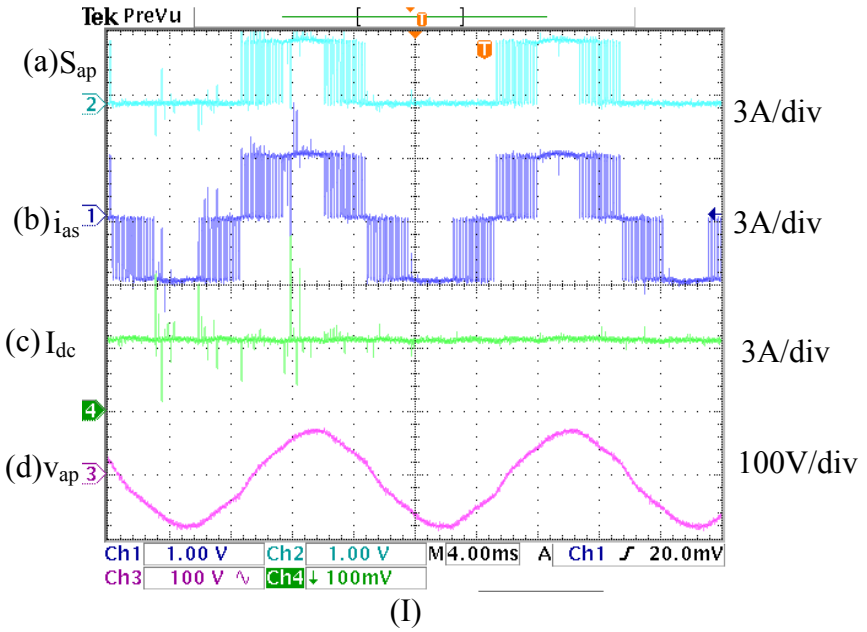
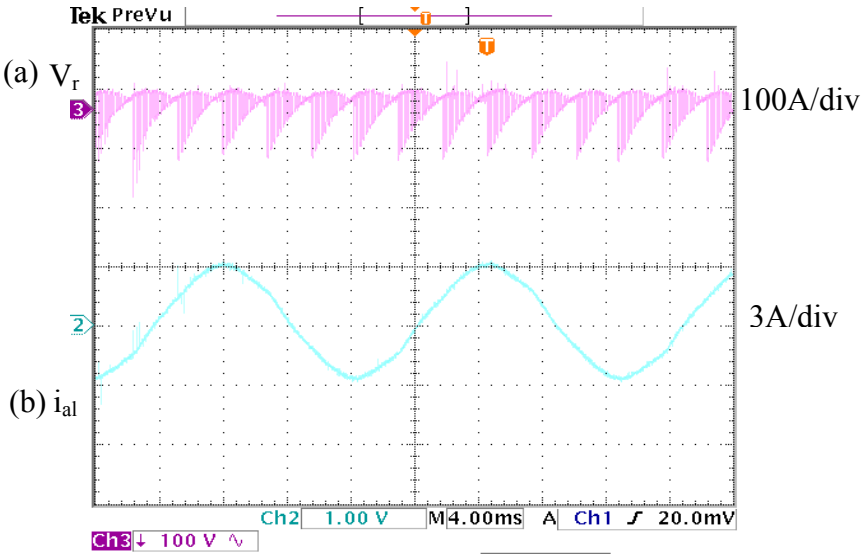


Figure 5.40 Open loop simulation results for Three phase CSI for discontinuous modulating signals DCM 3 with M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) Modulating Signals for all the six devices M_{ap}, M_{bp}, M_{cp}, M_{an}, M_{bn}, M_{cn} (II) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) DC voltage across the inverter, (b) phase 'a' load line current.

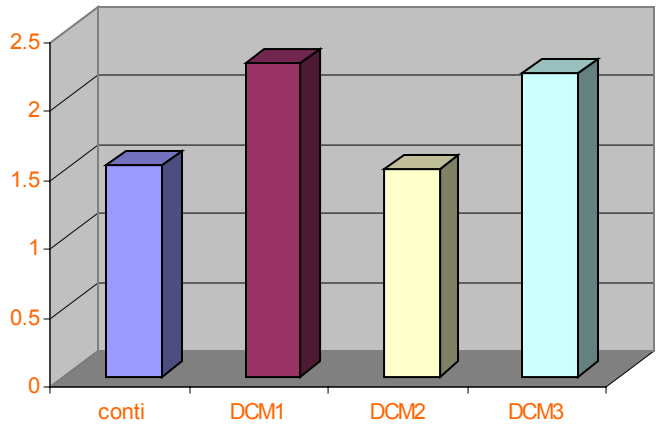


(I)

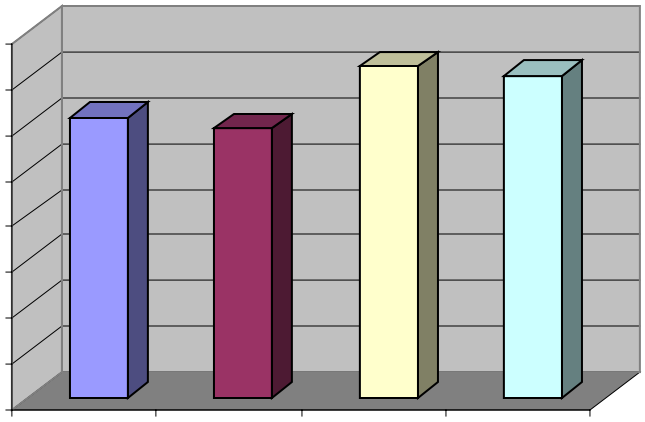


(II)

Figure 5.41 Open loop Experimental results for Three phase CSI for discontinuous modulating signals DCM 3 at M = 1.25 at f_s = 5kHz with input DC voltage = 100V, I_{dc} = 3A, R_L = 25Ω, (I) (a) phase 'a' device switching function, (b) phase 'a' line current, (c) input DC current, (d) phase 'a' capacitor voltage. (III), (a) inverter DC bus voltage, (b) Phase 'a' load line current.



(I)



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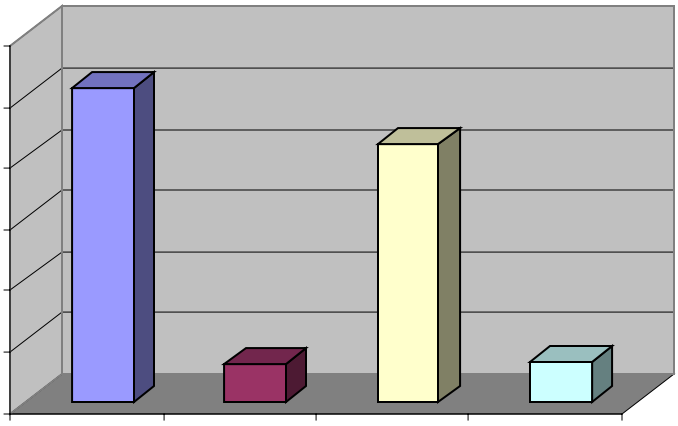


(III)

Figure 5.42 Comparison of the harmonics obtained from FFT of output currents for various modulating schemes at M = 0.85 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic (III) Comparison of the 5th harmonic

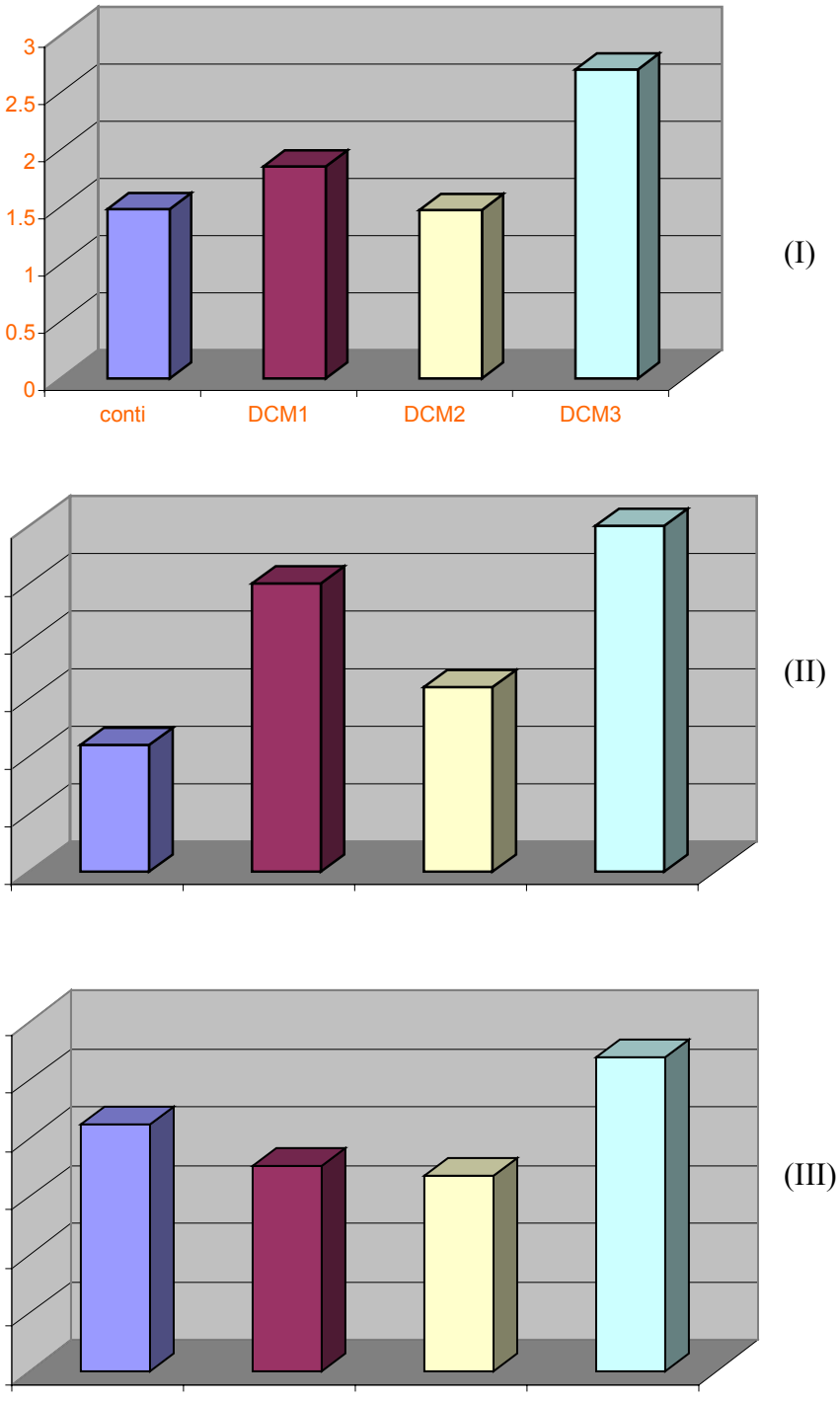


Figure 5.43 Comparison of the harmonics obtained from FFT of output voltages for various modulating schemes at M = 0.85 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic (III) Comparison of the 5th harmonic

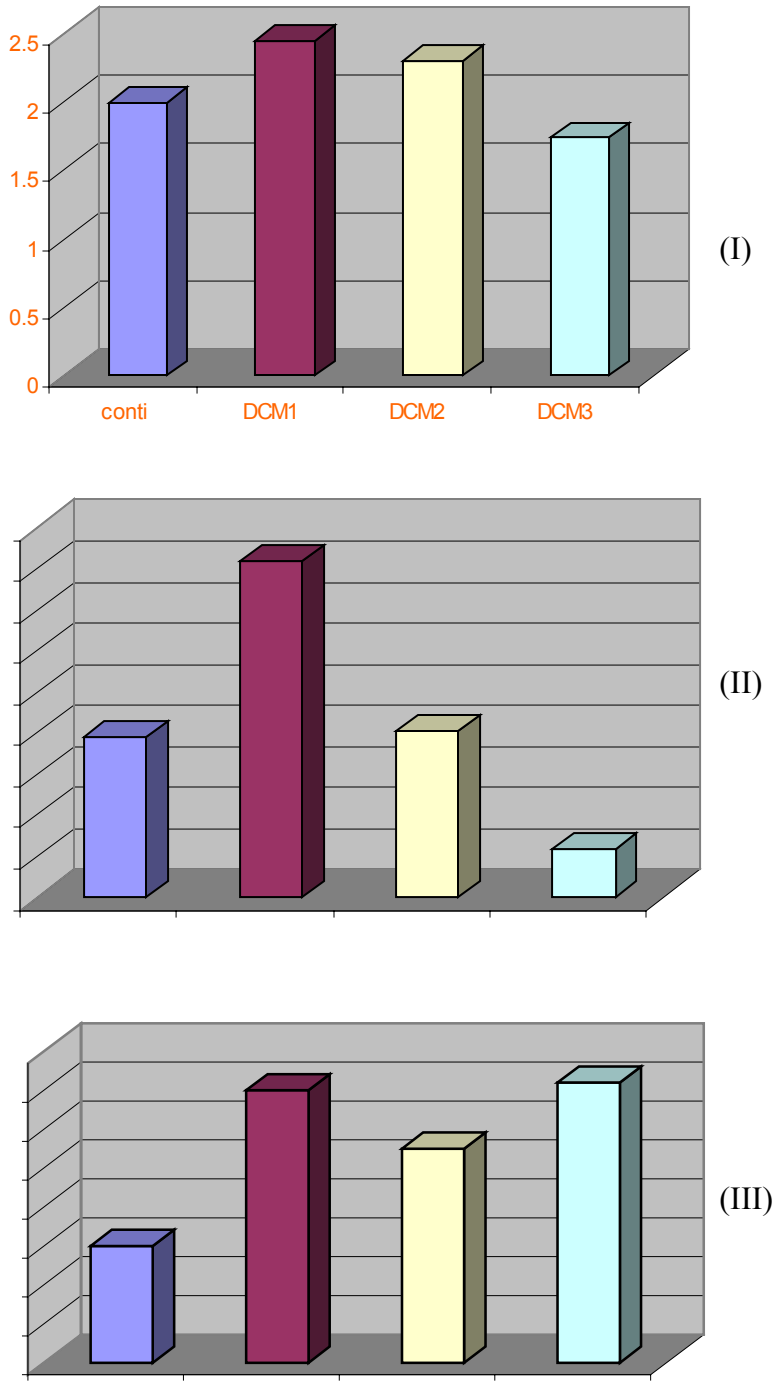
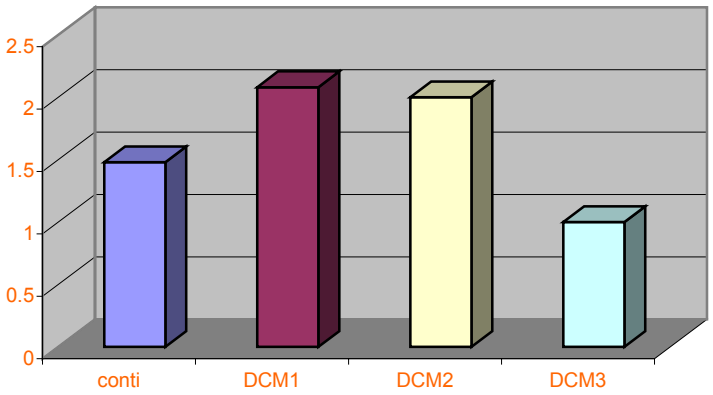
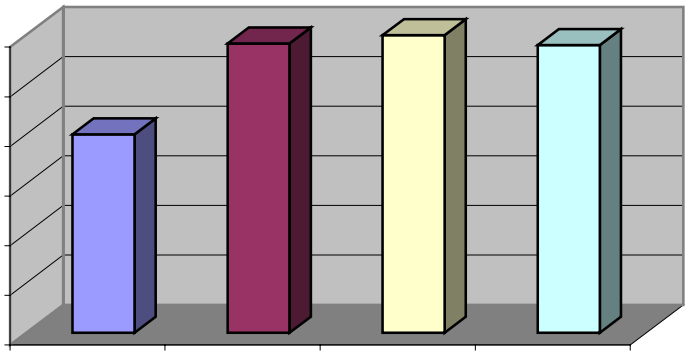


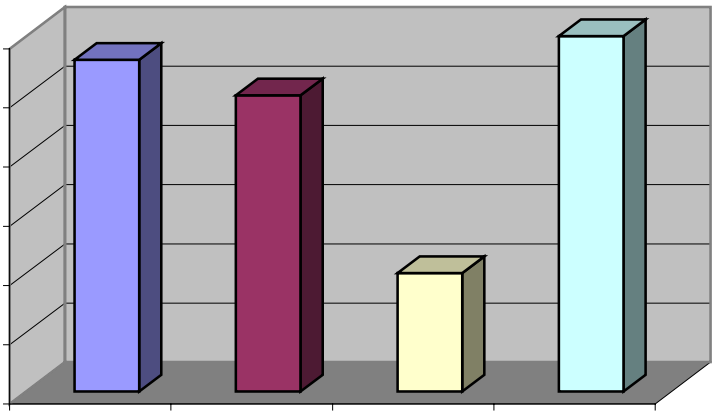
Figure 5.44 Comparison of the harmonics obtained from FFT of output currents for various modulating schemes at M = 1.25 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic (III) Comparison of the 5th harmonic



(I)

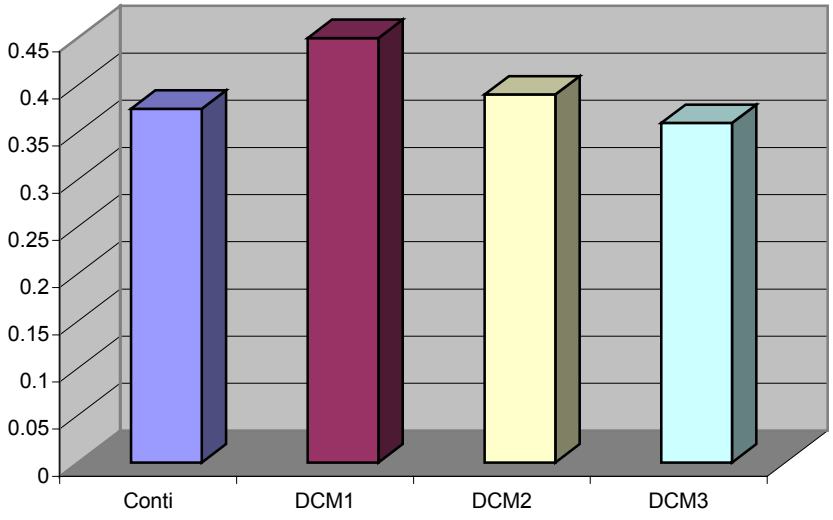


(II)

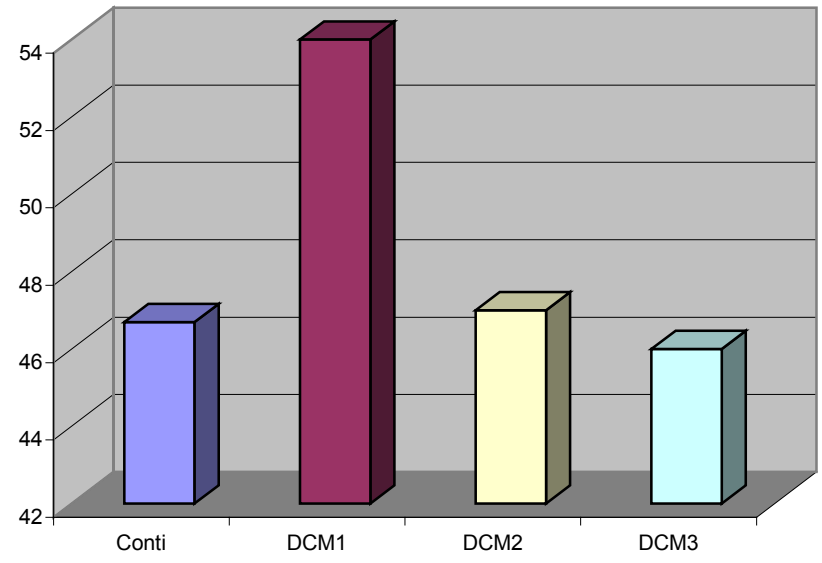


(III)

Figure 5.45 Comparison of the harmonics obtained from FFT of output voltages for various modulating schemes at M = 1.25 (I) Comparison of the 2nd harmonic, (II) Comparison of the 3rd harmonic (III) Comparison of the 5th harmonic

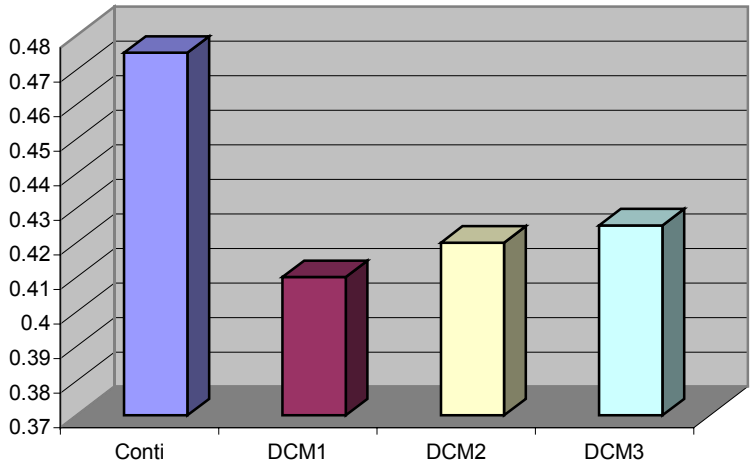


(I)

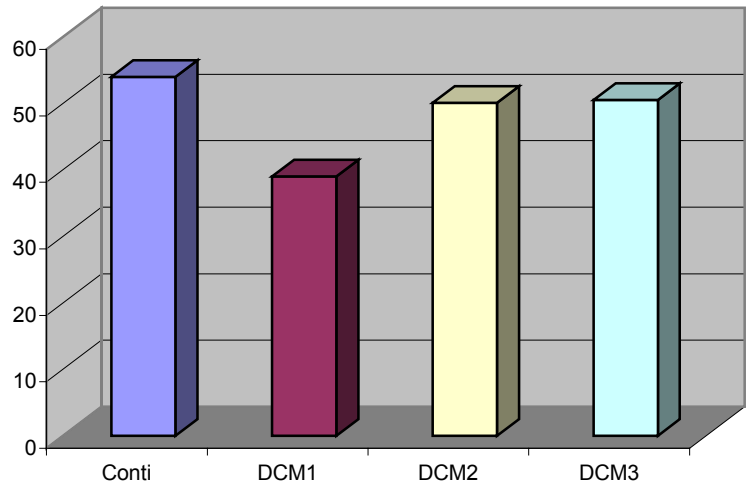


(II)

Figure 5.46 Comparison of the fundamental components obtained from FFT for different modulating signals M = 0.85 (I) output current (II) output voltage



(I)



(II)

Figure 5.47 Comparison of the fundamental components obtained from FFT for different modulating signals M = 1.25 (I) output current (II) output voltage

5.8 Observations from the Simulation and Experimental Results

Figures 5.15 to 5.30 show the simulation and experimental results using the modulation strategy developed in this chapter. Plots for continuous modulation and discontinuous modulation are presented in both the linear region and in over modulation region.

5.8.1 Continuous Modulation

Figures 5.22 to 5.25 show the simulation and experimental results for a continuous modulation in linear and over modulation region. Figures 5.26 and 5.27 show the FFT of the output current and voltage waveforms. In linear region modulation index is taken as 0.85 and in overmodulation it is taken as 1.25. In linear region it can be seen that in the final switching pattern, each device is turned OFF for a period of $120^{o.}$ And in overmodulation the device is continuously turned OFF completely for 180^{o} and turned ON continuously for 60^{o}. It is seen that the current gain is more in linear region of operation then in overmodulation. Even though in overmodulation it synthesizes less amount of current but the advantage is of reduction in switching losses. From the FFT plots it is seen the amount of harmonic components are less in linear region of operation but 3^{rd} and 5^{th} harmonics are comparatively more in overmodulation

5.8.2 Discontinuous Modulation

Figures 5.28 to 5.31 show the simulation and the experimental results for DCM1 in linear region and in overmodulation region of operation. Figures 5.32 and 5.33 show the FFT of the output current and voltage waveforms in both the regions of operation. Switching pattern of DCM1 is different form DCM2 and DCM3. Because in modulating signals of DCM1 clamping of the devices can be seen, which is not seen for the DCM2 and DCM3. From the final switching pattern of the DCM1 it is seen that a device completely clamps the top DC rail for 60^{o} and the bottom DC rail for 120^{o} , in the case of overmodulation the devices are continuously clamped to the positive DC rail for 60^{o} and bottom DC rail for 180^{o}. From the close study of the switching pattern, it is seen that there are no null states in the switching sequence, which says that all the time is used by active states in order to synthesize the desired currents. Also it is seen from the switching pattern that it follows a minimum transition path, which reduces the effective switching of the devices, that reduces the switching losses. From the FFT plots shown in Figures 5.32 and 5.33 it is seen that there are little amount of 3^{rd} and 5^{th} harmonic component present in current and voltage waveforms. By performing the experimentation for varying modulation index form 0.3 to 1.5 it is seen that the DCM1 gives high sophisticated waveforms of current and voltages. The drawback of DCM1 is that, there are no null states while transition from one active state to other active state. Their will be a effect of non-optimal switching, studied in section 4.5 which results in a glitch in the output current waveform which effects the insulation in the motor windings. And also from the

FFT analysis it can be seen that DCM1 does not give better waveform in lower modulation regions.

Figures 5.34 to 5.41 gives the simulation and experimental results for DCM2 and DCM3. In this set of modulating signals the final switching to the devices is continuously turned OFF for a period of 120^{o}. From the FFT of the output currents and voltage of the DCM2 and DCM3 it is seen that amount of harmonics are less in linear region when compared to that of a DCM1. Figures 5.42 to 5.45 show the comparison of 2^{nd}, 3^{rd}, 5^{th}, harmonics for different modulating signals and Figures 5.46 to 5.47 gives the comparison of the peak of the fundamental voltage and current synthesized by different modulators at M = 0.85 and M = 1.24. It is seen that the continuous has more gain in all the regions of operation and DCM1 has more gain in linear region of operation. From the above figures it can be said that the continuous modulating signal gives better current and voltage waveform compared to the other modulators both in linear and overmodulation region. Also DCM1 gives good performance waveform with a modulation index of 0.8 and more. The added advantage of the DCM1 is that in linear region the amount of switching loss in less compared to that of the other modulating signals. And in terms of gain, both continuous and DCM1 shows similar amount of gain in linear region. In overmodulation region almost all the modulators have the same gain.

CHAPTER 6

MODELING AND CONTROL OF THE THREE-PHASE CSR

6.1 Introduction

From the past 10 years or so, concerns about power quality and harmonics fed back into the utility have become increasingly important, because of the great increase in the use of electronic devices. Currently, the chief utility interface is the diode rectifier, in both single phase and three phase versions, with its highly distorted current input waveform. One of the results of the increased concern over power quality is more widespread replacement of diode rectifiers with active rectifiers to provide unity power factor (UPF) and low distorted currents.

Now with more drives incorporating active rectifiers, there are also choices to be made about which type to use. The most common active rectifier is the Voltage Source Rectifier (VSR) because its advantages of having simple modulation. VSR topology cannot be used in some low DC voltage applications because it cannot buck the DC voltage. An obvious choice for a buck type rectifier is a Current Source Rectifier (CSR), one of the most well-known converters. Other more complex and flexible rectifier topologies [C.19] are also possible allowing both bidirectional power flows, step-up, and step-down capabilities. This operation could be useful to applications, which operate below base speed with a significant load on the motor for more time. Some examples

include: electric vehicles, off road electric construction equipment, and compressor pumps.

Initially, phase controlled thyristors were extensively used for this application, since they are simple, economical, and reliable, requires no special means for commutation, for their operation. However, this type of converter has the following drawbacks: [C.14]

- Power factor decreases as the firing angle increases.
- Power factor is low for low output voltage or low output power. Therefore, high KVA is required from the utility line to satisfy load demand, which increases the operating cost.
- There is significant amount of ripple in the output voltage due to the presence of lower order harmonics in the line current, which requires large LC filter elements. It also can cause malfunction of sensitive devices connected to the utility lines, such as computers.

These drawbacks have led to the ongoing research towards converter structures, which will improve performance in these aspects. Forced commutated converters are able to overcome or reduce the limitations of thyristor-based converters. They are known to improve source and load–side performance. Reduction in KVA to meet the load demand can be obtained by achieving near unity or leading power factor at the supply side. Employing large number of pulses using PWM technique can reduce input side harmonic current and output side ripple voltage.

This section is going to discuss about the PWM operation of the three phase CSR, [C.8] it's modeling in a-b-c reference frame. Some aspects of the input side and output side filters design, steady state analysis of the rectifier are discussed. A new method of

designing control scheme for the rectifier for output DC voltage regulation under unity power factor operation has been proposed.

The main objectives in this section are to,

- Explain about the principle of operation of the three-phase buck rectifier.
- Develop a mathematical model of the ac-dc converter in a-b-c reference frame.
- Design techniques for the input side filter of the rectifier.
- Discuss about the steady state analysis of the rectifier.
- Designing the control structure for the rectifier for unity power factor operation and for output DC voltage regulation.
- Fabricate the prototype of the converter, pulsewidth modulation, gate drive, and closed loop controllers.

6.2 Operation of the Three-Phase Current Source Rectifier

A phase–controlled rectifier can be classified into two categories, depending on supply voltage and output voltage. Depending on its input supply, rectifiers can be divided into two categories: single–phase converter and three-phase converter. Each category can be divided into three subcategories: semi converter, full converter, and dual converter. The semi converter is a one–quadrant converter, it has one polarity of output voltage and current. Full converter, is a two quadrant converter; the output voltage can be positive or negative depending on the firing angle, but the output current has only one polarity the dual converter can be operated in four quadrants; its output voltage and current can be either positive or negative. From its output voltage, two most widely used three–phase rectifiers are the buck rectifier and the boost rectifier as in [C.15].

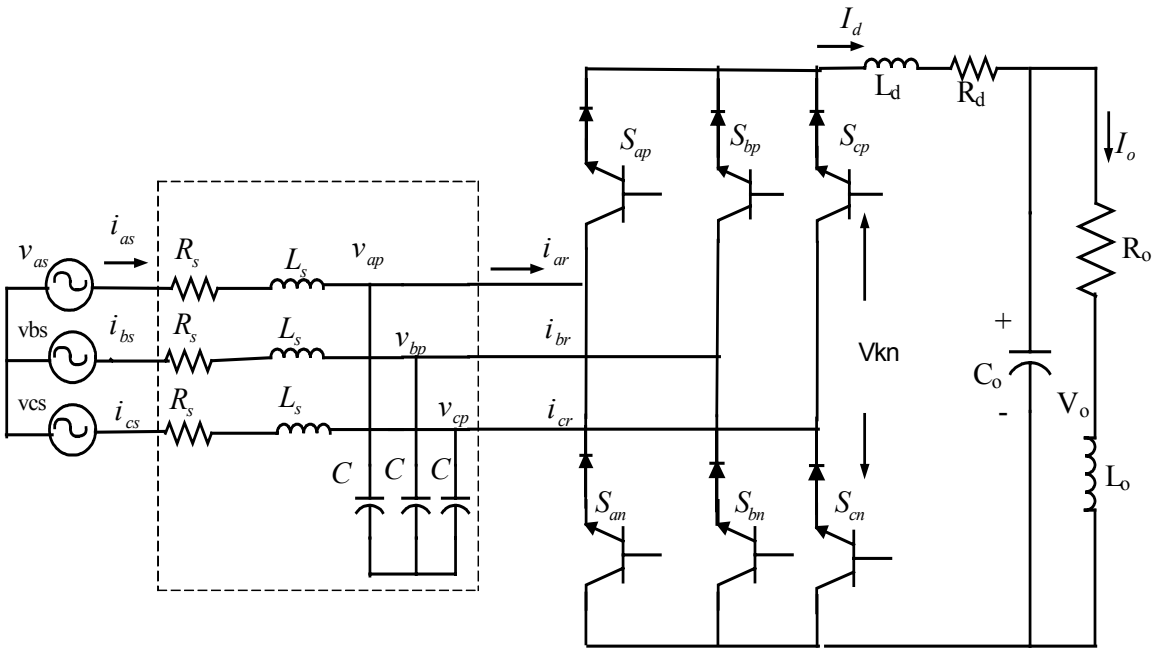


Figure 6.1 Schematic diagram of the three phase current source rectifier

The power topology of the CSR is shown in Figure 6.1. The three-phase rectifier is composed of a bridge circuit, with six unilateral switches, formed by the serial connection of an IGBT and a diode. Three–phase second order input filter R_s, L_s, C and a dc-link filter composed by a reactor L_d and a capacitor C_o. R_{dc} represent the equivalent resistance of the inductance L_d. Pulsewidth Modulation (PWM) rectifier regulates the dc-link current by adjusting the DC-link bus voltage. The input filter minimizes the harmonic injected into the AC mains by the PWM rectifier operation, with a good separation of switching and line frequency the AC-side filter can be implemented as a single LC filter. The inductance value of the link inductor is chosen to maintain a low ripple current, the ripple frequency will be related to the switching frequency and so the inductor value can be relatively small. Large inductance detracts from the transient response of the circuit. The output capacitor is not required to hold the output voltage over a main cycle and so it is considerably smaller than in a line commutated controlled

rectifier. In steady state a continuous current flows in the inductor to balance the output current.

6.3 Modes of Operation of CSR

Depending upon the pattern of the switching of the devices, the CSR can be operated in different modes of operation. Modes of operation of the CSR are as shown in Figures 6.2 to 6.8. The possible modes of operation of CSR can be divided as active states and null modes of operation. In an active mode of operation, the current flows from the source to the load. But in the case of null mode of operation the current does not flow from source to load.

Table 6.1 gives three-phase current and their stationary reference frame transformed quantities in all active and null states. In order to properly gate the power switches of the CSR, two main constraints must be met at any time.

Table 6.1 States of operation of the CSR.

ON Device	**ON Device**	$\mathbf{i_{as}}$	$\mathbf{i_{bs}}$	$\mathbf{i_{cs}}$	$\mathbf{i_{qq}}$	$\mathbf{\sqrt{3}\ I_{dd}}$
S_{ap}	S_{bn}	I_d	$-I_d$	0	I_d	I_d
S_{ap}	S_{cn}	I_d	0	$-I_d$	I_d	$-I_d$
S_{bp}	S_{an}	$-I_d$	I_d	0	$-I_d$	$-I_d$
S_{bp}	S_{cn}	0	I_d	$-I_d$	0	$-2I_d$
S_{cp}	S_{an}	$-I_d$	0	I_d	$-I_d$	I_d
S_{cp}	S_{bn}	0	$-I_d$	I_d	0	$2I_d$
S_{ap}	S_{an}	0	0	0	0	0
S_{bp}	S_{bn}	0	0	0	0	0
S_{cp}	S_{cn}	0	0	0	0	0

(1) The AC side is of voltage source type due to the input filter and must not be short-circuited, thus implies that, no two top switches and two bottom switches should be closed at any time.

(2) The DC bus is of current source type it cannot be opened. Therefore, there must be at least one top and one bottom switch closed at all times.

From both constrains, it can be summarized that at any time only one top and one bottom switch must be closed;

i.e $S_{ap} + S_{bp} + S_{cp} = 1$ (6.1)

$S_{an} + S_{bn} + S_{cn} = 1$

$S_{ap} * S_{bp} = S_{ap} * S_{cp} = S_{bp} * S_{cp} = S_{an} * S_{bn} = S_{an} * S_{cn} = S_{bn} * S_{cn} = 0.$ (6.2)

Figures 6.2 to 6.7 shows the circuit diagram for active mode of operation of the CSR, in which one device from the top and another device from a different phase in the bottom are turned ON. Figure 6.8 shows the circuit diagram for the null mode of operation.

MODE I

	Device ON
Top	S_{ap}
Bottom	S_{bn}

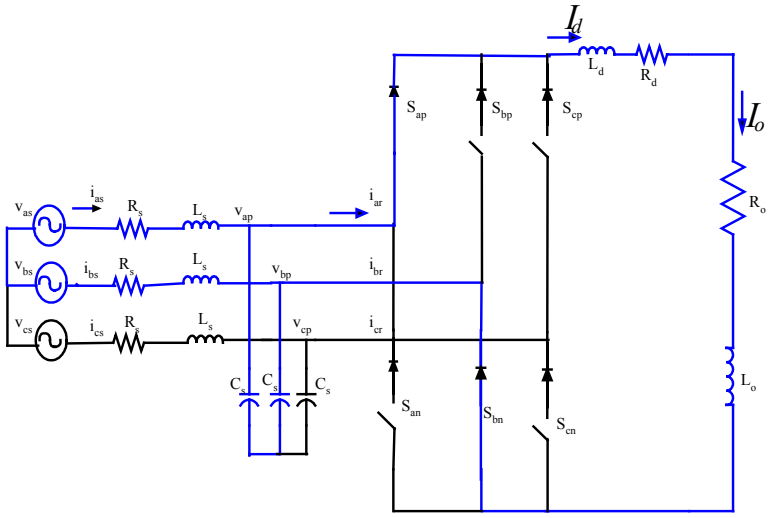


Figure 6.2 Circuit diagram of CSR showing Mode I of operation.

In this mode of operation, phase 'a' top device and phase 'b' bottom device are turned ON, such that the current I_d flows through the i_{as} and $-I_d$ flows through the i_{bs}. This state of operation is an active state because power is transferred from input side to output side.

MODE II

In this mode of operation, phase 'a' top device and phase 'c' bottom device are turned ON, such that the current I_d flows through the i_{as} and $-I_d$ flows through the i_{cs}. This state of operation is an active state because power is transferred from input side to output side.

	Device ON
Top	S_{ap}
Bottom	S_{cn}

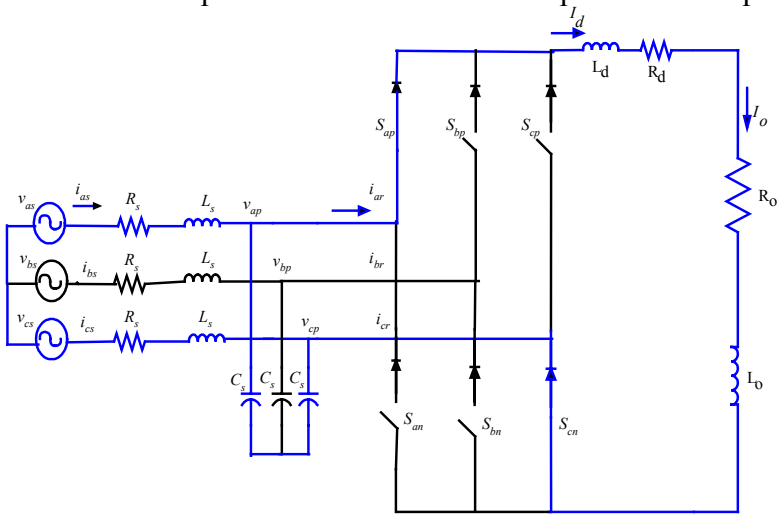


Figure 6.3 Circuit diagram of CSR showing Mode II of operation.

MODE III

	Device ON
Top	S_{bp}
Bottom	S_{bn}

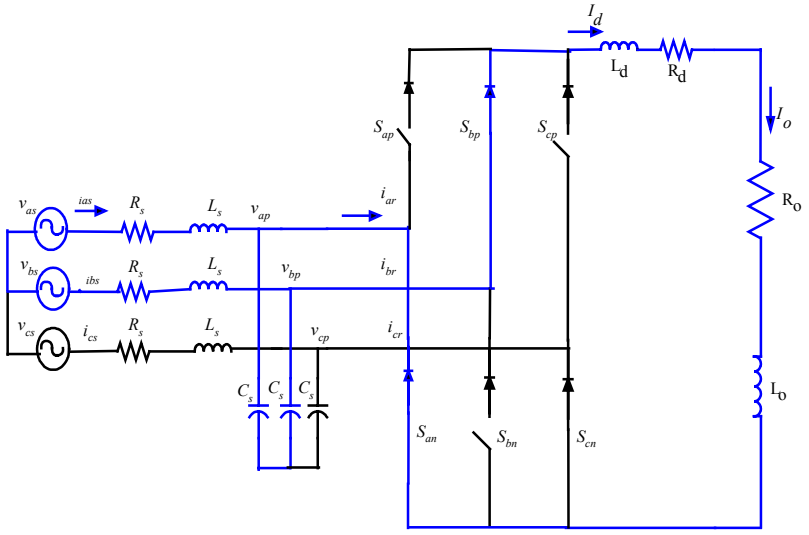


Figure 6.4 Circuit diagram of CSR showing Mode III of operation.

In this mode of operation, phase 'b' top device and phase 'a' bottom device are turned ON, such that the current I_d flows through the I_{bs} and $-I_d$ flows through the I_{as}. This state of operation is an active state of operation because there is transfer power from input side to output side.

MODE VI

In this mode of operation, phase 'b' top device and phase 'c' bottom device are turned ON, such that the current I_d flows through the I_{bs} and $-I_d$ flows through the I_{cs}. This state of operation is an active state of operation because there is transfer power from input side to output side.

	Device ON
Top	S_{ap}
Bottom	S_{cn}

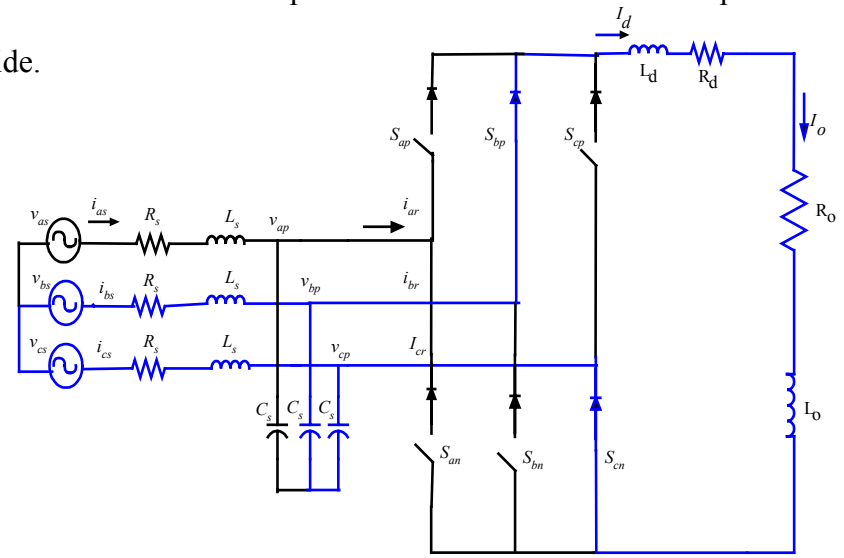


Figure 6.5 Circuit diagram of CSR showing Mode IV of operation.

MODE V

	Device ON
Top	S_{cp}
Bottom	S_{an}

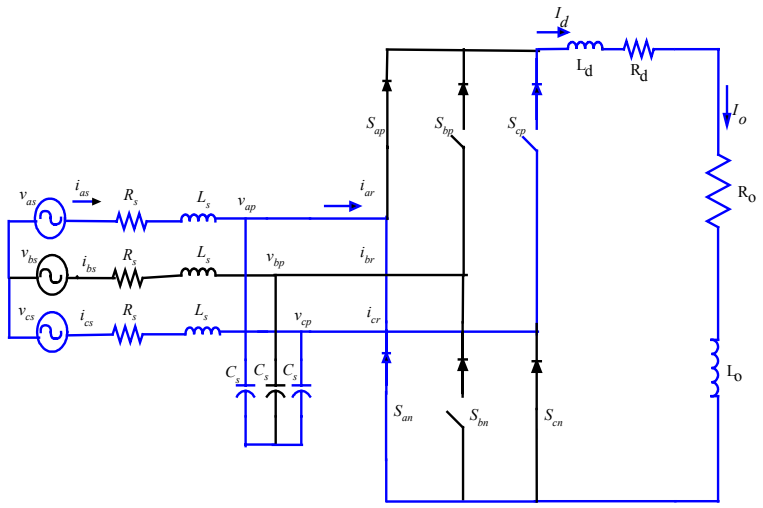


Figure 6.6 Circuit diagram of CSR showing Mode V of operation.

In this mode of operation, phase 'c' top devices and phase 'a' bottom devices are turned ON, such that the current I_d flows through the I_{cs} and $-I_d$ flows through the I_{as}. This state of operation is an active state of operation because there is transfer power from input side to output side.

MODE VI

In this mode of operation, phase 'c' top devices and phase 'b' bottom devices are turned ON, such that the current I_d flows through the I_{cs} and $-I_d$ flows through the I_{bs}. This state of operation is an active state of operation because there is transfer power from input side to output side.

	Device ON
Top	S_{cp}
Bottom	S_{bn}

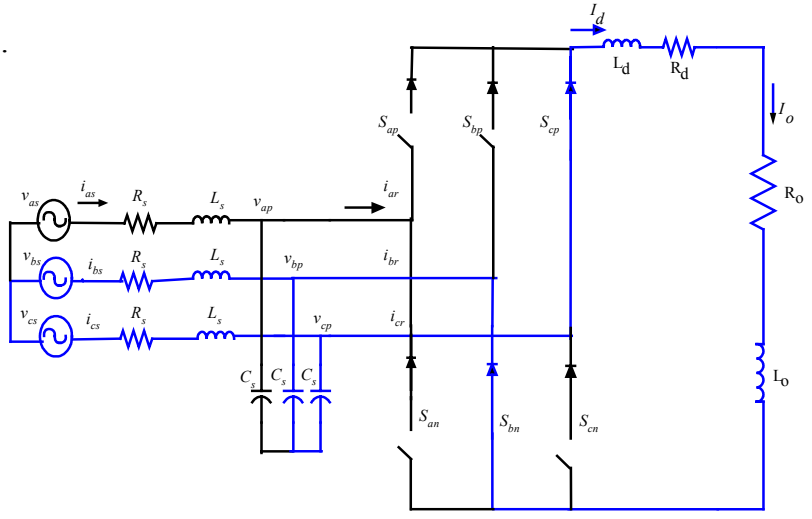
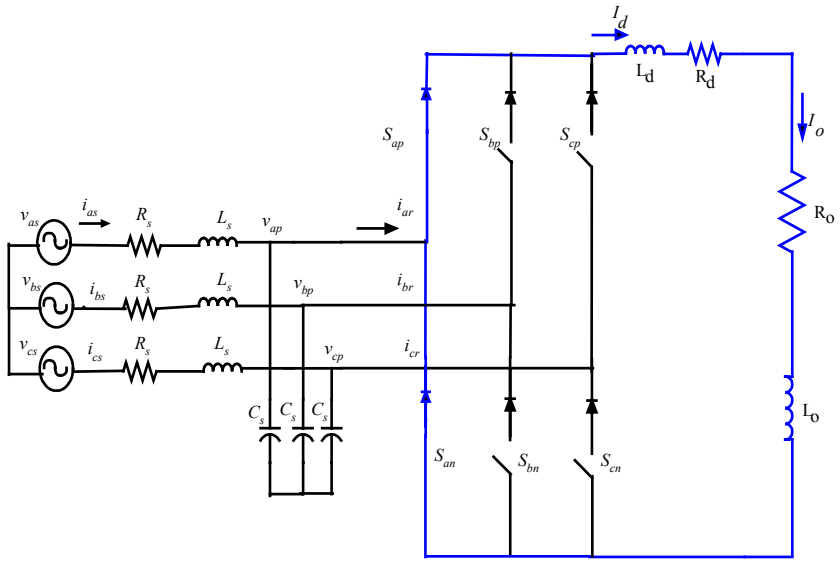


Figure 6.7 Circuit diagram of CSR showing Mode VI of operation.

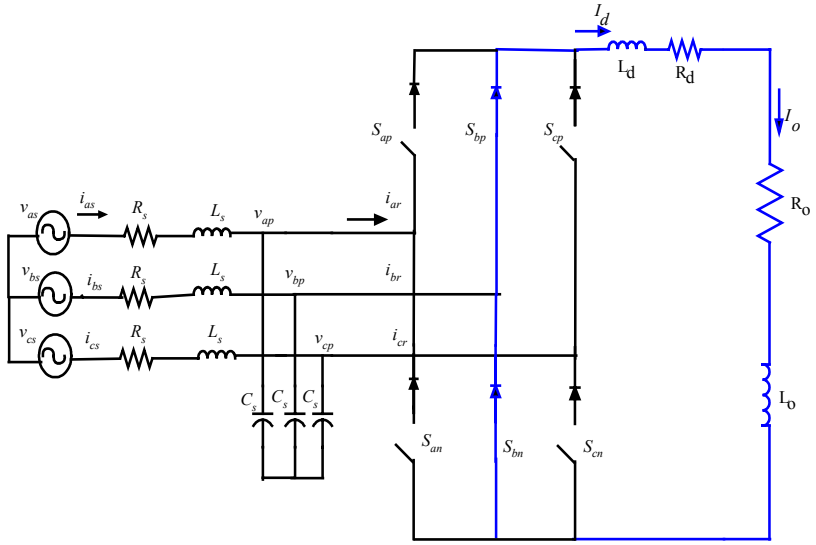
MODE VII

	Device ON
Top	S_{ap}
Bottom	S_{an}



MODE VIII

	Device ON
Top	S_{bp}
Bottom	S_{bn}



MODE IX

	Device ON
Top	S_{cp}
Bottom	S_{cn}

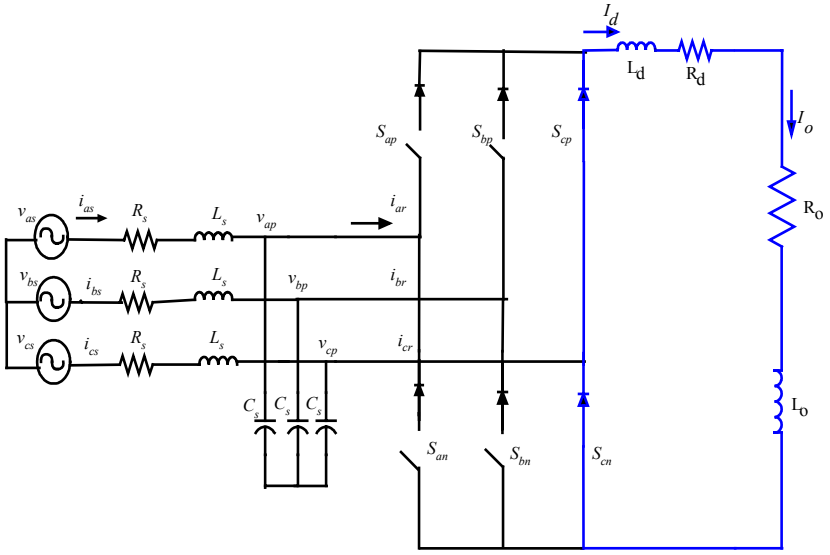


Figure 6.8 Circuit diagrams of CSR showing Modes VII, VIII, IX of operation.

Figure 6.8 shows the circuit diagram of the null mode of operation in which operation both the top and bottom devices of the same phase are turned ON at the same time. In all these null modes of operation there is no flow of current from input side to output side.

6.4 Modeling of the Current Source Rectifier

Figure 6.1 is the schematic diagram of a three phase current source type rectifier with all the input and out quantities of the rectifier described in Table 6.2.

Table 6.2 Terminology used in modeling of CSR

Parameters	**Description**
v_{as},v_{bs},v_{cs}	Three phase voltages
v_{ap},v_{bp},v_{cp}	Three phase capacitor voltages
i_{ar}, i_{br}, i_{cr}	Three phase currents into the rectifier
i_{as}, i_{bs}, i_{cs}	Three phase supply currents
L_d	Output side filter inductor
C_o	Output side capacitor
R_o	Load resistor
I_d	Output DC current
I_o	Output load current
L_s	Input side inductance
C	Input side capacitance
R_s	Input side line resistors
S_{ap}, S_{bp}, S_{cp}	Top three devices
S_{an}, S_{bn}, S_{cn}	Bottom three devices

Model equations of the rectifier in the a-b-c reference frame can be obtained by writing the Kirchoff's voltage and current law for the above CSR topology.

Expressions for the input side voltages are given as

$$v_{as} = r_s i_{as} + L_s p i_{as} + v_{ap}$$

$$v_{bs} = r_s i_{bs} + L_s p i_{bs} + v_{bp} \tag{6.3}$$

$$v_{cs} = r_s i_{cs} + L_s p i_{cs} + v_{cp}\,.$$

Equations across the three phase input side capacitors as

$$Cpv_{ap} = i_{as} - I_d (S_{ap} - S_{an})$$

$$Cpv_{bp} = i_{bs} - I_d \left(S_{bp} - S_{bn}\right) \tag{6.4}$$

$$Cpv_{cp} = i_{cs} - I_d (S_{cp} - S_{cn})\,. \tag{6.5}$$

Unfiltered currents into the rectifier are as,

$$i_{ar} = (S_{ap} - S_{an}) I_d$$

$$i_{br} = (S_{bp} - S_{bn}) I_d \tag{6.6}$$

$$i_{cr} = (S_{cp} - S_{cn}) I_d$$

where I_d is the output side DC current.

By writing KVL at the output inductor

$$L_o p I_L + r_o I_L = V_{kn} - V_o \tag{6.7}$$

$$V_{kn} = v_{ap}\left(S_{ap} - S_{an}\right) + v_{bp}\left(S_{bp} - S_{bn}\right) + v_{cp}\left(S_{cp} - S_{cn}\right). \tag{6.8}$$

Output capacitor equation can be written as

$$C_o p V_o = I_d - I_o\,. \tag{6.9}$$

Output load inductor voltage can be expressed as

$$L_o pI_o = V_{co} - I_o R_o . \tag{6.10}$$

These equations in a-b-c reference frame were used to simulate the CSR. The above derived model equations can be transformed into q-d-o synchronous reference frame for designing the controller.

6.5 Modeling of CSR in q-d-o Synchronous Reference Frame

The q-d-o model of the three-phase CSR in synchronous reference frame is obtained by applying transformation to Equations (6.3) to (6.10). Reference frame transformations explained in [A.3].

q-d-o quantities can be obtained from the a-b-c coordinates through the following relationship.

$$f_{qdos} = T(\theta).f_{abc} \text{ where} \tag{6.11}$$

$$T(\theta) = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta-\beta) & \cos(\theta+\beta) \\ \sin(\theta) & \sin(\theta-\beta) & \sin(\theta+\beta) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \text{ and } \beta = \frac{2\pi}{3}. \tag{6.12}$$

The relations that will be used during the transformations are derived as below using Equations (6.3) to (6.10).

$$V_{asbscs} = \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix},\ I_{asbscs} = \begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix},\ V_{apbpcp} = \begin{bmatrix} v_{ap} \\ v_{bp} \\ v_{cp} \end{bmatrix},\ S_{abc} = \begin{bmatrix} S_{ap} \\ S_{bp} \\ S_{cp} \\ S_{an} \\ S_{bn} \\ S_{cn} \end{bmatrix}. \tag{6.13}$$

$$V_{qdo} = \begin{bmatrix} V_{qs} \\ V_{ds} \\ V_{os} \end{bmatrix},\quad I_{qdos} = \begin{bmatrix} I_{qs} \\ I_{ds} \\ I_{os} \end{bmatrix}\quad S_{qdo} = \begin{bmatrix} S_{qs} \\ S_{ds} \\ S_{os} \end{bmatrix} \tag{6.14}$$

$$V_{qdo} = T(\theta).V_{asbscs} \tag{6.15}$$

$$V_{qdp} = T(\theta).V_{apbpcp} \tag{6.16}$$

$$I_{qdos} = T(\theta).I_{qdos} \tag{6.17}$$

$$S_{qdos} = T(\theta)S_{apbpcp} \tag{6.18}$$

Also the inverse transformation can be applied as

$$f_{abc} = T^{-1}(\theta) f_{qdo} \tag{6.19}$$

$$T^{-1}(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos(\theta - \beta) & \sin(\theta - \beta) & 1 \\ \cos(\theta + \beta) & \sin(\theta + \beta) & 1 \end{bmatrix}. \tag{6.20}$$

Now define $\theta = \int \omega dt + \theta_o$ where θ_o is the initial reference angle and $\frac{d\theta}{dt} = \omega$

writing the above a-b-c model equations in the matrix form

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} \begin{bmatrix} i_{as} \\ i_{bs} \\ i_{cs} \end{bmatrix} + \begin{bmatrix} L_s & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & L_s \end{bmatrix} \begin{bmatrix} pi_{as} \\ pi_{bs} \\ pi_{cs} \end{bmatrix} + \begin{bmatrix} v_{ap} \\ v_{bp} \\ v_{cp} \end{bmatrix}. \tag{6.21}$$

Transforming the above equation to synchronous reference frame using the transformation matrix $T(\theta)$

$$V_{qs} = r_s I_{qs} + L_s pI_{qs} + \omega L_s I_{ds} + V_{qp} \tag{6.22}$$

$$V_{ds} = r_s I_{ds} + L_s pI_{ds} - \omega L_s I_{qs} + V_{dp} \tag{6.23}$$

$$V_{os} = r_s I_{os} + L_s pI_{os} . \tag{6.24}$$

Similarly applying the transformation for the capacitor equations (6.4)

$$CpV_{qp} + C\omega V_{dp} = I_{qs} - (S_{qp} - S_{qn})I_d \tag{6.22}$$

$$CpV_{dp} - C\omega V_{qp} = I_{ds} - (S_{dp} - S_{dn})I_d \tag{6.23}$$

$$CpV_o = I_{os} - (S_{po} - S_{no})I_d \tag{6.24}$$

where

$$S_{qdop} = T(\theta)\lfloor S_{abcp} \rfloor \tag{6.25}$$

$$S_{qdon} = T(\theta)[S_{abcn}]. \tag{6.26}$$

$T(\theta)$ is the transformation matrix

where

$$S_{qp} = \frac{2}{3}\left[S_{ap}\cos(\theta) + S_{bp}\cos(\theta - \beta) + S_{cp}\cos(\theta + \beta)\right] \tag{6.27}$$

$$S_{dp} = \frac{2}{3}\left[S_{ap}\sin(\theta) + S_{bp}\sin(\theta - \beta) + S_{cp}\sin(\theta + \beta)\right] \tag{6.28}$$

$$S_{0p} = \frac{1}{3}\left[S_{ap} + S_{bp} + S_{cp}\right] \tag{6.29}$$

and

$$S_{qn} = \frac{2}{3}\left[S_{an}\cos(\theta) + S_{bn}\cos(\theta - \beta) + S_{cn}\cos(\theta + \beta)\right] \tag{6.30}$$

$$S_{dn} = \frac{2}{3}\left[S_{an}\sin(\theta) + S_{bn}\sin(\theta - \beta) + S_{cn}\sin(\theta + \beta)\right] \tag{6.31}$$

$$S_{0n} = \frac{1}{3}\left[S_{an} + S_{bn} + S_{cn}\right]. \tag{6.32}$$

Form the constrains of the CSR defined in Equations (6.1) and (6.2) we have

$$S_{0p} = S_{on} = \frac{1}{3}. \tag{6.33}$$

$$L_d pI_d + r_d I_d = \frac{3}{2}(V_{qp}(S_{qp} - S_{dp}) + V_{dp}(S_{qn} - S_{dn})) \tag{6.34}$$

$$C_d pV_o = I_d - I_o. \tag{6.35}$$

In the above equations V_{qs} ,V_{ds} are the transformed input side voltages, I_{qs} and I_{ds} are the transformed input side line currents, V_{qp} and V_{dp} are transformed input side capacitor voltages, while $S_{qp,}$ $S_{dp,}$ $S_{qn,}$ S_{dn} are the transformed switching functions.

6.6 Input Filter Design

In practice, due to the presence of imperfections such as asymmetry in gating signals, asynchronism in the PWM method, switching delays, and other inaccuracies in hardware implementation, some unwanted harmonics with small amplitude exist in the system. The filter can amplify the harmonics if no damping is provided.

Some of the practical considerations in the design of filter parameters are:

- The effect of the filter on the converter performance and on the rating of the converter components has to be considered.

- Considerations related to system efficiency, power factor, kilovolt ampere rating of the filter components and cost of the filter.

Design of LC filters involves the positioning of the resonant frequency to meet the harmonic attenuation requirements (THD), and introducing damping at the resonant frequency to avoid amplification of residual harmonics. Similar approach used in the design of the input side filter for the PWM rectifier [C.16, C.17]. In order to simplify the design of L_d and C_s, a maximum peak-to-peak ripple criterion is used. On the other hand, L_s is designed to obtain a desired resonant frequency at the input AC filter. Thus it is possible to avoid any resonance due to the PWM operation of the CSR (Harmonics around N, 2N, …, where N is the normalized sample frequency), and non-characteristics harmonics (fifth, seventh).

In designing the dc-link inductor for the rectifier, the following assumptions are considered:

- The design of the dc-link inductor is done assuming a small peak-to-peak dc-link current of 20% of the normal dc–link current.

- It is assumed that the harmonics in the supply voltage are zero.

The peak-peak dc current can be expressed as

$$\Delta i_{dc} = \frac{\sqrt{3}V_{qs}}{L_{dc}} G_{dc} M_d T_s = K_{Ldc} I_{dc} \tag{6.36}$$

where Ts is the sampling time or (= $1/f_{sn}$), f_{sn} represents the normalized switching frequency.

- G_{ac} is the ac term ratio of maximum value (peak) of the fundamental component of the ac term to the amplitude of the unfiltered pulses comprising the same term.

- G_{dc} term gain is the ratio of the maximum value of the DC component of the term to the maximum amplitude of the unfiltered pulses comprising the same term.

K_{Ldc} is a constant to fix the permissible DC current ripple. It is generally taken as K_{Ldc} = 0.20 p.u. The expression for output DC current I_{dc} is given as $I_{dc} = G_{ac}$ M where G_{ac} is the ac gain and M is the modulation magnitude.

Hence from the above two equations per the unit value of the reactance are given:

$$X_{Ldc} = \frac{2\pi\sqrt{3}}{K_{Ldc}} \frac{G_{dc}}{G_{ac}} p.u \, . \tag{6.37}$$

The input side capacitor (C_i) is designed to meet a given peak–to-peak voltage ripple requirements. It is assumed that for a better design all the current harmonics are absorbed by the capacitor. This condition assumes that the frequency of the harmonics injected by the PWM operation of the CSR is higher than the resonant frequency of the input filter.

The normalized ac capacitor reactance is given by

$$X_{ci} = \frac{K_{ci} N}{\pi} p.u \ . \tag{6.38}$$

The input side AC inductor (L_i) is calculated using a desired normalized resonant frequency for the input filter (f_{rn}) and the resonant frequency is usually chosen lower than the half the normalized switching frequency (f_{sn}) and higher than low frequency due to transient over modulation Thus the reactance is given by

$$X_{Li} = \frac{X_{ci}}{f_{rn}^{\ 2}}\, p.u\ . \tag{6.39}$$

$\omega_r = \sqrt{L_i C_i}$ is the resonant angular frequency of the input filter, f_{rn} is the normalized resonant frequency.

6.7 Steady State Analysis

The steady state solution is very important because the dynamic response of these non-linear equations is related to the steady state operating point. It can also provide the knowledge of relationship between state variables and system parameters in steady-state operation [C.5, C.10].

If a system is in steady state, then rate of change of the system variables are considered as zero i.e., all the derivative terms are made zero in steady state analysis. Hence by substituting the derivative terms as zero in the above equations

$$V_{qs} = r_s I_{qs} + \omega L_s I_{ds} + V_{qp} \tag{6.40}$$

$$V_{ds} = r_s I_{ds} - \omega L_s I_{qs} + V_{dp} \tag{6.41}$$

$$I_{qs} - (S_{qp} - S_{qn}) I_d - C\omega V_{dp} = 0 \tag{6.42}$$

$$I_{ds} - (S_{dp} - S_{dn}) I_d + -CwV_{qp} = 0 \tag{6.43}$$

$$r_d I_d = \frac{3}{2}[V_{qp}(S_{qp} - S_{qn}) + V_{dp}(S_{dp} - S_{dn})] - V_o \tag{6.44}$$

$$V_o - I_o r_L = 0\,. \tag{6.45}$$

From section 3.9 the expression for the switching functions, i.e., from Equations 3.46

$$S_{abcp} = \frac{1}{3} + \sigma_{abcp} \quad , \quad S_{abcn} = \frac{1}{3} + \sigma_{abcn} \tag{6.46}$$

where $\sigma_{abcp} = \frac{I_{abc}}{2I_d}$ and $\sigma_{abcn} = -\frac{I_{abc}}{2I_d}$. (6.47)

By transforming the above switching functions into synchronous reference frame by applying transformation matrix

$$S_{qdp} = T(\theta)\left[\frac{1}{3} + \sigma_{abcp}\right] \text{ and } \; S_{qdn} = T(\theta)\left[\frac{1}{3} + \sigma_{abcn}\right]. \tag{6.48}$$

Then Equation (6.48) transforms into

$$S_{qdop} = \sigma_{qdop} \; , \; S_{qdon} = \sigma_{qdon} \, . \tag{6.49}$$

But from Equation (6.47) $\sigma_{abcp} = -\sigma_{abcn}$

Then expression (6.49) becomes

$S_{qdop} = -S_{qdon}$. Hence from this condition

$$S_{qp} = -S_{qn} \;\; \text{And} \;\; S_{dp} = -S_{dn} \, . \tag{6.50}$$

Hence, by substituting the above conditions into Equation (6.42) to (6.44)

$$I_{qs} - (2S_{qp})I_d - C\omega V_{dp} = 0 \tag{6.51}$$

$$I_{ds} - (2S_{dp})I_d + -CwV_{qp} = 0$$

$$r_d I_d = \frac{3}{2}[V_{qp}(2S_{qp}) + V_{dp}(2S_{dp})] - V_o \, . \tag{6.52}$$

Form the above equations considering

$$2S_{qp} = M_q \text{ and } 2S_{dp} = M_d . \tag{6.53}$$

By substituting the above condition in Equations (6.40) to (6.45)

$$V_{qs} = r_s I_{qs} + \omega L_s I_{ds} + V_{qp} \tag{6.54}$$

$$V_{ds} = r_s I_{ds} - \omega L_s I_{qs} + V_{dp} \tag{6.55}$$

$$I_{qs} - (M_q) I_d - C\omega V_{dp} = 0 \tag{6.56}$$

$$I_{ds} - (M_d) I_d + -CwV_{qp} = 0 \tag{6.57}$$

$$r_d I_d = \frac{3}{2}[V_{qp}(M_q) + V_{dp}(M_d)] - V_o \tag{6.58}$$

$$V_o - I_o r_L = 0 . \tag{6.59}$$

Calculations are simplified by aligning the q-axis with phase 'a' of the supply voltage to make V_{ds} identically equal to zero.

The input reactive power at the input supply is defined as

$$Q = \frac{3}{2}(V_{qs} I_{ds} - V_{ds} I_{qs}) . \tag{6.60}$$

For unity power factor operation at the source end, the input reactive power has to be zero, which means that the reactive power Q has to be made zero. By considering the input supply as a balanced source hence by transforming the balanced voltages into synchronous reference frame $V_{ds} = 0$, by equating expression (6.60) to zero and since V_{ds} is zero, current I_{ds} has to be zero for unity power factor. Using the above condition for the

unity power factor and Equations (6.54) to (6.59) be solved in order to attain the values of M_q and M_d for different values of DC voltage.

6.8 Steady State Results

The input and the output side inductor and capacitors were designed to limit the maximum current harmonics and voltage ripple below 5 percent. The values of the filter parameters are as given L_i = 3mH, C = 60μF, L_d = 50mH, C_o = 100μF. Using the above filter parameters and for the RMS supply voltage of 110Volts per phase and load a resistance of 25Ω, corresponding values of M_q and M_d are obtained for unity power factor operation. Plots are given for Modulation index (M) vs Phase angle, Modulation index (M) vs Output capacitor voltage, Modulation index (M) vs Output current, and Modulation index (M) vs Input capacitor voltage. Phase angle 'φ' can also be defined as the modulation angle is given as the angle between M_q and M_d; i.e., $\varphi = \tan^{-1}(M_d / M_q)$.

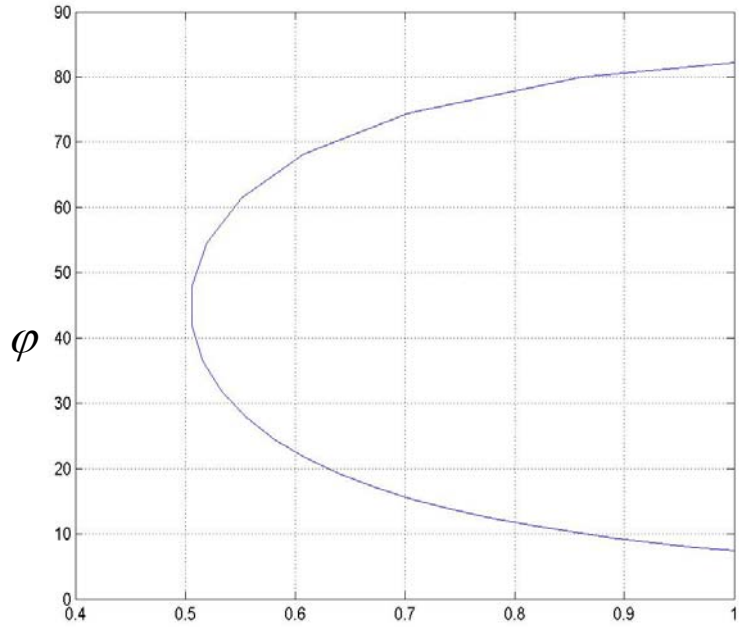


Figure 6.9 Plot of Modulation Index Versus Input displacement phase angle for various values of output voltage under unity power factor operation.

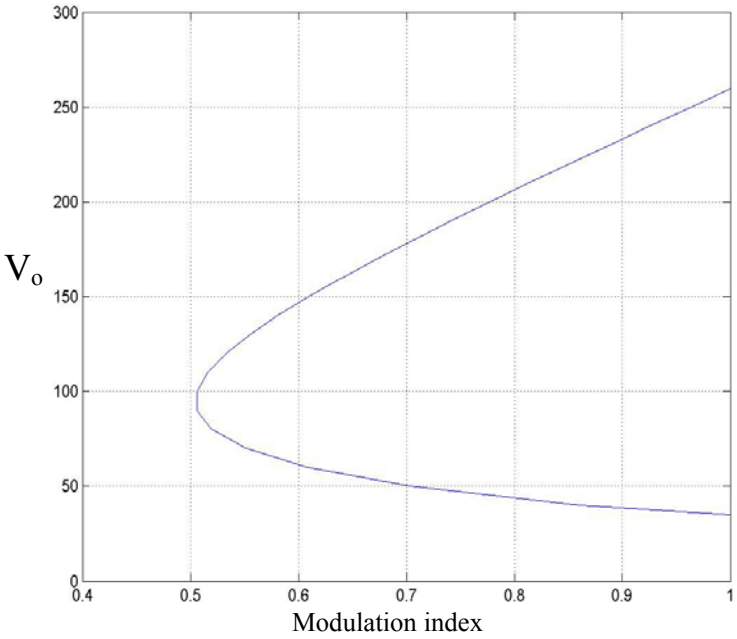


Figure 6.10 Plot of Modulation Index Versus Output Capacitor Voltage for various value of output voltage under unity power factor operation.

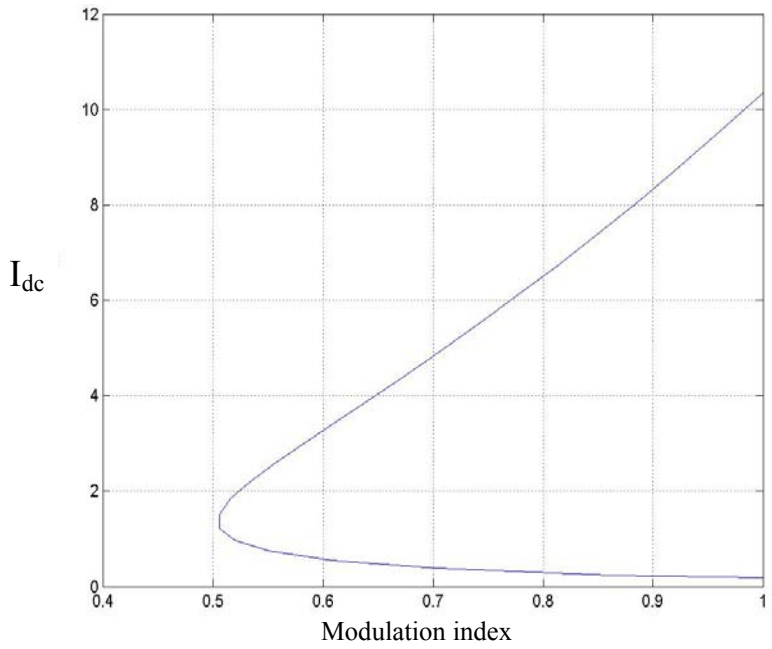


Figure 6.11 Plot of Modulation Index Versus Output DC current for various values of output voltage under unity power factor operation

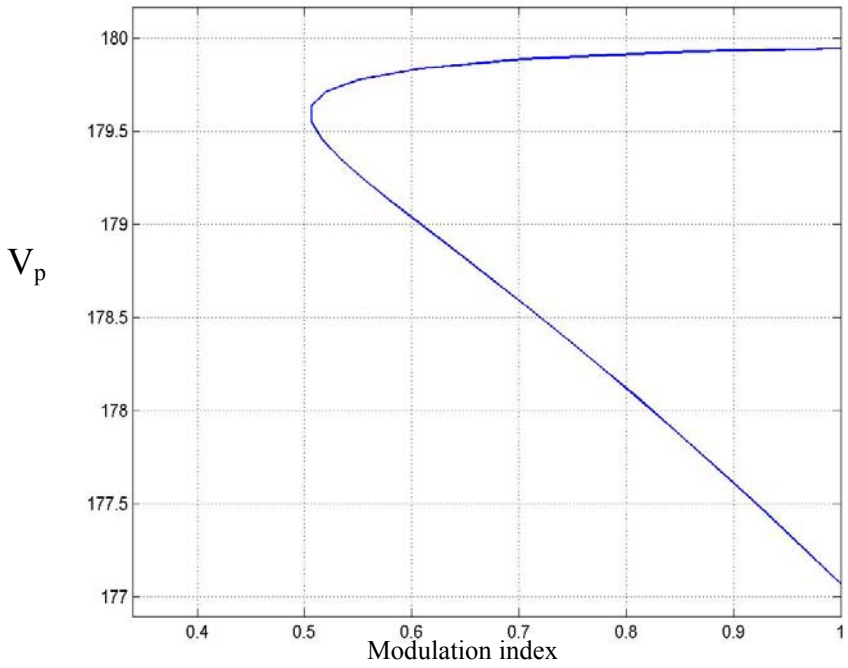


Figure 6.12 Plot of Modulation Index Versus Input Capacitor Voltage for various values of output voltage under unity power factor operation

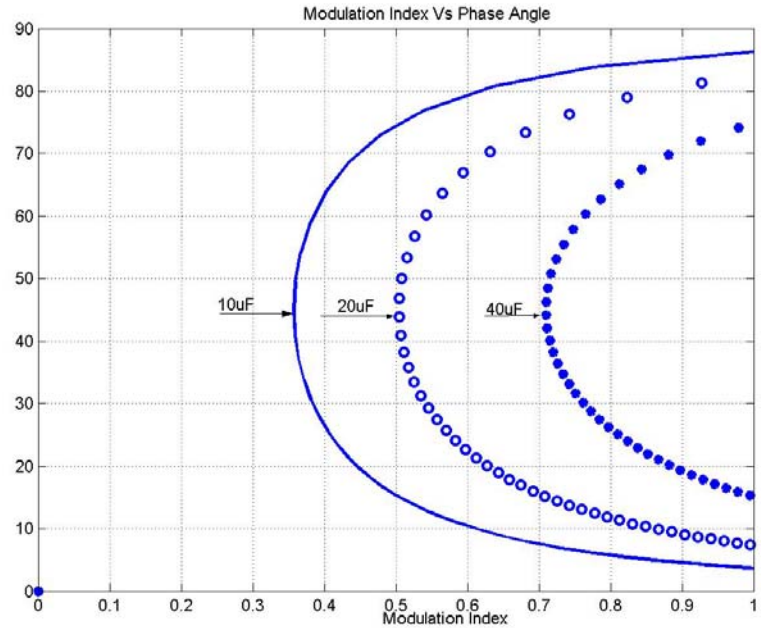


Figure 6.13 Plot of Modulation Index Versus Input displacement phase

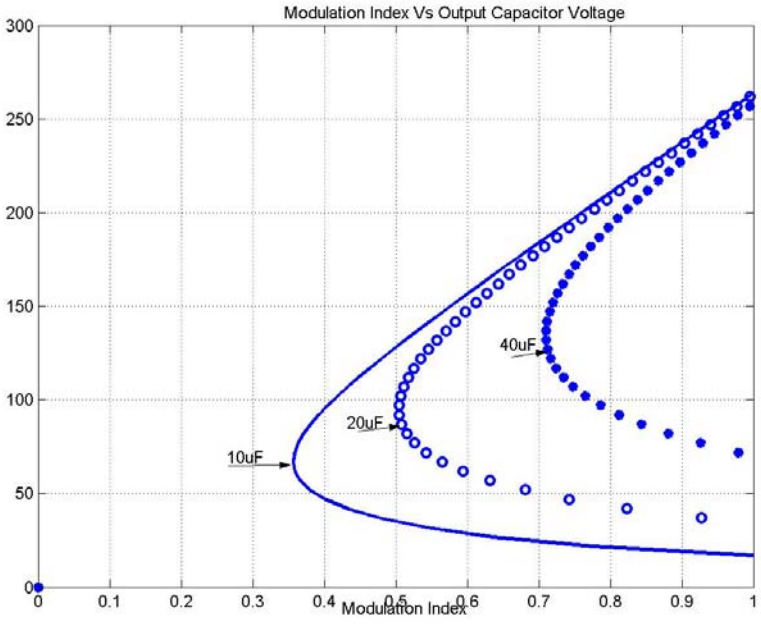


Figure 6.14 Plot of Modulation Index Versus Output Capacitor Voltage

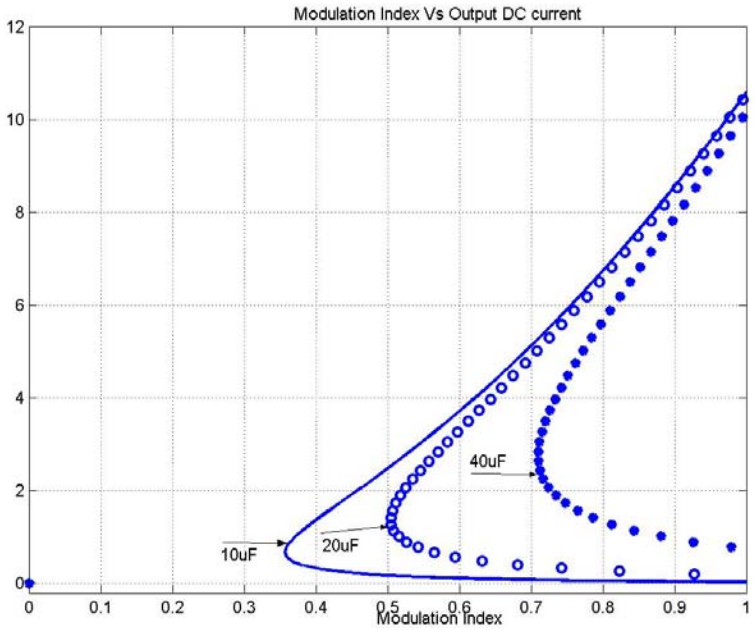


Figure 6.15 Plot of Modulation Index Versus Output DC

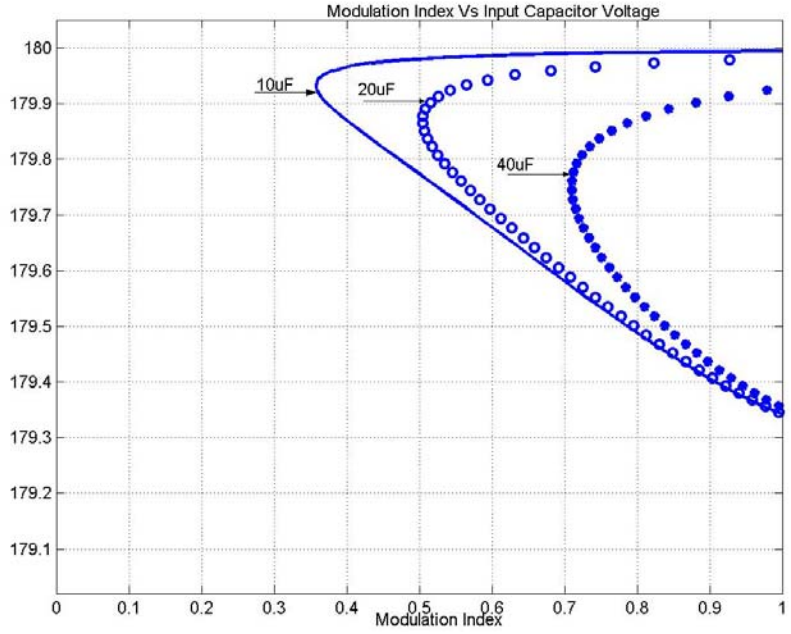


Figure 6.16 Plot of Modulation Index Versus Input Capacitor Voltage

Figures 6.12 to 6.16 gives Modulation index vs Input displacement power factor, output capacitor voltage, output DC current, and input capacitor voltages for different values of input side capacitor. From the above plots, it is observed that both the modulation index magnitude and modulation angle affect the output voltage and input current under unity power factor operation. For a wide operating condition, the input voltage to the converter, i.e., the input shunt capacitor voltage magnitude is almost constant, independent of the control. Figure 6.9 shows the plot of modulation index versus phase shift for unity power factor operation. Notice that the modulation index (M) decreases as the phase shift increases to about 45^{o}, and it increases beyond that and all the other plots also have the same characteristics: all of them decrease as the phase shift increases. For different values of modulation index there are two possible values of output voltage, input current and input capacitor voltage, while maintaining unity power factor operation.

6.9 Small Signal Analysis

To further investigate the system beyond the steady state response, small signal analysis is provided. This analysis is very useful to describe the system in a transient time. For controller design with linear control-system design techniques, the nonlinear dynamics equations cannot be directly used. They have to be linearizied around an operating point by using perturbation techniques. For small-signal inputs or disturbances, the linearizied equations are valid.

From Equations (6.3) to (6.9), which represent the rectifier in the synchronously rotating reference frame, let

$$x = X + \Delta\ x \tag{6.61}$$

$$x\ = \begin{bmatrix} i_{qs} \\ i_{ds} \\ v_{qp} \\ v_{dp} \\ i_d \\ V_o \end{bmatrix} + \begin{bmatrix} I_{qs} + \Delta i_{qs} \\ I_{ds} + \Delta i_{ds} \\ V_{qp} + \Delta v_{qp} \\ V_{dp} + \Delta v_{dp} \\ I_d + i_d \\ V_o + v_o \end{bmatrix} \tag{6.62}$$

$$\Delta x = \begin{bmatrix} \Delta i_{qs} & \Delta i_{ds} & \Delta v_{qp} & \Delta v_{dp} & \Delta i_d & \Delta v_o \end{bmatrix}^T \tag{6.63}$$

and the control inputs (M_q and M_d) perturbations given as

$m_q = M_q + \Delta\ m_q$ and $m_d = M_d + \Delta\ m_d$

By substituting Equations (6.3) to (6.9) into the space state equation of the converter given by

$$\Delta \dot{x}\ = A\ \Delta x\ + B\ \Delta u\ + E\ \Delta d \tag{6.64}$$

where

$x = \begin{bmatrix} i_{qs} & i_{ds} & v_{qp} & v_{dp} & i_d & v_o \end{bmatrix}^T$ represents state variables of the system

$u = \begin{bmatrix} M_q & M_d \end{bmatrix}^T$ represents input variables of the system

$v = \begin{bmatrix} v_{qp} & v_{dp} \end{bmatrix}^T$ represents disturbance in the system

After the perturbation of the above equation yields

$$A = \begin{bmatrix} \frac{-r_s}{L_s} & -\omega & \frac{-1}{\omega} & 0 & 0 & 0 \\ \omega & \frac{-r_s}{L_s} & 0 & \frac{-1}{L_s} & 0 & 0 \\ \frac{1}{C} & 0 & 0 & -\omega & \frac{-M_q}{C} & 0 \\ 0 & 1/C & \omega & 0 & \frac{-M_d}{C} & 0 \\ 0 & 0 & \frac{1.5M_q}{L_o} & \frac{-1.5M_d}{L_o} & 0 & \frac{-1}{L_o} \\ 0 & 0 & 0 & 0 & \frac{1}{L_o} & \frac{-1}{C_o R_o} \end{bmatrix} \tag{6.65}$$

The parameters of the designed rectifier used for this analysis are: input side line resistance r_s = 0.3Ω, input side line inductor L = 3mH, input side shunt capacitor C = 60μF, output side DC link inductor L_{dc} = 50mH, equivalent resistance of the DC inductor r_d = 0.2Ω, load resistance R_L = 25Ω, output side capacitor C_o = 100μF. The eigenvalues of the rectifier are plotted for all values of M_q and M_d at unity power factor operation with the change in the output DC voltage varying between 20V to 300V. Calculations are done for three different input side capacitor values. It is seen that there are a total of six eigenvalues for the system; Figure 6.17 shows the loci of two complex conjugate eigenvalues. There are in addition two real valued eigenvalues that lie in the left-half plane. All the poles are in the left-half plane showing that the system is stable for considered operating conditions.

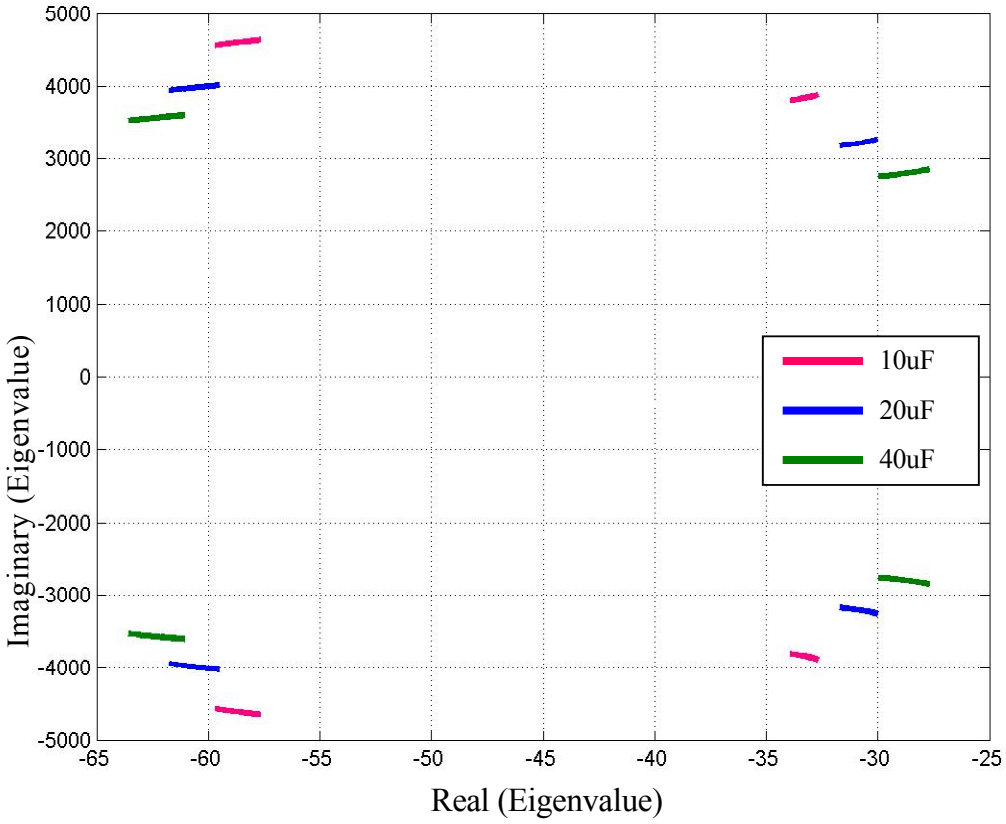


Figure 6.17 Eigenvalues for different values of input side capacitor at unity power factor operation.

6.10 Current Source Rectifier Control Structure

Three-phase PWM converters are increasingly being considered for use as front-end power processing units with power factor correction. The three-phase buck converter with six-step PWM provides DC output voltage and sinusoidal input current with no low frequency harmonics. However, the switching frequency harmonics contained in the

input currents must be suppressed by the input line filter, which produces a phase shift between the line currents and input voltages. The phase shift varies with the load and with the magnitude of the input phase voltage. The solution originally in [C.20] and more recently in [C.21] and [C.22] is to control the phase shift of the input currents in a closed loop. In that case, the filter is included in the control loop together with the converter. The full state feedback of input filter states is usually employed [C.18, C.20, C.22], and extensive digital hardware is needed for the controller implementation [C.21].

This work presents a new simple control algorithm, which provides output voltage regulation and compensation for input displacement factor without restoring to the control of the input filter states. The phase shift of the input currents is compensated through a output current loop which assures the converter in steady-state draws the desired reactive current. A fast control loop is employed for output voltage regulation.

Control of the CSR is done in q-d-o synchronous reference frame, because in synchronous reference frame all the time varying quantities become time invariant quantities. Controlling these time invariant quantities can be much easily achieved by using PI, PD, or PID controllers. Hence, all the time varying quantities are transformed into time invariant quantities using the synchronous frame transformation. And the control scheme adopted is a cascade control [A.2]; i.e., the output of the one controller is used to calculate the reference for the other controllers. Hence the time response of the controllers becomes a main criterion in designing the control parameters.

The main objectives of the control of the current source rectifier are:

- To attain unity power factor at the source side.

- To regulate the output DC voltage.

Writing the model equations for the CSR in complex q-d-o synchronous reference frame, equations in complex form are as

$$V_{qds} = L_S pI_{qds} + r_s I_{qds} - j\omega_e L_s I_{qds} + V_{qdp} \tag{6.66}$$

$$CpV_{qdp} - j\omega_e C_s V_{qdp} = I_{qds} - M_{qds} I_d \tag{6.67}$$

$$L_d pI_d + r_d I_d = \mathrm{Re}al\left[\frac{3}{2}\left[V_{qdc} M_{qds}{}^{*}\right]\right] - V_{dc} \tag{6.68}$$

$$C_d pV_{dc} = I_d - I_o . \tag{6.69}$$

The above four equations are the model equations for the rectifier in complex form. complex form of the equations is used to decouple equations in order to attain values of M_q and M_d.

Differentiating Equation (6.37) and multiplying by C

$$CpV_{qds} = CL_s p^2 I_{qds} + r_s CpI_{qds} - j\omega_e L_e pI_{qds} + CpV_{qdp} \ . \tag{6.70}$$

Using Equation (6.66) substituting C_pV_{qdp} in the above equation

$$CpV_{qds} = CL_s p^2 I_{qds} + r_s CpI_{qds} - j\omega_e L_e pI_{qds} + I_{qds} - M_{qds} I_d + jw_e CV_{qdp} . \tag{6.71}$$

Arranging the above equation

$$CpV_{qds} = I_{qds}(CL_s p^2 + r_s Cp - j\omega_e L_s Cp) + I_{qds} - M_{qds} I_d + jw_e CV_{qdp} . \tag{6.72}$$

Let

$$\sigma_{I_{qds}} = I_{qds}(CL_s p^2 + r_s Cp - j\omega_e L_s Cp) . \tag{6.73}$$

Then above equation becomes

$$M_{qds} = \left[\sigma_{I_{qds}} + j\omega_e CV_{qds} + I_{qds} - CpV_{qds}\right]\frac{1}{I_d} . \tag{6.74}$$

From (6.38)

$$I_d = C_d pV_{dc} + I_o . \tag{6.75}$$

Substituting the above equation in Equation (6.68)

$$(L_d p + r_d)(C_d pV_{dc} + I_o) = \mathrm{Re}al\left[\frac{3}{2}\left[V_{qdc} M_{qds}{}'\right]\right] - V_{dc} . \tag{6.76}$$

Arranging terms in the above equation

$$(L_d C_d p^2 + r_d C_d p)V_{dc} + V_{dc} = \mathrm{Re}al\left[\frac{3}{2}\left[V_{qdc} M_{qds}{}'\right]\right] - (L_{dp} + r_d)I_o . \tag{6.77}$$

Let

$$\sigma_{Vd} = V_{dc}(L_d C_d p^2 + r_d C_d p) \ . \tag{6.78}$$

Equation (6.77) can be given as

$$\sigma_{Vd} = \frac{3}{2}\mathrm{Re}al\left[V_{qdc} M_{qds}{}'\right] - (L_d p + r_d)I_o - V_{dc} . \tag{6.79}$$

it can be said that

$$\frac{3}{2}\mathrm{Re}al\left[V_{qdc} M_{qds}{}'\right] = \frac{3}{2}\mathrm{Re}al\left[V_{qdc}{}' M_{qds}\right]. \tag{6.80}$$

Using the above condition and using the Equation (6.77) can be written as

$$\frac{3}{2}\mathrm{Re}al\left[\left[-CpV_{qds}{}' + \sigma_{qds} + jw_e CV_{qdc} + I_{qds}\right]\frac{1}{I_d}V_{qdc}{}'\right] . \tag{6.81}$$

it is known that in synchronous reference frame of transformation.

Imaginary part of the V_{qds} is zero;

i.e. $jw_e V_{qds} = 0$.

Equation (6.81) can be given as

$$\frac{3}{2I_d}\mathrm{Re}al\left[\sigma_{qds} V_{qdc}{}' + I_{qds} V_{qdc}{}'\right] - I_o\left[r_d + L_{dp}\right] - V_{dc} . \tag{6.82}$$

From Equation (6.80)

$$\mathrm{Re}\,al\left[\sigma_{qds}V_{qdc}'+I_{qds}V_{qdc}'\right]=\frac{2I_d}{3}\sigma_{Vd}+\frac{2I_d}{3}I_o(r_d+L_{dp})+\frac{2I_d}{3}V_{dc}. \tag{6.83}$$

Simplifying the above equation

$$\mathrm{Re}\,al\left[\sigma_{qds}V_{qdc}'+I_{qds}V_{qdc}'\right]=\frac{2I_d}{3}\left[\sigma_{Vd}+I_o(r_d+L_{dp})+V_{dc}\right]. \tag{6.84}$$

By separating the real and imaginary parts in the above equations and equating the real part to the RHS, above equation is given as

$$I_{qs}V_{qc}+I_{ds}V_{dc}+\sigma I_{qs}V_{qc}+\sigma I_{ds}V_{dc}=\frac{2I_d}{3}\left[\sigma_{Vd}+I_o(r_d+L_{dp})+V_{dc}\right]. \tag{6.85}$$

Arranging the terms in the above equation using the I_{ds}=0 for unity power factor operation we have the commanded I_{qs} current as

$$I_{qs}^{*}=\frac{\frac{2I_d}{3}\left[\sigma_{Vd}+I_o(r_d+L_d p)+V_{dc}\right]-V_{dc}(I_{ds}+\sigma I_{ds})-\sigma I_{qs}V_{qc}}{V_{qc}}. \tag{6.86}$$

From Equation (6.74)

$$M_{qds}=\left[\sigma_{I_{qds}}+jw_eCV_{qdc}+I_{qds}-CpV_{qds}\right]\frac{1}{I_d}. \tag{6.87}$$

Separating the above complex and equating the real and imaginary parts on the both sides

$$M_q+jM_d=\left[\sigma_{I_q}+j\sigma_{I_d}+j\omega_eC(V_q+jV_d)+I_{qs}+jI_{ds}\right]\frac{1}{I_d} \tag{6.88}$$

$$M_q=\left[\sigma I_{qs}-\omega_eCV_{dc}+I_{qs}\right]\frac{1}{I_d} \tag{6.89}$$

$$M_d=\left[\sigma I_{ds}+\omega_eCV_{qc}+I_{ds}\right]\frac{1}{I_d}. \tag{6.90}$$

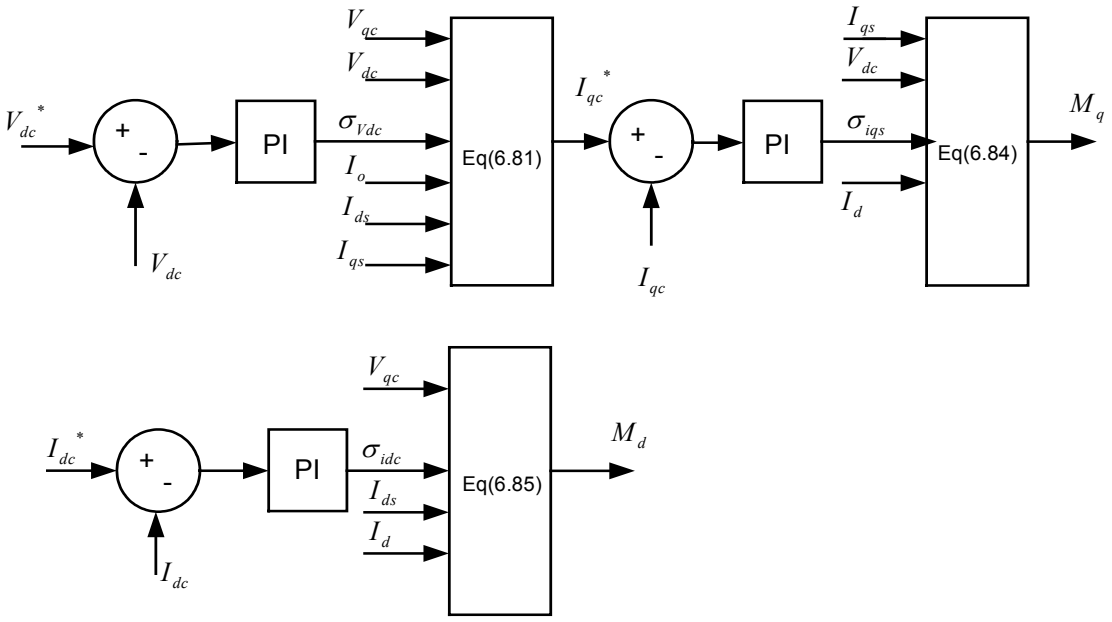


Figure 6.18 Control Structure for Current Source Rectifier.

The above figure shows the control structure of the rectifier in which the commanded DC voltage is compared with the actual DC voltage and the error signals from this comparison is passed through a PI voltage controller. The output of this controller is passed through Equation (6.58) to attain the commanded q axis current. The obtained commanded current is compared with the actual q axis current, and the error signal is passes through the PI current controller. The output of the controller is used in Equation (6.60) to calculate commanded M_q.

The commanded d-axis currents compared with the actual d axis current and the error from this comparison is passed through a PI controller. The output of the controller is used in Equation (6.66) to calculate M_d. From Equations (6.53) can be expressed as M_q and M_d in terms of transformed switching functions

$$M_q = 2S_{qp} \quad \text{and} \quad M_d = 2S_{dp}. \tag{6.91}$$

Hence, from Equation (6.91)

$S_{qp} = \frac{M_q}{2}$, $S_{dp} = \frac{M_d}{2}$ and using the condition (6.50) and transforming S_{qp}, S_{dp}, S_{qn}, S_{dn} into a-b-c reference frame using the inverter transformation matrix S_{ap}, S_{bp}, S_{cp}, S_{an}, S_{bn}, and S_{cn} can be obtained . These switching functions can be expressed into sum of a fundamental component and dc-term form section 3.9. Hence the fundamental component can be taken as the expression for modulating signals to generate commanded currents.

6.10.1 Voltage Controller Design

From the above Equation (6.78)

$$\sigma_{Vd} = V_{dc}(L_d C_d p^2 + r_d C_d p) \tag{6.92}$$

where σ_{Vd} is the output of the DC Voltage controller

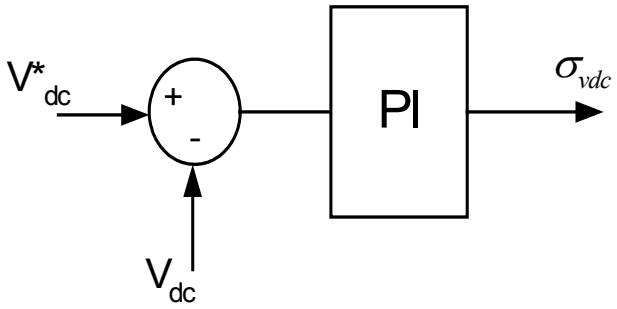


Figure 6.19 Voltage controller

From Figure 6.14, we can write the output of the controller as

$\sigma_{Vd} = K_{vdc}(V^*_{dc} - V_{dc})$.

Substituting Equation (6.67)

$$V_{dc}(L_d C_d p^2 + r_d C_d p) = K_{vdc}(V_{dc}^* - V_{dc}). \tag{6.93}$$

where K_{vdc} is the controller gain, V_{dc}^* is the commanded DC voltage, and V_{dc} is the actual voltage at the capacitor.

The transfer function from the above equation can be given as

$$\frac{V_{dc}}{V_{dc}^*} = \frac{K_{vdc}}{L_d C_d p^2 + r_d C_d p + Kvdc}. \tag{6.94}$$

Let the controller be a PI controller so that controller constant can be given as

$$K_{vdc} = K_{pvdc} + \frac{K_{Ivdc}}{s} \tag{6.95}$$

where K_{pvdc} is the proportional constant and the K_{ivdc} is the integral constant

By substituting the above equation in the transfer function

$$\frac{V_{dc}}{V_{dc}^*} = \frac{(K_{pvdc} + \frac{K_{Ivdc}}{S})\frac{1}{L_d C_d}}{S^3 + \frac{rd}{Ld}S^2 + \frac{K_{pvdc}}{L_d C_d}S + \frac{K_{Ivdc}}{L_d C_d}}. \tag{6.96}$$

Comparing the denominator with the butterworth third order polynomial;

i.e. $P^3 + 2P^2\omega_o + 2P{\omega_o}^2 + {\omega_o}^3 = 0$. (6.97)

From the comparison

$$2W_o^2 = \frac{K_{pvdc}}{L_d C_d} \qquad K_{pvdc} = 2{\omega_o}^2 L_d C_d \tag{6.98}$$

$$W_o^3 = \frac{K_{Ivdc}}{L_d C_d} \qquad K_{Ivdc} = {\omega_o}^3 L_d C_d. \tag{6.99}$$

After having the expressions for the K_{pvdc} and k_{ivdc} ,for different values of W_o ,controller is tuned to track the commanded voltages.

6.10.2 Current Controller Design

From the Equation (6.73)

$$\sigma_{I_{qds}} = I_{qds}(CLp^2 + r_s Cp - j\omega_e LCp) \tag{6.100}$$

where $\sigma_{I_{qds}}$ is the output of the current controllers

From the above Figure (6.19) the output of the controller can be given as

$I_{qs} = K_{Iqs}(I^*_{qs} - I_{qs})$. Substituting in Equation (6.100)

$$I_{qds}(CLp^2 + r_s Cp - j\omega_e LCp) = k_{Iqds}(I_{qds}^* - I_{qds}) . \tag{6.101}$$

By writing the above complex current in real and imaginary and equating

$$I_{qs}(CLp^2 + r_s C_p - j\omega_e LCp) = k_{Iqs}(I_{qs}^* - I_{qs}) \tag{6.102}$$

$$I_{ds}(CLp^2 + r_s Cp - j\omega_e LCp) = k_{Ids}(I_{ds}^* - I_{ds}) . \tag{6.103}$$

Writing the transfer function for the I_{qs} current controller

$$\frac{I_{qs}}{I_{qs}^*} = \frac{(SK_{PIqs} + K_{Iqs})\frac{1}{LC}}{S^3 + \frac{r_s C - j\omega_e LC}{CL}S^2 + \frac{K_{pIqs}}{LC}S + \frac{K_{Iqs}}{LC}} . \tag{6.104}$$

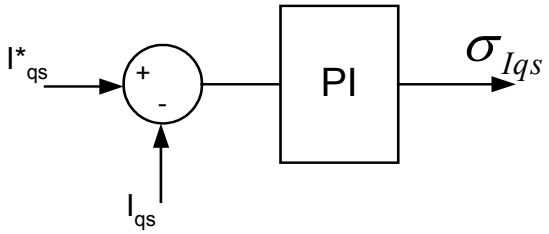


Figure 6.20 Structure of Current controllers

Comparing the denominator with the butterworth third polynomial

$$K_{pIqs} = 2\omega_o{}^2 LC \tag{6.105}$$

$$K_{I_{Iqs}} = \omega_o{}^3 LC\ . \tag{6.106}$$

Same procedure is followed for the d axis current controller and the transfer function for this controller can be written as

$$\frac{I_{ds}}{I_{ds}{}^*} = \frac{(SK_{PIds} + K_{Ids})\frac{1}{LC}}{S^3 + \frac{r_s C - j\omega_e LC}{CL}S^2 + \frac{K_{pIds}}{LC}S + \frac{K_{Ids}}{LC}}\ . \tag{6.107}$$

Comparing the denominator with the butterworth third polynomial

$$K_{pIds} = 2\omega_o{}^2 LC \tag{6.108}$$

$$K_{I_{Ids}} = \omega_o{}^3 LC\ . \tag{6.109}$$

6.11 Closed Loop Simulation Results

Using the control structure explained in section 6.10 a CSR is simulated using the modulation scheme proposed in Chapter 4 for continuous modulating signals. In the control scheme the DC voltage was commanded to a value of 170 V and at a time of 0.25 sec the commanded voltage was changed to 180 V. And the d-axis current is commanded to zero, in order to attain unity power factor at the source end. The simulation is done using the filter parameters designed in the section 6.6 with L_i = 3mH, C = 60μF, r_i = 0.01Ω, L_d = 40mH, r_d = 0.5Ω, R_L = 25Ω with a switching frequency of 5KHz. The

controller parameters are calculated using the equations derived in the above sections of voltage and current controller.

6.11.1 Simulation Results for Change in the DC Command Voltage

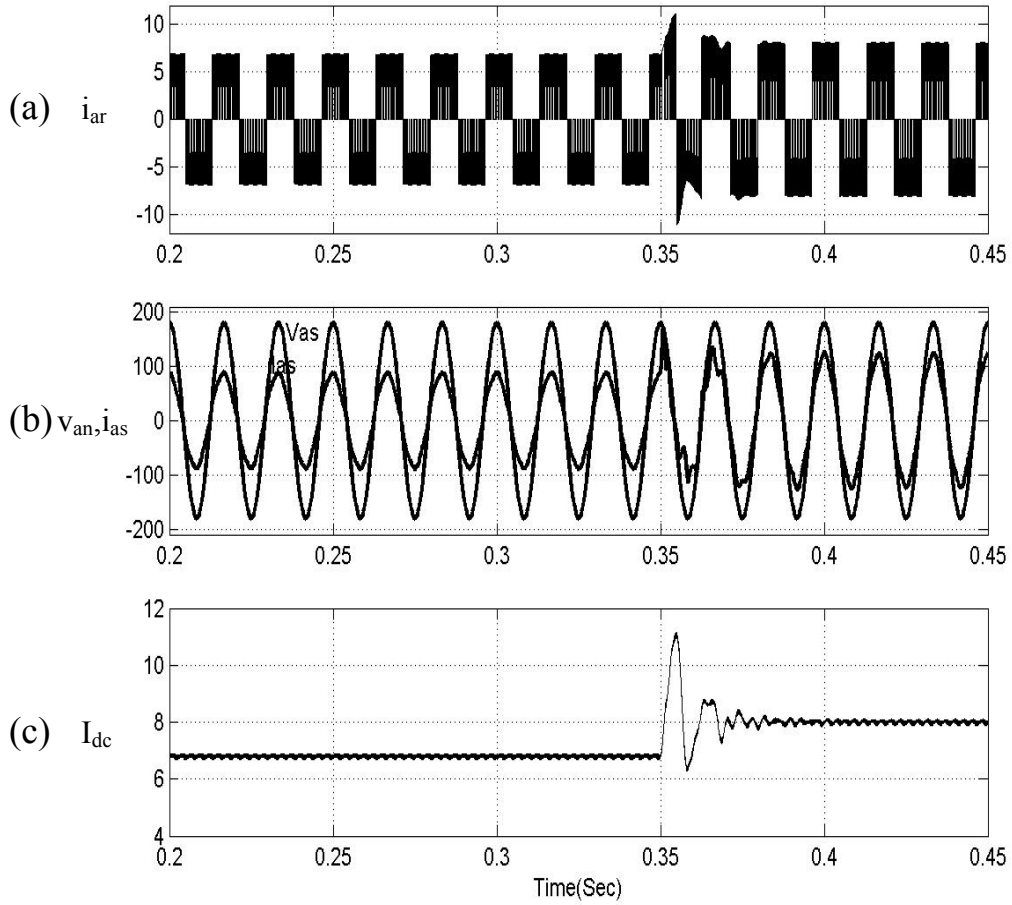


Figure 6.21 Closed loop simulation results for control of three phase CSR for a change in the commanded dc from 170V to 200V at time t = 0.35 sec with $R_L = 25\Omega$. (a) phase 'a' input current to the rectifier (b) phase 'a' line voltage and line current (c) output DC current.

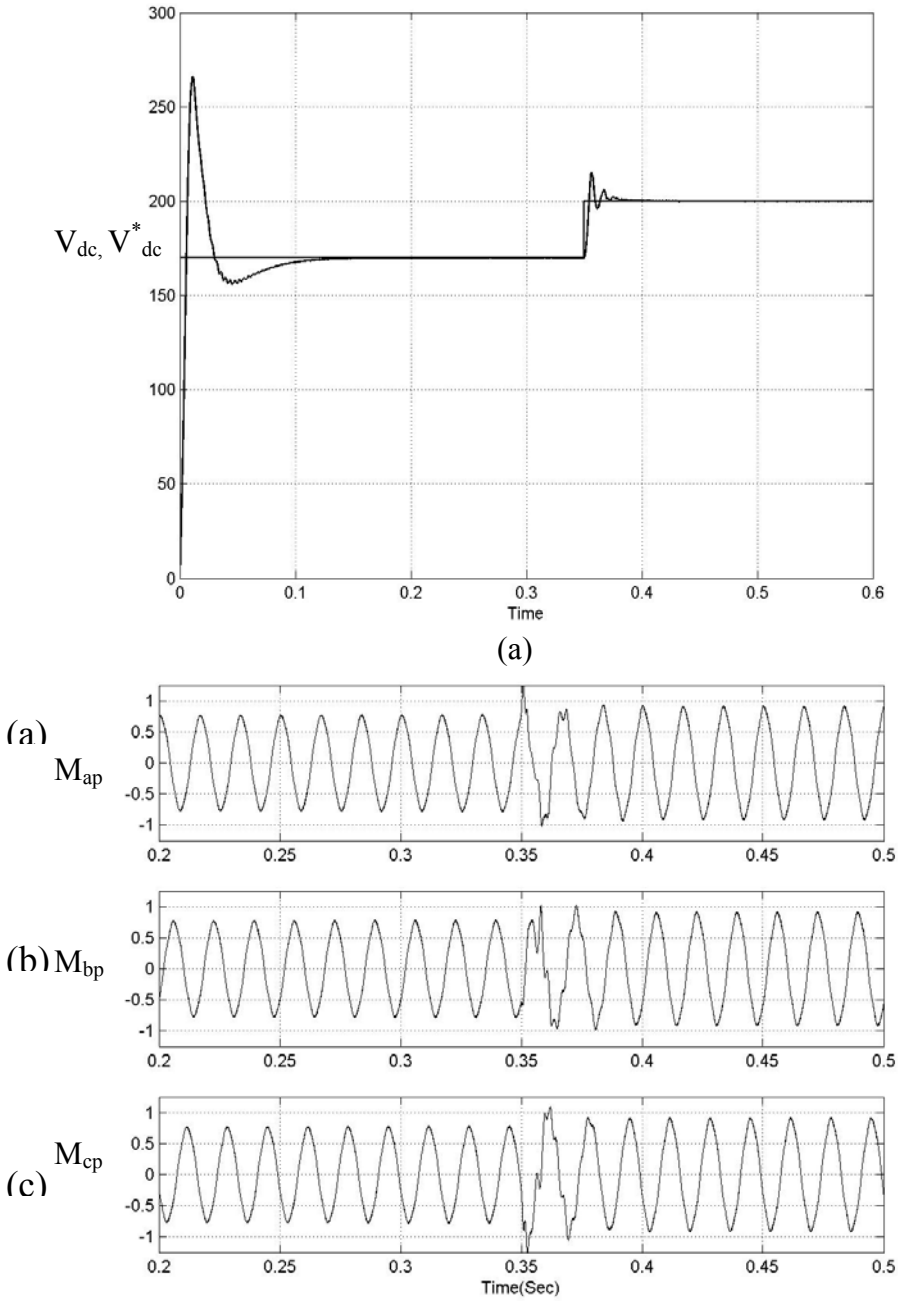


Figure 6.22 Closed loop simulation results for control of three phase CSR for a change in the commanded dc from 170V to 200V at time t = 0 .35 sec with $R_L = 25\Omega$. (a) commanded voltage and actual voltage (b) Three phase modulating signals.

6.11.2 Simulation Results for the Change in Load

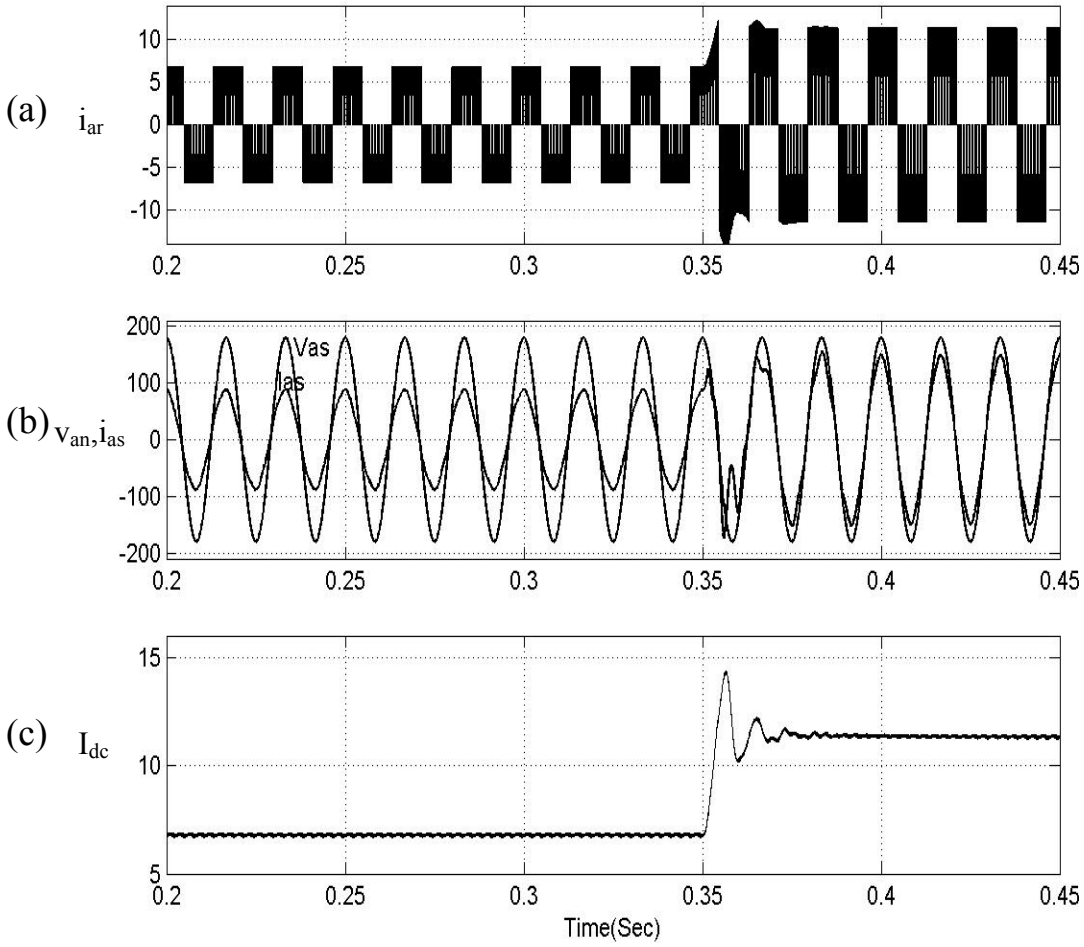
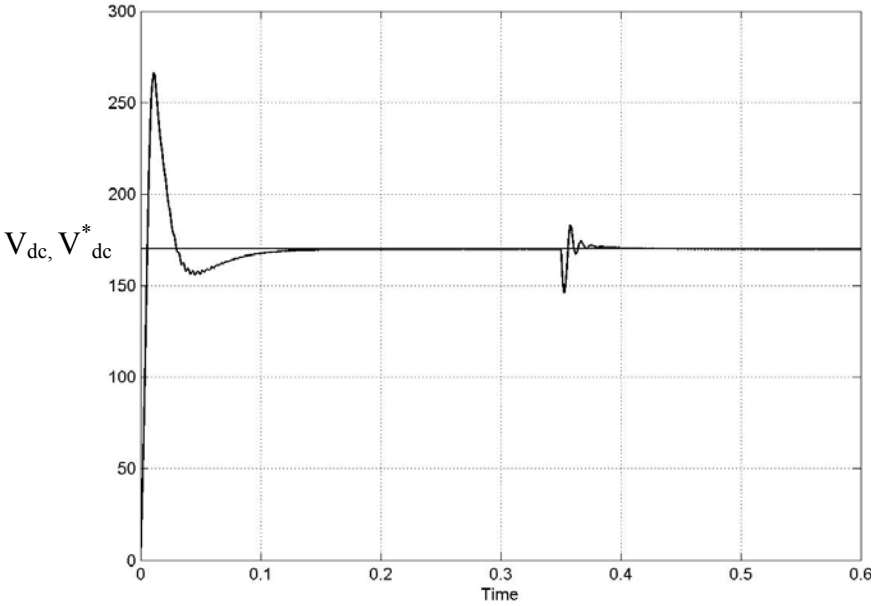
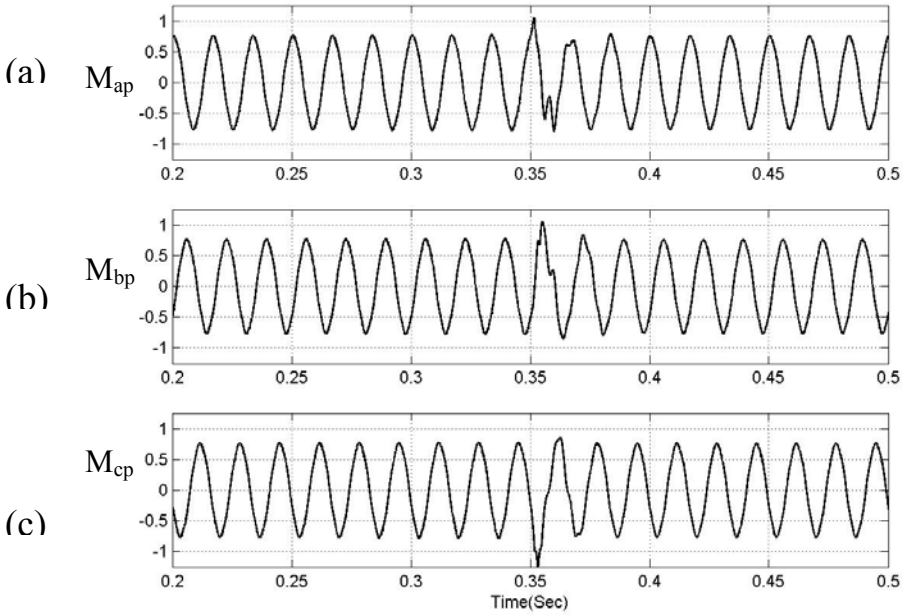


Figure 6.23 Closed loop simulation results for control of three phase CSR for a change in the load from 25Ω to 15Ω at time t = 0.35 sec with V_{dc} = 170V. (a) phase 'a' input current to the rectifier (b) phase 'a' line voltage and line current (c) output DC current.



(a)



(b)

Figure 6.24 Closed loop simulation results for control of three phase CSR for a change in the load from 25Ω to 15Ω at time t = 0.35 sec with V_{dc} = 170V.(a) commanded DC voltage and actual DC voltage (b) Three phase modulating signals.

6.12 Discussions about the Closed Loop Simulation Results

The above Figures 6.21 to 6.22 show the simulation results of the closed loop control of the three-phase rectifier for a change in the DC voltage at a constant load. Initially, the DC Voltage was commanded at 170 V after a time t = 0.25sec the commanded DC voltage was changed to 180 V. Figure 6.21(a) shows the phase 'a' input switching current to the rectifier, it is observed the change in switching for change in the command. Figure 6.21 (b) shows the input phase 'a' voltage and line current; it is seen that the voltage and the current are in the same phase. Which shows the rectifier is operating in unity power factor operation Figure 6.21(c) shows the output DC current it can be seen that the DC current increases as the commanded DC voltage is changed. Figures 6.23 to 6.24 shows the simulation results of closed loop control of the CSR for increase in the load form 25Ω to 15Ω. At a constant DC voltage command of 170 V. Figure 6.23(a) shows the phase 'a' input switching current to the rectifier; it can be seen that the current changes as the command changes. Figure 6.23(b) shows the input phase 'a' voltage and line current, which shows unity power factor operation of the rectifier. Figure 6.23(c) shows the change in the output DC current. It is seen that the output DC current increases as the load is increased. Figure 6.24(a) Commanded DC voltage and actual DC voltage. Commanded DC voltage is kept at a constant value of 170 V and load resistance value is changed. The above plot shows the little change in the actual DC voltage. Figure 6.24(b) shows the three modulating signals for change in the load resistance.

6.13 Open Loop Experimental Results

A prototype of the current source rectifier is built in the lab using a TMS320LF2407A Floating point DSP to generate the PWM signals. And the modulation scheme formulated in Chapters 4 and 5 is used to modulate the rectifier.

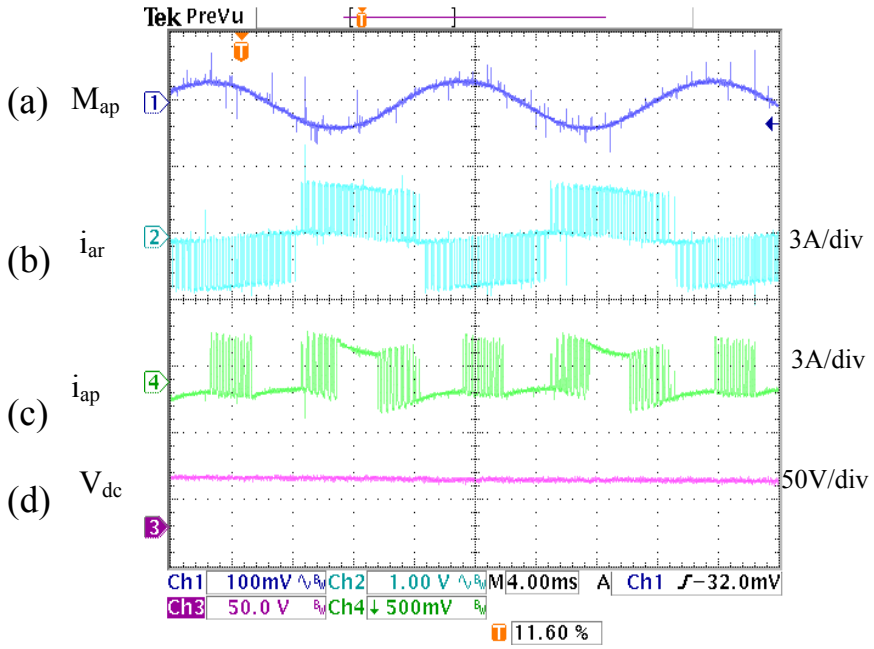


Figure 6.25 Open loop experimental results of CSR for a continuous modulating signals at M = 0.85 and f_s = 5kHz with a load R_L = 25 Ω. (a) Phase 'a' modulating signals (b) phase 'a' input current to the rectifier (c) phase 'a' one device switching (d) output DC voltage.

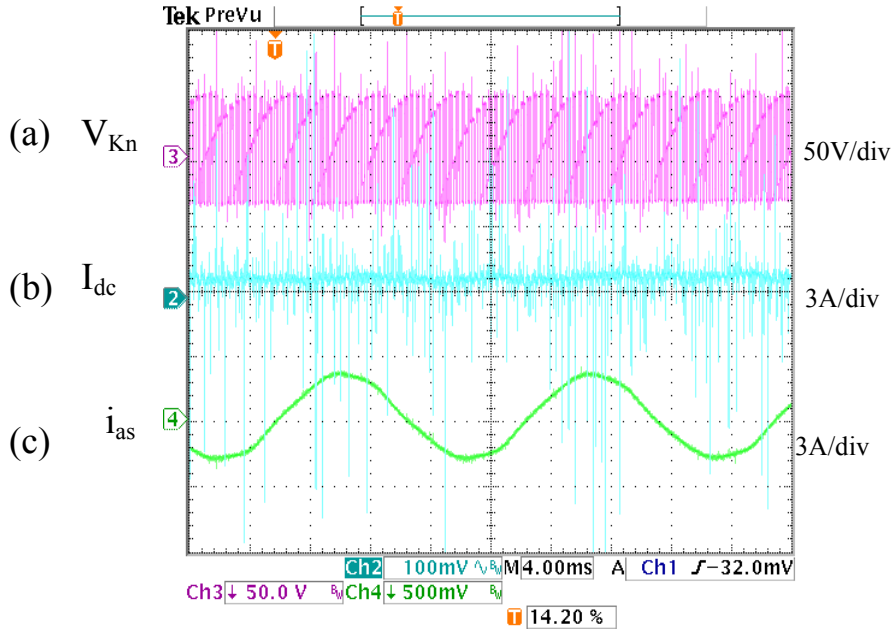


Figure 6.26 Open loop experimental results of CSR for a continuous modulating signals at M = 0.85 and f_s = 5kHz with a load R_L = 25 Ω. (a) DC-link voltage (b) output DC current (c) phase 'a' input line current.

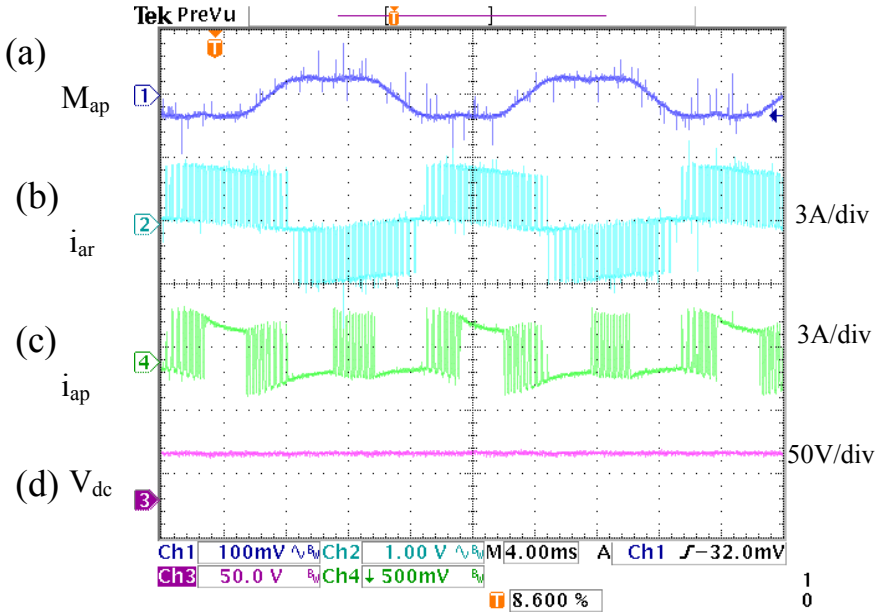


Figure 6.27 Open loop experimental results of CSR for GDPWM discontinues modulating signals for α = 0.5 at M = 0.85 and f_s = 5kHz with a load R_L = 25 Ω. (a) Phase 'a' modulating signals (b) phase 'a' input current to the rectifier (c) phase 'a' one device switching (d) output DC voltage.

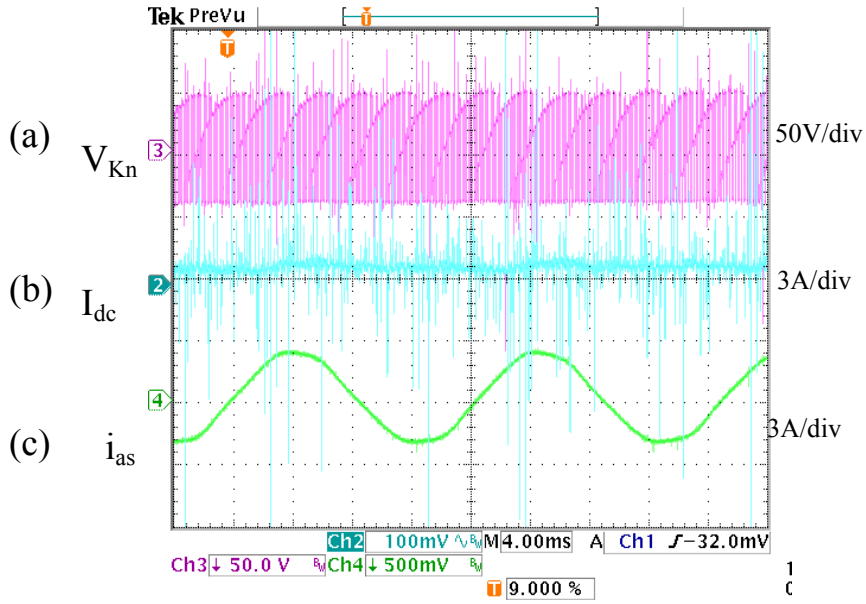


Figure 6.28 Open loop experimental results of CSR for a GDPWM discontinuous modulating signals for $\alpha = 0.5$ at $M = 0.85$ and $f_s = 5kHz$ with a load $R_L = 25\ \Omega$. (a) DC-link voltage (b) output DC current (c) phase 'a' input line current.

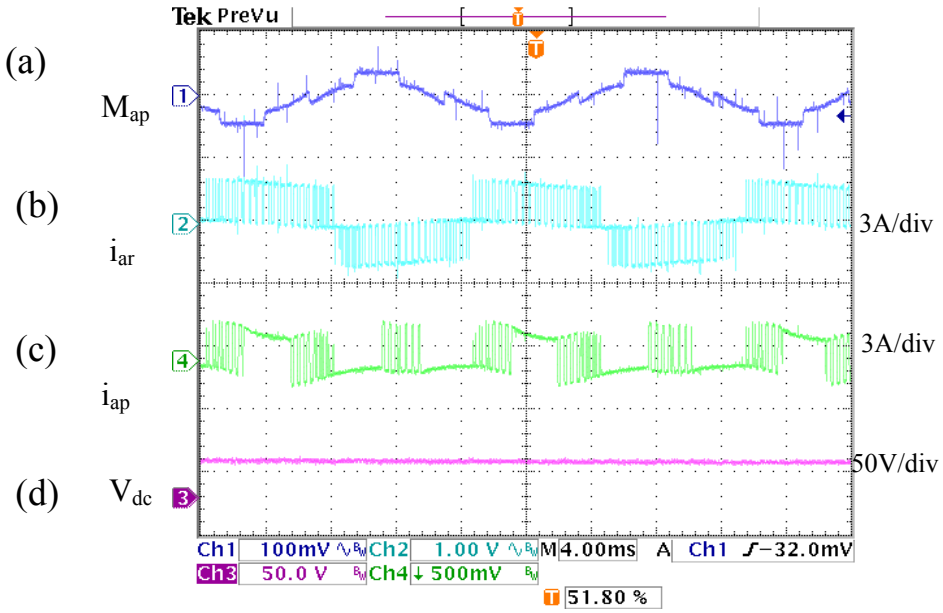


Figure 6.29 Open loop experimental results of CSR for GDPWM discontinues modulating signals for $\delta = 0$ at $M = 0.85$ and $f_s = 5kHz$ with a load $R_L = 25\ \Omega$. (a) Phase 'a' modulating signals (b) phase 'a' input current to the rectifier (c) phase 'a' one device switching (d) output DC voltage.

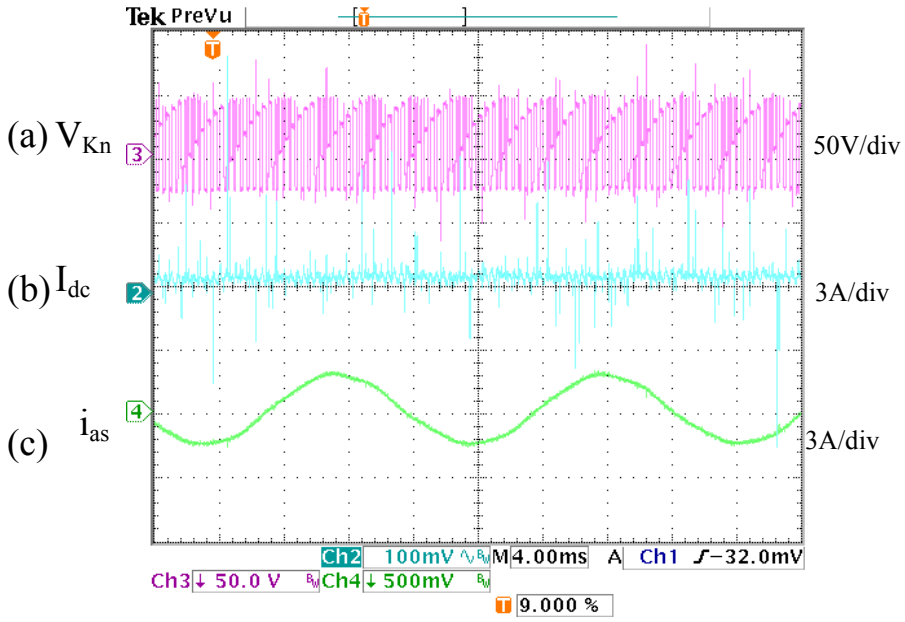


Figure 6.30 Open loop experimental results of CSR for a GDPWM discontinuous modulating signals for $\delta = 0$ at $M = 0.85$ and $f_s = 5$kHz with a load $R_L = 25\ \Omega$. (a) Dc-link voltage (b) output DC current (c) phase 'a' input line current.

Figures 6.25 to 6.30 show the open loop experimental results performed using the designed filter parameters and at a fixed modulation index of M = 0.85. And switching frequency of f_s = 5KHz. The scheme developed by mapping VSI states to CSI states is used to modulate the rectifier. Both continuous and GDPWM discontinuous modulating signals for $\alpha = 0.5$ and $\delta = 0$ are presented. From the final switching it is seen that the bottom rail is clamped for 120^0 and top rail is clamped for a period of 60^o. And it is seen that almost all the modulating signals synthesis same amount of DC voltage but there is difference in the amount of harmonics present in input line current. And also it is seen that there are some oscillations in the system because resonance in the input filter, which are caused due to the harmonics generated in the switching of the converter and also due to the harmonics present in the input side voltage. These oscillations in the system can be eliminated using better-closed loop control scheme.

CHAPTER 7

HARDWARE DESIGN

7. 1 Introduction

This section discusses some of the implementation aspects for the schemes proposed in the previous chapters. This chapter explains about the process of synthesizing six independent signals from the DSP. Explains about the requirement of the overlap time between the CSC devices, and explains the hardware circuit designed for overlap period. This also explains how the simple gates are used to implement the logic developed in the above sections. And gives the type of switches and diodes used in constructing the converter.

7.2 Usage of Event Managers to Generate Independent Signals

In implementing CSI/CSR using the GDPWM scheme mentioned in Chapter 5, a powerful TMS320LF204O7A floating point DSP with 40MHz cycle frequency is used. In this scheme it is necessary to generate six independent switching signals for six devices. So the main objective is to study these independent switching signals from the DSP. In this section it explains about the usage of the six full compare registers of the DSP to generate six switching signals.

7.2.1 Initialization of EVA and EVB

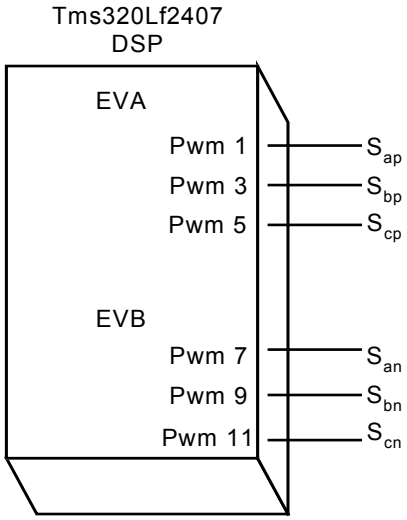


Figure 7.1 The PWM ports of the DSP

Generating six independent signals is just like driving two three-phase VSI's on a single DSP. Two Event managers EVA and EVB of the DSP are used to generate six switching pattern. Switching for the top three devices are taken from the EVA and for the bottom three-devices is taken from the EVB. All the six PWM output signals should have same PWM Time periods; i.e., the two events has to be synchronized .

The following steps are followed to attain six independent switching signals.

- All the three timers in the DSP are configured identically in continuous up/down mode with internal clock, with timers 2 and 3 set up to use the time 1 period and start bit.
- All the compare output pins are enabled, with PWM 1/3/5/7/8/9 active high and PWM 2/4/6/ T x PWM active low.

- The full compare unit is set up for shadow reload on count = 0 only. The simple compare and individual timer compares for both count = 0 and count = period.
- The hardware dead band unit is set up to zero.

The modulating signals for the top three devices M_{ap}, M_{bp}, M_{cp} are loaded in compare registers of EVA. And modulating signals for bottom M_{an}, M_{bn}, M_{cn} is loaded in compare registers of EVB. And the hardware dead time in both the events are set to zero. Since CSI does not need any dead time.

7.2.2 Synchronization of EVA and EVB

Because of using two different events for a single inverter, it has to be taken care that the time of start of the two events is same. Since the two events are two different hardware structures of the same DSP, they may have difference in initial time of starting between them. The two events have to be synchronized, so that the outputs form the two events start at the same time. Same Time period is loaded in both the events, and same modulating signal is loaded in all the compare registers of both the events. Counter of the EVA is given some initial value and the Counter of EVB is changed, until the outputs from these two events are same for the same modulating signal. In this way the synchronization between these two events is achieved.

7.3 Overlap Time in the Switching of the CSI

Dead time between the devices in a converter is one of the important aspects in higher power applications; it is the delay time between the two switches. Dead time is necessary in VSI topology because if the devices used for the converter are not fast enough to respond immediately for the switching changes from ON state to OFF state; i.e., if there is a transient time in which one device is getting ON and the other complimentary device is getting OFF, then there is possibility of shorting of the input side supply. Hence dead time is very much necessary.

But in the case of a Current source converter it is not the dead time, which is necessary in between the devices. It is the overlap period that is necessary between the top and bottom three devices. If there is any delay in the transient time between switching ON and OFF of two top devices, then there will not be any path for the input current at that time. Which may damage the devices, since there is a very big inductor at the input side of the inverter. And any open circuit in the bridge will make the inductor to release the energy stored it. So in order to take care of this backfiring of the inductor there should be some dead time in the devices for a current source converters.

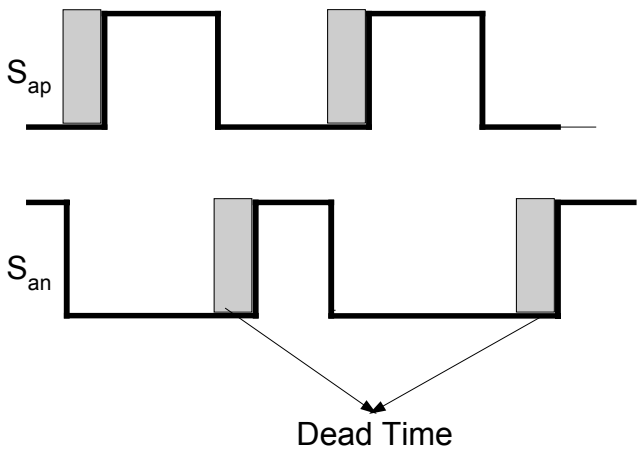


Figure 7.2 Dead time between Top and Bottom Devices of VSI

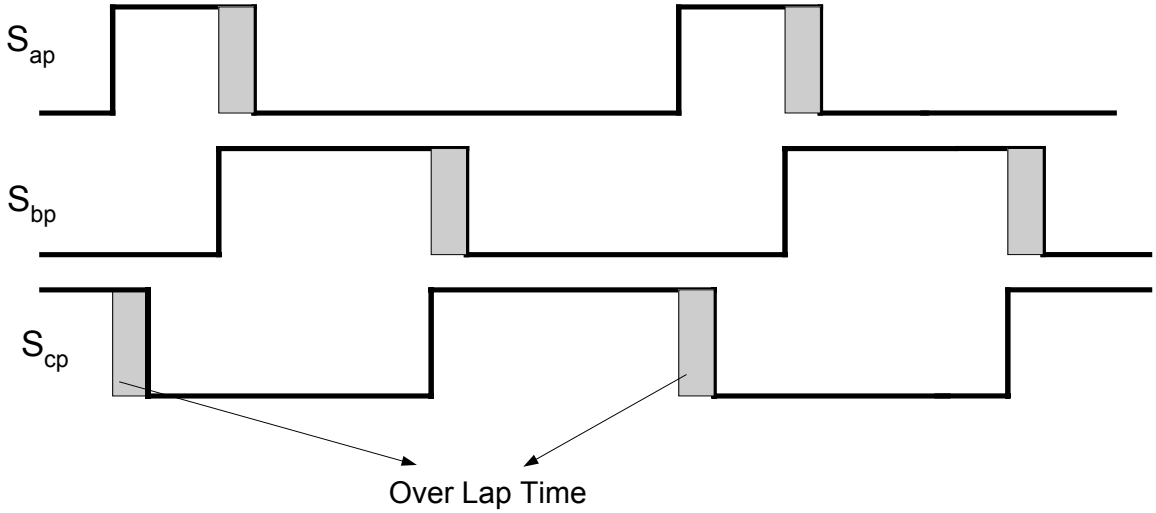


Figure 7.3 Overlap Time between Top three devices of CSC

7.3.1 Hardware Implementation of the Over Lap Time

Dead Time in case of VSI can be achieved by setting the delay registers in the DSP. But in the case of the CSI since the switching for the devices is not taken directly from the DSP, it is passed through some Hardware logic, so overlap time also has to be designed through hardware. Hence simple logic NAND gate and capacitors are used to have overlap in the switching.

Figure 7.4 shows the circuit diagram for overlap time. A NAND gate connected with capacitor and the diode is shown, and this is used to achieve overlap. The same circuit is used to attain overlap time for all the switching signals.

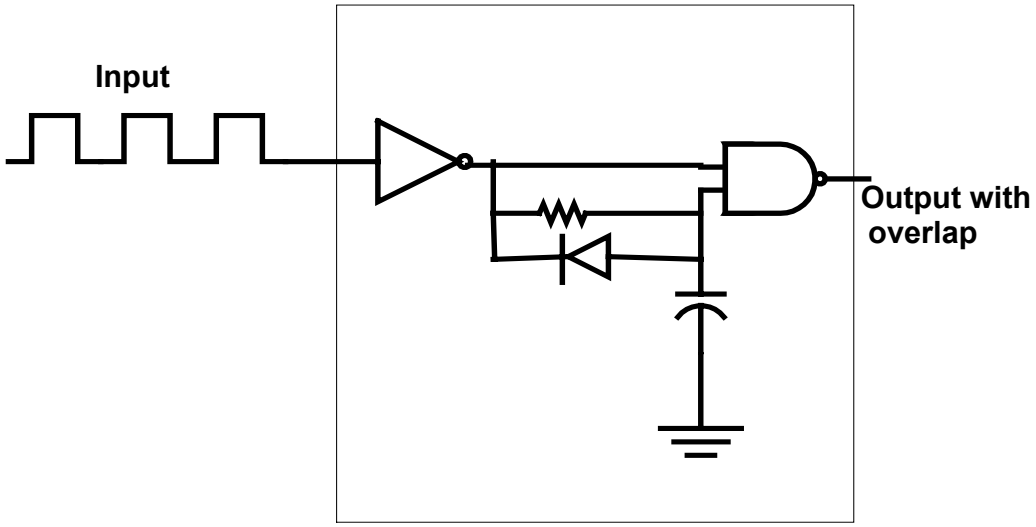


Figure 7.4 Circuit diagram for the overlap time.

7.4 Implementation of Logic Circuit Using Gates

Basic logic gates are used to implement the logic presented in Chapters 4 and 5. This logic be can be implemented using the FPGA's and EPLD's. Equations developed in 4. 6 can is implemented using the AND, OR, and NAND gates. In Equations (4.20)-(4.25) the switching has to be passed through this equation to sort the states.

Consider $h2 = S_{cn}S_{bp} + S_{an}S_{ap}$.

In this equation, let $S_{cn}S_{bp} = A$ and $S_{an}S_{ap} = B$. Now in order to implement multiplication between two signals an OR is used; i.e Output of OR of S_{cn} and S_{bp} is taken as A. Output of OR of S_{an} and S_{ap} is taken as B. And the outputs A and B are added through the AND gate .

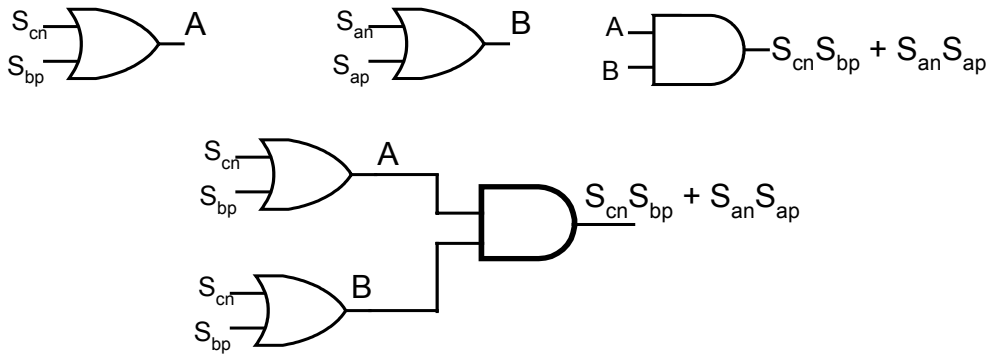


Figure 7.5 Gates used to implement the logic.

7.5 Components used in Building the Inverter

IGBT' are used to build the prototype of the converter in the lab, SKM 75 GB 0 63D is a IGBT module from Semikron. In this module two N- Channel IGBT's are connected together. Each module is similar to leg of a bridge of a two level converter. Three of these modules are used for the converter, and high frequency diodes from IRF are connected in series with the IGBT's. The rating of the IGBT's and diode are listed in Table 7.1.

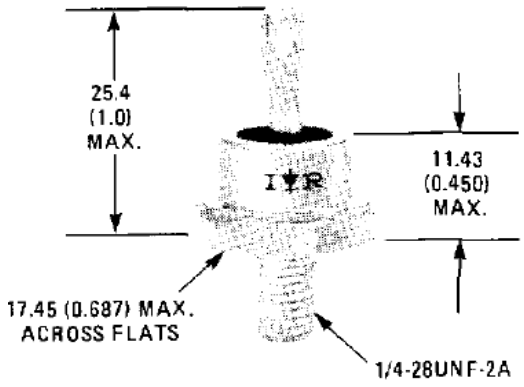


Figure 7.6 (a) IGBT Module (b) High frequency Diode.

Table 7.1 Voltage and current ratings of the IGBT and Diode.

Part Number	Voltage Rating	Current Rating
SKM 75 0 63D (IGBT's)	600V	50A
IRD 3909 (Diodes)	450V	20A

CHAPTER 8

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

This thesis has made an extensive study on the modulation strategies for a current source converter and developed a unified theory of continuous and discontinuous carrier–based pulse width methodology. The performance of these modulation strategies, their limitations, and advantages were studied in linear and over modulation regions. This chapter is a summary of the contributions of this thesis and some conclusions that can be drawn form the work are also presented. In the final section, ideas for extending the results of this thesis are presented.

8.1 Modeling and Operation of the CSI

The basic principle of operation of a three-phase current source inverter was studied. Also the constraints involved while switching a CSI, in order to satisfy the Kirchhoffs voltage and the current laws, have been studied. The mathematical model of the CSI has been formulated. Expressions for the modulating signals are derived using the objective of attaining maximum gain from the converter.

8.2 PWM Schemes in CSI using VSI Modulation Strategy

A scheme for mapping states of a voltage source inverter to current source inverter has been presented. This mapping technique was developed in both the carrier based PWM and also in space vector PWM method.

In carrier-based technique, an already developed continuous and discontinuous modulation scheme for VSI has been used .The advantages of reduced switching loss, voltage linearity, and over modulation performance of this modulation strategy was extended to CSI. Various modulating schemes of VSI mapped to CSI were studied. It has been shown that the benefits of the discontinuous schemes can be drawn through CSI to generate high quality waveforms and reduce switching losses. Illustrative experimental results are deployed to demonstrate the simplicity and efficiency of the novel modulation methodology.

A space vector approach of mapping direct VSI states to CSI states has been discussed. In this approach, a method of mapping eight states of a VSI to nine states of CSI has been developed. A novel strategy of placing the null states in between the active states to have minimum amount of switching is presented.

8.3 A New Generalized Discontinuous PWM Strategy for CSI

In this section, a new generalized Discontinuous PWM strategy for CSI has been developed. This scheme is a direct approach for developing a modulation strategy for the

CSI. Modulation of the CSI using both the carrier based and space vector approach has been presented.

Expressions for modulating signals required to synthesize balanced three-phase reference currents were derived in both the continuous and discontinuous schemes. For different values of introduced weighting factors α, β, γ different sets of modulating signals are obtained. The performance of all the possible modulators was studied, and a new algorithm was developed in order to satisfy constrains laid out for a CSI. This algorithm automatically removes the shorting of the devices and also sorts the null states to attain minimum switching. Illustrative experimental results are deployed to demonstrate the simplicity and efficiency of the novel modulation methodology in both linear and over modulation region.

In direct digital implementation method (SVM), all the expressions for times to synthesize three phase reference currents were derived very clearly. Also a method of proper arrangement of the null and active states was explained which gave minimum amount of switching. This method aids in reduction of switching losses. Operation of the scheme in over modulation region was also explained. But the experimental results to validate the proposed digital implementation was not provided because to some hardware limitations of the DSP.

8.4 Current Source Rectifier Control Scheme

The developed modulation schemes become the platform for the implementation and designing a control structure for the unity power factor operation and DC voltage

regulation of a current source rectifier. A mathematical model of the CSR was presented and with the aid of synchronous reference frame transformation, the defining equations of the rectifier–load system are made linear but coupled between q and d axes. A new approach of using complex form of the transformed equations was developed to design the controller for the CSR. All the control equations were clearly laid out and a method of designing of PI parameters using features of the Butterworth polynomials was explained. Steady state analysis of the CSR for unity power factor was performed and effects of different parameter on the performance of the controller were studied. Simulation results for the dynamic and steady state regulation of the DC voltage under unity power factor operation was performed. Commanded DC voltage was changed keeping the load constant. In this operation it was seen that the actual voltage tracks the commanded DC voltage. This shows the effectiveness of the controller. Some open loop experimental results were given to validate the modulation scheme. In the end it can be concluded that the thesis presented some new PWM strategies for the CSI, and a new method of controller design was proposed.

8.5 Suggestions for Future Work

In this final section the results and conclusions of this work are applied to ideas for future research. The experimental results reported in the above sections matched quite well except for some harmonics in the current waveform. Research is needed to improving the quality of the waveform generation. One such approach of improving the quality of waveform would be using multilevel current source inverters.

Work has to be done on using the proposed modulation methods to apply for the multilevel current source converters. The approach followed in Chapter 4 for modulating a two level three-phase current source inverter using the VSI modulation strategy can be followed in modulating a three phase three level CSI using the modulation scheme of a three-phase three level VSI. Work has to be done in developing mapping technique for multilevel CSI in both carrier-based and space vector approach.

The scheme developed for direct modulation for the CSI can be extended for a multilevel CSI. Work has to be done to develop both the direct carrier based and space vector technique for the multilevel CSI. The implementation of the logic for removing the short has been done using the logic gates. But the quality of the waveform can still be improved by using EPLD or FPGA boards for logic implementation. In general the space vector implementation of the converter is done using the soft wear determined switching patter, which are determined in DSP. Soft wear implementation through DSP requires a symmetric switching scheme; i.e. the switching timings of the devices should be symmetrically distributed. From Figure 5.8 and it can be seen that there is no symmetry in the switching times for a CSI, which makes it difficult to implement using a DSP because of the hardware limitations, which can be overcome by use of EPLD's or FPGA boards.

Due to the presence of the LC filter at the input side of the CSR lot of oscillation are found in the system. Because of the resonating of the filter due to the harmonics generated, with the switching of the rectifier and also due to the harmonics present in the supply voltage. Work has to be done to control these oscillations without affecting the system efficiency and to obtain stability in the system

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