CHAPTER 4

PWM SCHEMES IN THREE PHASE VOLTAGE SOURCE INVERTERS APPLIED TO CURRENT SOURCE INVERTERS

4.1 Introduction

Due to the inability of VSI to regenerate the incoming AC supply in absence of complex rectifying converter, there are large d_v/d_t transitions on the phase leg output voltages. This results in conspicuous problems as increased motor losses, acoustic noise in load, insulation degradation due to voltage surges and electromagnetic interference effects (EMI).

Three-phase Current Source Inverter as in figure 4.1 (CSI) has distinct advantage over Voltage Source Inverter (VSI) drives primarily due to following reasons:

1. The drive is current sensitive. Torque is directly related to stator current and rather nonlinearly with stator voltage.

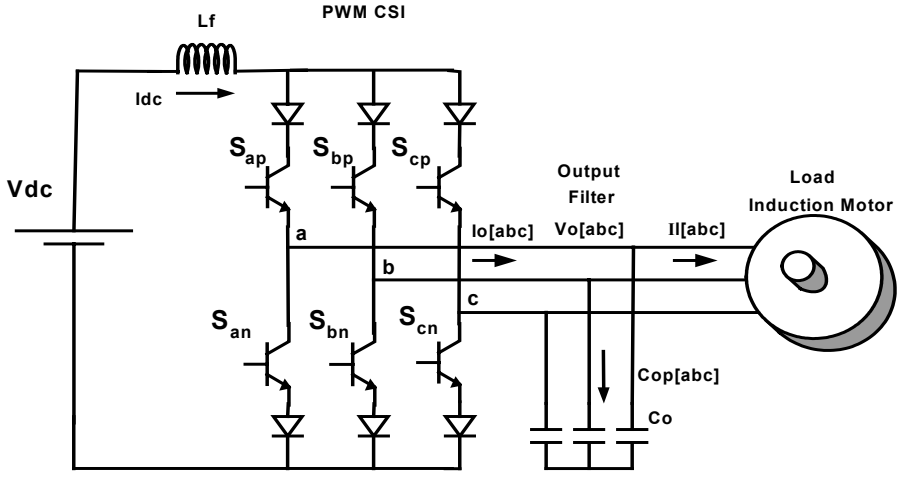


Figure 4.1 Topology of a current source inverter in motor drive application

2. The drive is regenerative. Hence the control of current ensures the direct and precise control of the electromagnetic torque. Pulse width modulation (PWM) current source inverter (CSI) fed ac motor drives are often used in high power (1,000–10 000 hp) applications. The CSI drive has the features of simple structure:

1. Reliable short circuit protection
2. Four quadrant operation capability and nearly sinusoidal outputs.
3. Low output dv/dt resulting from filtering effect of output capacitors.
4. In addition, the switching device [symmetrical GTO or gate commutated thyristor (GCT)] used in the CSI can be easily connected in series, which makes the CSI drive particularly suitable for implementation at medium voltage (2300 V–7200 V) levels.

These advantages outweigh the other disadvantages of the CSI topology.

The Current Source PWM Rectifier can be used as the front end as a DC link source. The rectifier can be operated at unity power factor. Figure 4.2 shows the schematic diagram of a PWM CSR and CSI fed induction motor drive.

As compared with VSI there is intense need for developing modulation and control strategies for CSI. The performance of CSI in very high power applications still holds good essentially due to the ruggedness and ability to meet load demands easily.

The six-step or square wave inverters switching leads to large amount of harmonics in load voltage and current, the widespread application of this inverter has been curbed [1].

The PWM CSI are feasible with the advent of GTO's, but due to the restriction on switching speed, this approach has limited application. Hence the PWM CSI are less common in practice than VSI PWM inverters, in comparison with a square wave inverter. PWM CSI topology has the output filter capacitors to remove the harmonics due to the switching currents [4.1]. Topologies as shown in Figure 4.1 wherein the IGBT is in series with the diode has distinct disadvantage of low efficiency because in every period of conduction, the total loss is loss in series diode and IGBT which is twice much higher than that in VSI counterpart in very high power applications.

In spite of these drawbacks, the performance of CSI with IGBT in series with diode is being explored with high performance adaptive PWM algorithms. It should be possible to stretch the performance of these topologies to obtain high quality AC waveforms along with higher output power by utilizing various or adaptive PWM algorithms.

The following section will explore the utilization of the discontinuous PWM schemes as applied in VSI into a CSI. This will also cover the gating requirements to avoid shorting of adjacent legs, and the logic circuit development. The operation is studied with a current source inverter with R-L load. The performance is examined through both simulation and experimental results.

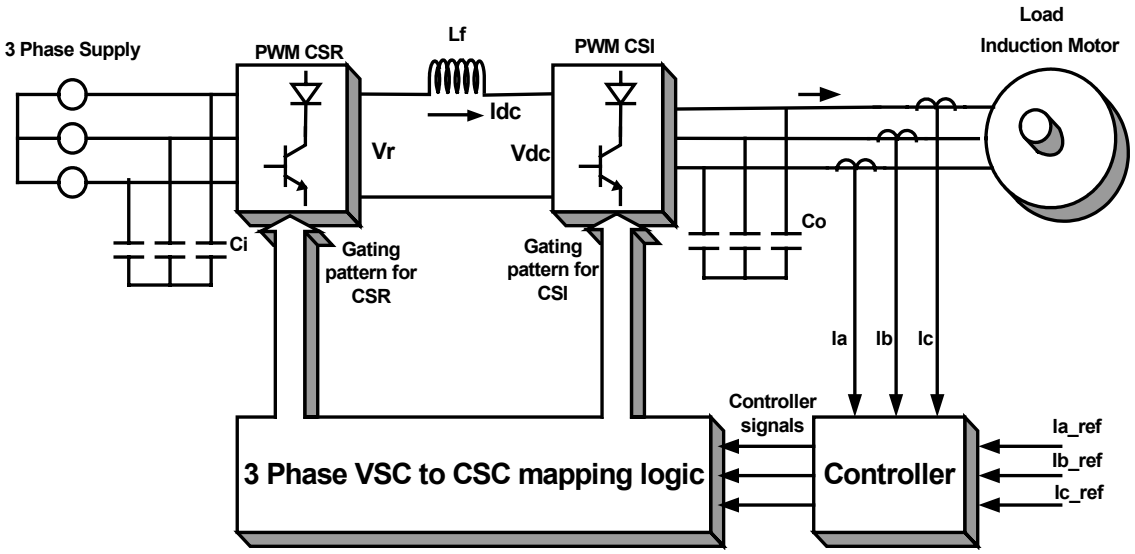


Figure 4.2: Schematic of PWM CSR-CSI drive for induction machine

4.2 Previous PWM Schemes in three phase CSI

In VSI PWM schemes where in by adding zero sequence voltages to the existing modulating signals in high modulation region, the switching loss, voltage linearity, and over modulation performance of the inverter is optimized [4.16]. In a similar way if we can adapt these modulation strategies into a CSI then the advantages of the modulation schemes in VSI can be extended to a CSI.

The online carrier based PWM scheme [4.11-4.13] is the easiest to be implemented. Using the state concepts developed for CSI and VSI it is clear that by any CSI can be controlled by any VSI modulation strategy if the active states created by the modulator are mapped to the stationary vectors and to the switching combinations

associated with these vectors. In developing this scheme, it is necessary to determine how the CSI null state should be related to the modulator state outputs.

In case of VSI with every sine triangle comparison there is implicit transition through the null states and thus is not a separate part of the modulation process. Whereas in case of CSI there is no direct mapping of the sine triangle output for the corresponding null states of a CSI. Hence the null states have to be defined explicitly. This chapter has detailed explanation of this mapping scheme. The various issues confronted and its solutions will be explicated.

As compared with VSI there is intense need for developing modulation and control strategies for CSI. Previous work [4.1-4.4] shows that the CSI gating requirements are more complex than those of the VSI. Most of the modulation schemes are developed as dedicated schemes or offline programmed patterns to optimize switching in contrast to mapping the required states from the VSI modulating schemes. From the space vector perspective though the CSI and VSI are not exactly dual of each other, one can actually map the VSI schemes in to CSI.

4.3 Development of the gating schemes for CSI.

In complying with Kirchoff's voltage (KVL) and current (KCL) law, the VSI is restricted in the sense that both the devices in a leg cannot be on at the same, else it would result in shorting of the DC link capacitor. But it does allow the shorting of the adjacent legs. Similarly for CSI it is mandatory that only one device in the top and only one in the bottom is on at a time, else the output capacitors will be shorted but it does

allow the shorting of the same leg. Table 4.1 gives the switching states available in a voltage source converter while Table 4.2 gives the switching states available in a current source converter.

Table 4.1 : Switching States in a 3 phase VSI

State	S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}	
Null, S_0	0	0	0	1	1	1	S_{an} S_{bn} S_{cn}
S_1	0	0	1	1	1	0	S_{cp} S_{an} S_{bn}
S_2	0	1	0	1	0	1	S_{bp} S_{an} S_{cn}
S_3	0	1	1	1	0	0	S_{bp} S_{cp} S_{an}
S_4	1	0	0	0	1	1	S_{ap} S_{bn} S_{cn}
S_5	1	0	1	0	1	0	S_{ap} S_{cp} S_{bn}
S_6	1	1	0	0	0	1	S_{ap} S_{bp} S_{cn}
Null, S_7	1	1	1	0	0	0	S_{ap} S_{bp} S_{cp}

Table 4.2 : Switching States in a 3 phase CSI

	State	h_1	h_2	h_3	h_4	h_5	h_6
ACTIVE	h_1h_2	1	1	0	0	0	0
	h_2h_3	0	1	1	0	0	0
	h_3h_4	0	0	1	1	0	0
	h_4h_5	0	0	0	1	1	0
	h_5h_6	0	0	0	0	1	1
	h_6h_1	1	0	0	0	0	1
NULL	h_1h_4	1	0	0	1	0	0
	h_2h_5	0	1	0	0	1	0
	h_3h_6	0	0	1	0	0	1

The active states are used to produce the required output voltages while the null states are used to remove the energy stored in the input inductor.

The objective here is to obtain Tables 4.2 and 4.1 subject to the following conditions of KVL and KCL these can be laid out as:

$$S_{ap} + S_{bp} + S_{cp} = 1 ,$$

$$S_{an} + S_{bn} + S_{cn} = 1 \qquad (4.1)$$

another necessary condition is that the product of any of the top 2 devices at any given time should always be zero.

$$S_{ap}.S_{bp} = 0 ,\ S_{bp}.S_{cp} = 0 ,\ S_{ap}.S_{cp} = 0 \qquad (4.2)$$

$$S_{an}.S_{bn} = 0 ,\ S_{bn}.S_{cn} = 0 ,\ S_{an}.S_{cn} = 0 \qquad (4.3)$$

The KVL and KCL conditions pre-applied to voltage source inverter are:

$$S_{ap} + S_{an} = 1,\ S_{bp} + S_{bn} = 1,\ S_{cp} + S_{cn} = 1 \tag{4.4}$$

and

$$S_{ap}.S_{an} = 0$$

$$S_{bp}.S_{bn} = 0$$

$$S_{cp}.S_{cn} = 0 \tag{4.5}$$

The 8 feasible switching modes of the three phase VSI are given in Table 4.1 . The stationary reference frame qdo voltages of the switching modes are expressed in the complex variable form as ($a = e^{j\beta}$, $\beta = 120°$) :

$$V_{qds} = 2/3(V_{an} + aV_{bn} + a^2V_{cn}),\ V_o = 1/3(V_{an} + V_{bn} + V_{cn}). \tag{4.6}$$

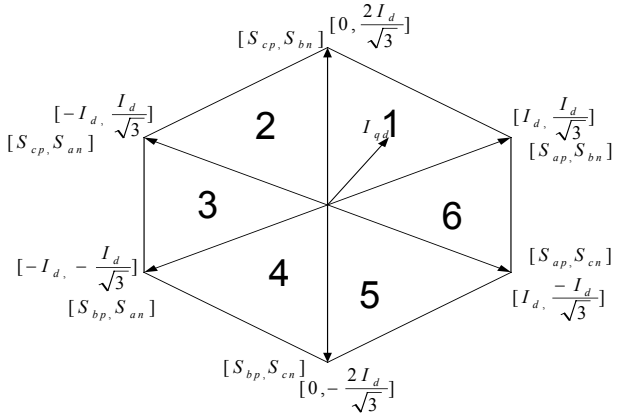
Using the phase to reference voltages V_{ao}, V_{bo}, and V_{co} for each switching mode, the components of the stationary reference frame V_{qdos} expressed in terms of the switching functions are given as :

$$V_{qs} = 1/6(2S_{ap} - S_{bp} - S_{cp} - 2S_{an} + S_{bn} + S_{cn})V_d,$$

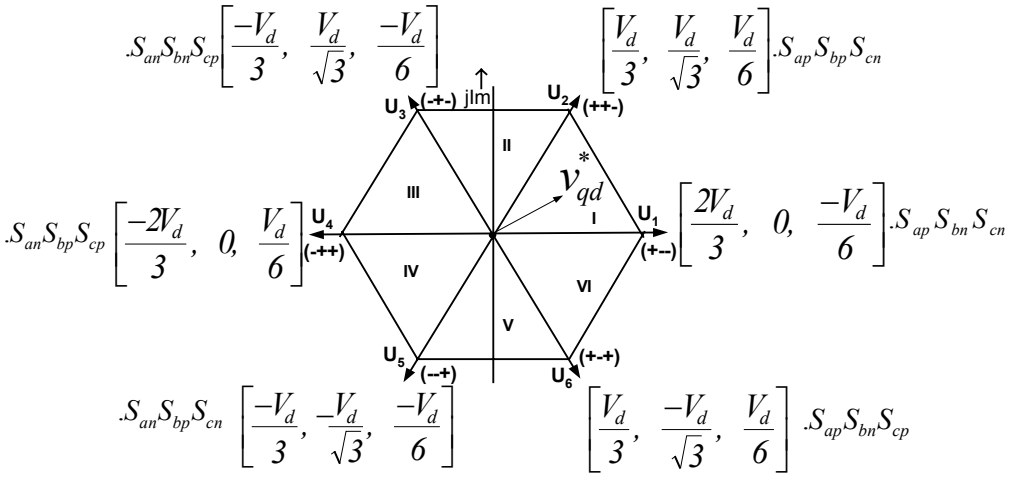
$$V_{ds} = 1/2\sqrt{3}(S_{cp} - S_{bp} - S_{cn} + S_{bn})V_d, \tag{4.7}$$

$$V_o = 1/6(S_{ap} + S_{bp} + S_{cp} - S_{an} - S_{bn} - S_{cn})V_d$$

S_{ip} and S_{in} for i =a,b,c are the switching functions of top (p) and bottom (n) for the phases. Based on the stationary reference frame q-d-o voltages and currents space vector diagrams, one can observe the relevance between the VSI and CSI. It is notable that there is one to one correspondence between the active states of VSI and CSI.



(a)



(b)

Figure 4.3 3-D Plot of Stationary qdo voltages and currents for the given states of (a) CSI (b) VSI

Figure 4.3 (b) shows eight possible space vectors for VSI of which 6 are active states and two are null states. As shown in Figure 4.3(a) CSI have nine possible space vectors of which six are active and three are null vectors. It is conspicuous that the angles between active space vectors are 60° for VSI and CSI and the CSI space vector lead the VSI space vector by 30 in an absolute sense [13]. From [9], there is one to one correspondence between the active states of VSI and CSI, hence the mapping is simple.

Table 4.3: Switching modes of the three-phase voltage source inverter and corresponding stationary reference frame qdo voltages.

Mode	S_{ap}	S_{bp}	S_{cp}	V_{qs}	V_{ds}	V_{os}
1	0	0	0	0	0	$-V_d/2$
2	0	0	1	$-V_d/\sqrt{3}$	$V_d/\sqrt{3}$	$-V_d/6$
3	0	1	0	$-V_d/3$	$-V_d/\sqrt{3}$	$-V_d/6$
4	0	1	1	$-2V_d/3$	0	$V_d/6$
5	1	0	0	$2V_d/3$	0	$-V_d/6$
6	1	0	1	$V_d/3$	$-V_d/\sqrt{3}$	$V_d/6$
7	1	1	0	$V_d/3$	$V_d/\sqrt{3}$	$V_d/6$
8	1	1	1	0	0	$V_d/2$

Table 4.4: Switching modes of the three-phase current source inverter and corresponding stationary reference frame qdo currents.

ON Device	ON Device	I_{as}	I_{bs}	I_{cs}	I_{qq}	$\sqrt{3}\, I_{dd}$
S_{ap}	S_{bn}	I_d	$-I_d$	0	I_d	I_d
S_{ap}	$.S_{cn}$	I_d	0	$-I_d$	I_d	$-I_d$
S_{bp}	S_{an}	$-I_d$	I_d	0	$-I_d$	$-I_d$
S_{bp}	S_{cn}	0	I_d	$-I_d$	0	$-2I_d$
S_{cp}	S_{an}	$-I_d$	0	I_d	$-I_d$	I_d
S_{cp}	S_{bn}	0	$-I_d$	I_d	0	$2I_d$
S_{ap}	S_{an}	0	0	0	0	0
S_{bp}	S_{bn}	0	0	0	0	0
S_{cp}	$.S_{cn}$	0	0	0	0	0

4.4 Mapping technique

From Table 4.1 and 4.2 the mapping procedure is done as follows:

Consider the output state we desire from the available input states. If we combine the VSI states in a particular way we can obtain the desired output states, thus:

$$h_1 = S_1 + S_3 \tag{4.8}$$

taking the complement of both sides we have

$$\overline{h_1} = \overline{S_1 + S_3}$$

$$\overline{h_1} = \overline{S_{cp} S_{an} S_{bn} + S_{bp} S_{cp} S_{an}}$$

$$\overline{h_1} = \overline{S_{cp} S_{an} (S_{bn} + S_{bp})} \tag{4.9}$$

now using the property of

$\overline{A.B} = \overline{A} + \overline{B}$ and $\overline{A + B} = A.B$ we have,

$$\overline{h_1} = \overline{S_{cp} S_{an}} + \overline{(S_{bn} + S_{bp})} = \overline{S_{cp} S_{an}} + S_{bn} S_{bp} = \overline{\overline{S_{cn}}.\overline{S_{ap}}} + S_{bn} S_{bp}$$

using the property $\overline{\overline{A}.\overline{B}.} = A.B$ we have

$$h_1 = S_{cn} S_{ap} + S_{bn} S_{bp} . \tag{4.10}$$

Here the first term corresponds to the active state while the second term corresponds to a null state in CSI. The remaining CSI states are listed as:

$$h_2 = S_{cn} S_{bp} + S_{an} S_{ap} \tag{4.11}$$

$$h_3 = S_{bp} S_{an} + S_{cn} S_{cp} \tag{4.12}$$

$$h_4 = S_{cp} S_{an} + S_{bn} S_{bp} \tag{4.13}$$

$$h_5 = S_{cp} S_{bn} + S_{an} S_{ap} \tag{4.14}$$

$$h_6 = S_{bn} S_{ap} + S_{cn} S_{cp} \tag{4.15}$$

It is evident from these expressions that any VSI state combination results in a combination of a CSI active state and a null state. The truth tables for the expressions are summarized in Table 4.5.

Table 4.5 Derivation of the desired states from the available states

						h_1	h_2	h_3	h_4	h_5	h_6
S_{ap}	S_{bp}	S_{cp}	S_{an}	S_{bn}	S_{cn}	$S_{ap}S_{cn}+S_{bp}S_{bn}$	$S_{bp}S_{cn}+S_{ap}S_{an}$	$S_{bp}S_{an}+S_{cp}S_{cn}$	$S_{cp}S_{an}+S_{bp}S_{bn}$	$S_{cp}S_{bn}+S_{ap}S_{an}$	$S_{ap}S_{bn}+S_{cp}S_{cn}$
0	0	0	1	1	1	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	1	1	0
0	1	0	1	0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0	1	1	0	0
1	0	0	0	1	1	1	0	0	0	0	1
1	0	1	0	1	0	0	0	0	0	1	1
1	1	0	0	0	1	1	1	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0

From the Table 4.5 it can be noted that only one device in the top and bottom is ON at any given time. However according to condition given by Equation 4.4 it is evident that this null state can never be mapped in CSI because the output of this product term will always be zero. This scheme as on its own can be used for generating the gating signals for a CSI but it won't allow the utilization of the available three null states $S_{ap}S_{an}$, $S_{bp}S_{bn}$, and $S_{cp}S_{cn}$ of the CSI.

4.6 Shorting Pulses and its Distribution

There is a necessity to introduce the null states in conjunction with the active states. Thus an additional condition for minimization of the number of switch transitions, ,maintain balanced switch utilization and reduction of losses can be imposed

[4.11],[4.12]. This should also ensure the symmetry in the output switched currents in order to have minimum harmonic distortion. To satisfy the above requirement a logic circuit is developed to detect the condition when the null state has to be applied. This logic circuit detects a NULL state whenever all the devices in the top and/or bottom are found to be zero. This condition corresponds to the highlighted section in Table 4.5. Once the condition for null state is detected one of the three legs of the CSI has to be shorted. This is done by gating the devices in the same leg by a common signal, which will be termed as a *shorting pulse*.

From the VSI states the occurrence of the null states causes a train of shorting pulses hence the main issue arising here is the distribution of these shorting pulses in the given cycle. In order to have minimum harmonics on the output waveform, the distribution has to be symmetric. Hence we refer back to Table 4.6 and Figure 4.5 to study this aspect. It is known that in a three- phase system each phase voltage is maximum/minimum for 120° in every cycle. If the line-line voltages are considered, then the maximum/minimum is 120° but distributed 60° in a cycle. This 60° distribution is essential for generation of symmetric output current waveforms. For example, V_{ap} has its maximum occurring in sector I for 60° and VI for 60°, thus the effective period for which the amplitude of V_{ap} is maximum is 120° but it is distributed by 60° in a cycle. It is also known that this sequence can be achieved using the absolute maximum of the line-line voltages of the reference signals.

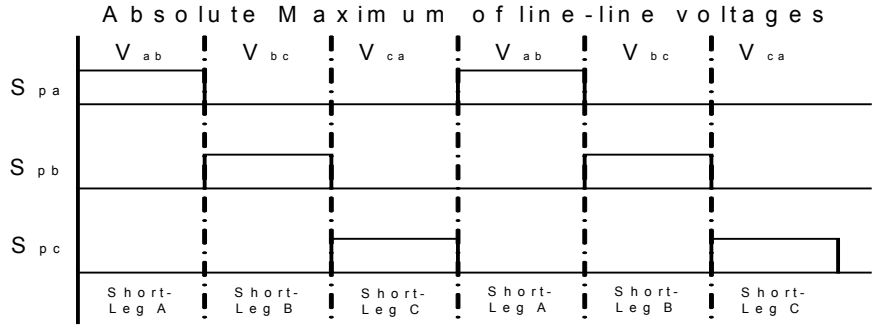


Figure 4.4 Generation of the Distribution pulses for shorting a leg in CSI

Table 4.6: Device Switching times expressed in terms of reference line-line voltages

Sector	I	II	III	IV	V	VI
Max Volt	V_{ap}	V_{bp}	V_{bp}	V_{cp}	V_{cp}	V_{ap}
Min Volt	V_{cp}	V_{cp}	V_{ap}	V_{ap}	V_{bp}	V_{bp}

V_{ab}, V_{bc}, V_{ca}

V_{an}, V_{bn}, and V_{cn}

Abs max (V_{ab}, V_{bc}, V_{ca})

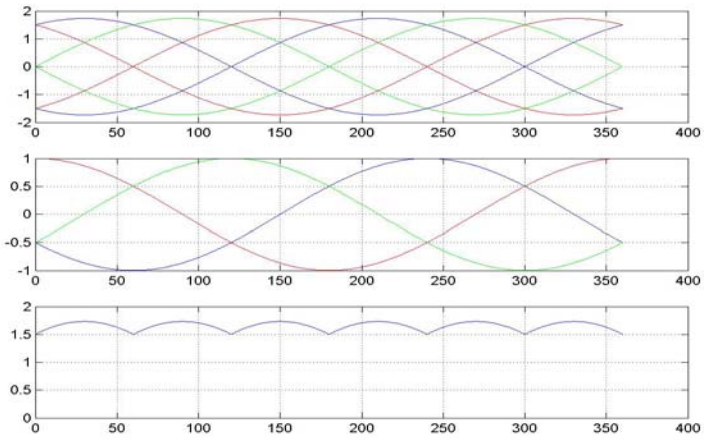


Figure 4.5 Generation of distribution logic for the NULL states

One can get the same result as explained above by the use of absolute maximum of line-line voltages. Using maximum of phase voltages V_{an}, V_{bn}, and V_{cn} will give a distribution of 120° in a cycle, but this results in asymmetric output currents. It will result in half wave symmetry and eventually more harmonics on the output currents. Thus the using absolute maximum of line-line voltages is a better option so that when line-line voltage V_{ab} is maximum we short leg 'A', V_{bc} is maximum we short leg B, V_{ca} is maximum we short leg C.

4.7 Practical scheme layout and gating pattern signals

Figure 4.6 shows the practical scheme for implementing the VSI to CSI mapping.

The PWM switching signals obtained from the output of the DSP are recombined to generate Table 4.1. Thus S_1 through S_7 are the outputs of the logic gates corresponding to the VSI states. These states are recombined using equations 4.8 through 4.13 to obtain the states listed in Table 4.2.

The third condition is for the detection of null states and their distribution logic. The null state logic detector activates $S_d = 1$ whenever sum of all the devices in the top and bottom are found to be zero. This S_d in combination with the distribution logic generates shorting pulses of the corresponding leg. The calculation of the absolute maximum of the reference signals is done internally in the DSP to generate the distribution signals $S_{pA,}$ $S_{pB,}$ and $S_{pC.}$

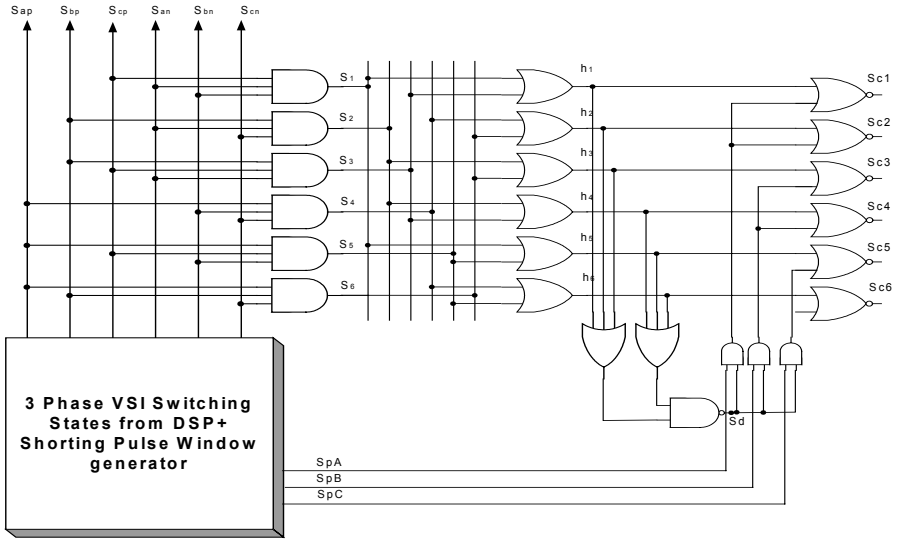


Figure 4.6 Implementation of the scheme as listed in Table 4.4

4.7.1 Gating pattern signals for developed scheme:

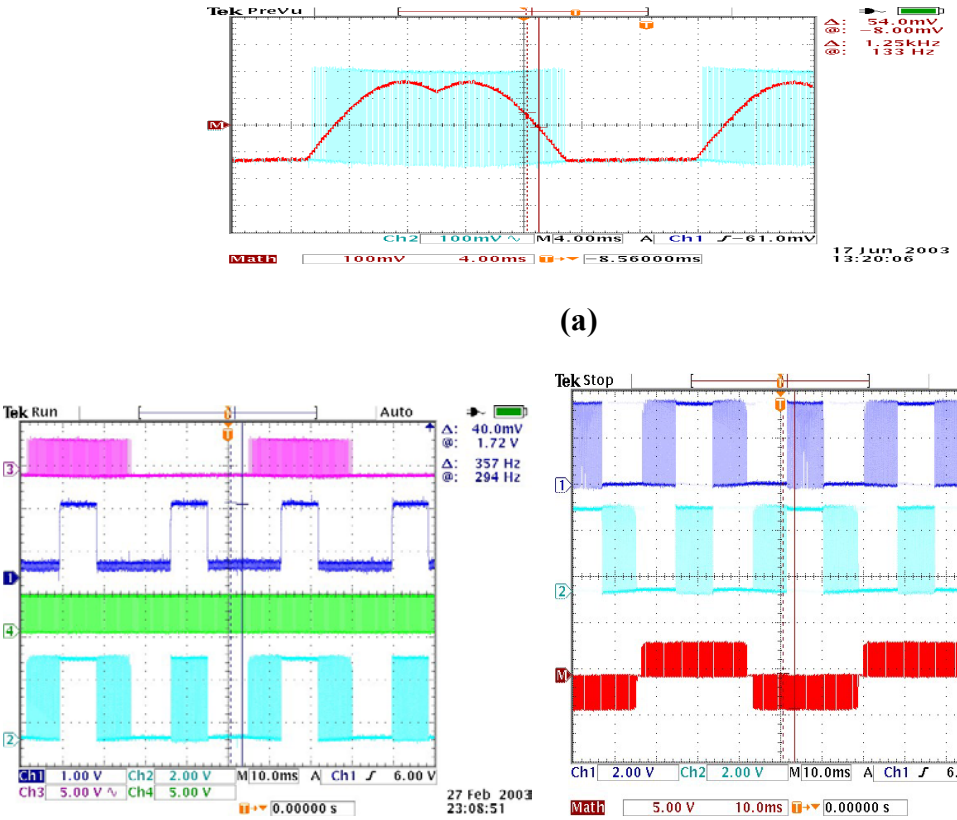


Figure 4.7 Experimental results generation of gating signals

Figure 4.7 (a) and similarly Scope 3 shows the generation of VSI switching states for S_{ap}. Scope 1 is the distribution logic pulse S_{pA}, which corresponds to maximum is AB amongst Absolute max (V_{ab}, V_{bc}, V_{ca}). Scope 4 is the occurrence of the null states during the VSI operation. These shorting pulses are supposed to be distributed through distribution pulses. Scope 2 is the final gating signal generated for the top device in phase'a' of the CSI. Figure (c) shows the gating pulse for the top and bottom device, and the generated current waveform. $I = I_d(S_{csi1} - S_{csi4})$

4.8 Modeling of CSI in a-b-c reference frame

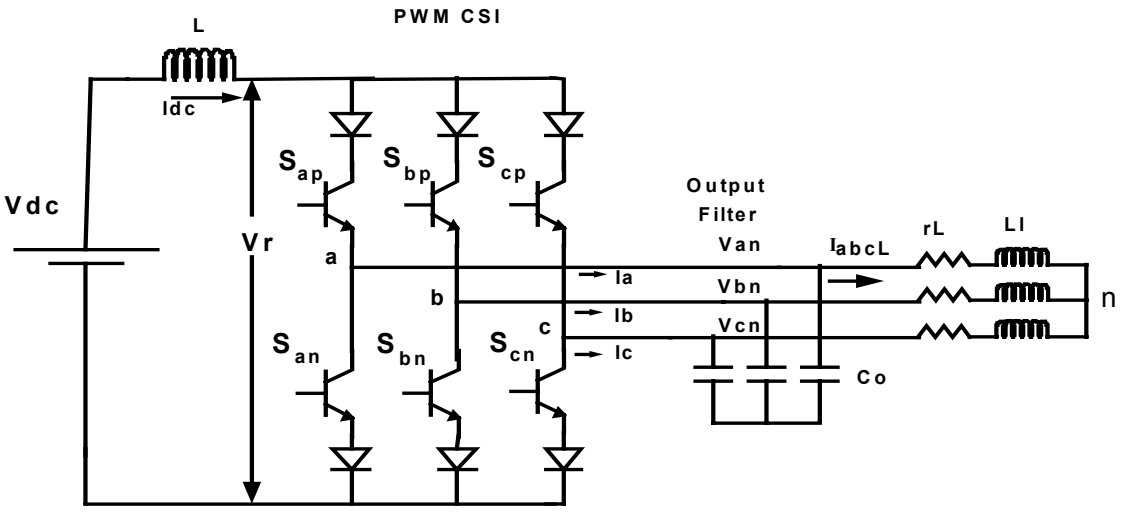


Figure 4.8 Modeling structure of a CSI

Table 4.7: Terminology used in modeling of CSI

Parameters	Description
V_{abcn}	Output phase voltages
I_{abcn}	Output line currents
I_{abcl}	Output load currents
I_{dc}	Input DC link current
V_{dc}	Input source voltage
V_r	Voltage at the output of the input inductor
S_{abcp} , S_{abcn}	Top and bottom switching devices
r_l , L_l	Output load resistance and inductance
C_o	Output Filter capacitor

From Figure 4.7 the input DC voltage to the CSI is given as:

$$V_r = (S_{ap}V_{an} + S_{bp}V_{bn} + S_{cp}V_{cn}) - (S_{an}V_{an} + S_{bn}V_{bn} + S_{cn}V_{cn})$$

hence,

$$V_r = (S_{ap} - S_{an})V_{an} + (S_{bp} - S_{bn})V_{bn} + (S_{cp} - S_{cn})V_{cn} \tag{4.16}$$

Thus the drop across the DC link inductor is given as:

$LpI_{dc} = V_{dc} - V_r$ or

$$LpI_{dc} = V_{dc} - (S_{ap} - S_{an})V_{an} + (S_{bp} - S_{bn})V_{bn} + (S_{cp} - S_{cn})V_{cn} \tag{4.17}$$

Now the unfiltered currents are given by

$$I_a = (S_{ap} - S_{an})I_{dc}$$

$$I_b = (S_{bp} - S_{bn})I_{dc}$$

$$I_c = (S_{cp} - S_{cn})I_{dc} \tag{4.18}$$

The currents flowing through the output filter capacitor are given by

$$C_o pV_{an} = I_a - I_{al}$$

$$C_o pV_{bn} = I_b - I_{bl}$$

$$C_o pV_{cn} = I_c - I_{cl} \tag{4.19}$$

and the load can be expressed as:

$$V_{an} = r_L I_{al} + L_L pI_{al}$$

$$V_{bn} = r_L I_{bl} + L_L pI_{bl}$$

$$V_{cn} = r_L I_{cl} + L_L pI_{cl} \tag{4.20}$$

Thus equations 4.16 through 4.20 can be used for simulating the CSI.

4.9 Simulation and Experimental Results

The simulation and experimental results were performed on a current source inverter with an R-L load of 30 ohm and 4mH respectively at modulation index m = 0.96 and m = 1.5 (Over modulation). It can be seen that the experimental and simulation results have a very close correspondence. The difference is be due to the inconsideration of nonlinearties in the switching devices.

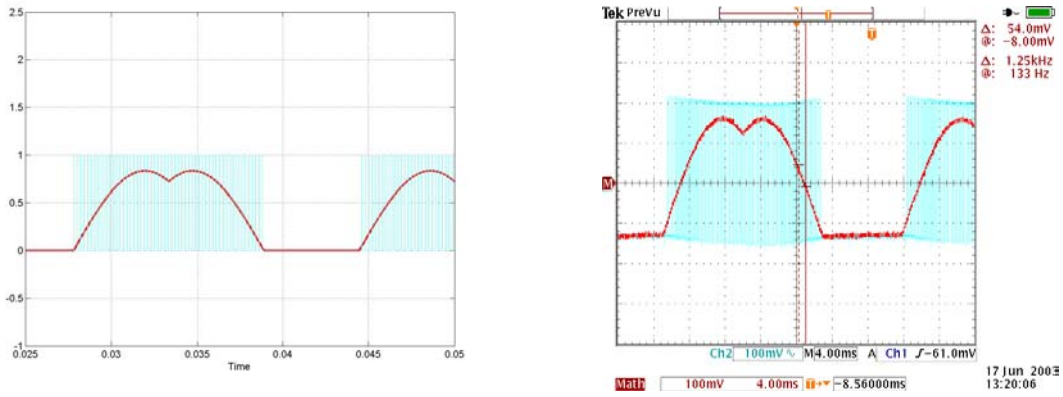
The objective was to observe the performance of various modulating schemes on the inverter output voltages and currents. Hence the FFT of the filtered output voltage and current was done to see the difference in the various PWM schemes.

It is observed that for a given 'm' all these schemes give the same fundamental output voltages irrespective of the modulating schemes. Thus the only difference would lie in the amount of device switching and the output waveform quality.

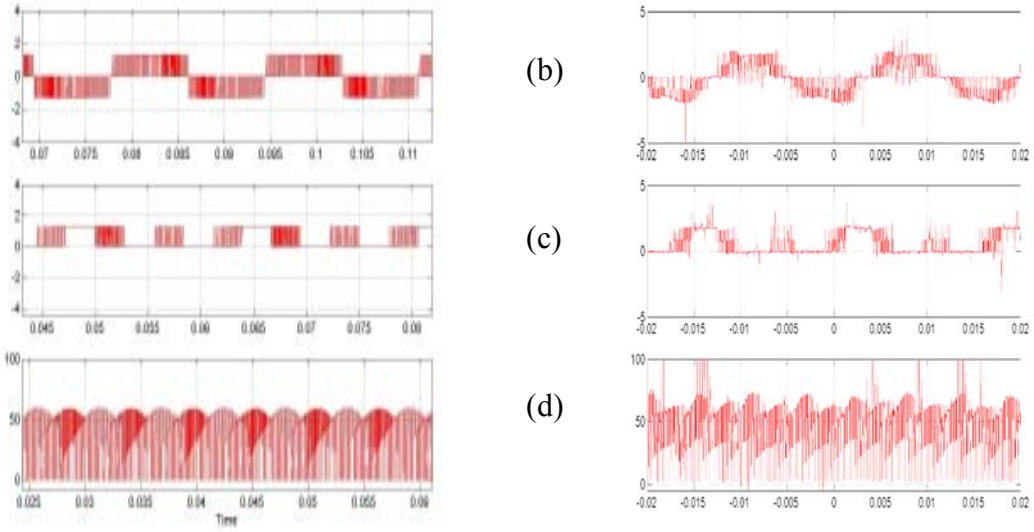
By studying the amount of actual switching performed in a cycle in each modulation shows that space vector PWM with $\beta = 0.5$ has more switching than its discontinuous counterparts to generate the same output voltages.

Following charts Figure 4.8 through 4.11 shows the plot of 3^{rd} and 5^{th} harmonics for each voltage and currents for all the modulating schemes at m= 0.96 and over modulation.

The percent distortion depends on the load power factor. In this particular case the $\alpha = 0$ has least harmonics in both the cases.



(a)



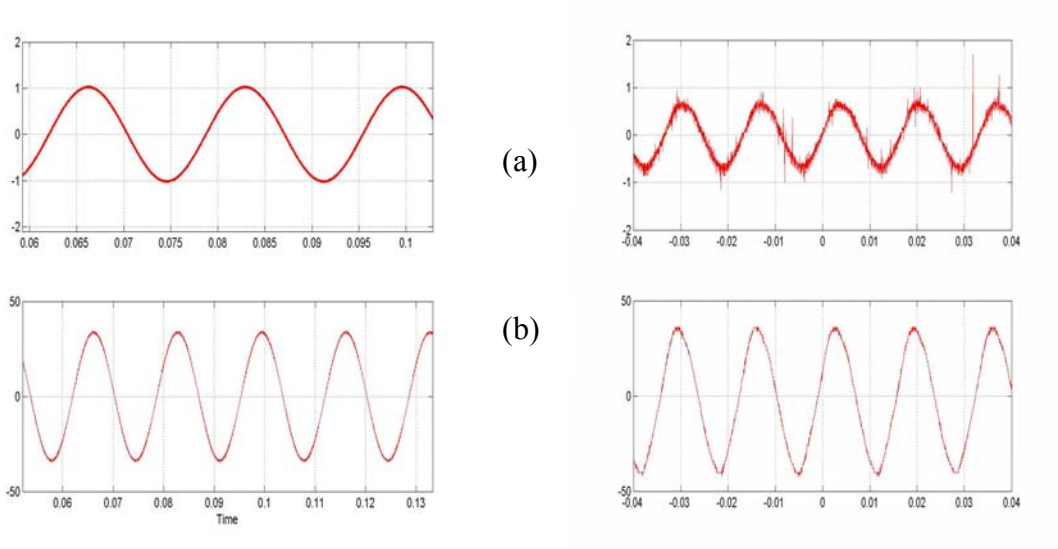
(b)

(c)

(d)

I Simulation **II. Experiment**

Figure 4.9 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.10 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A . (a) Phase 'a' Filtered Out put Current and (b) Voltage

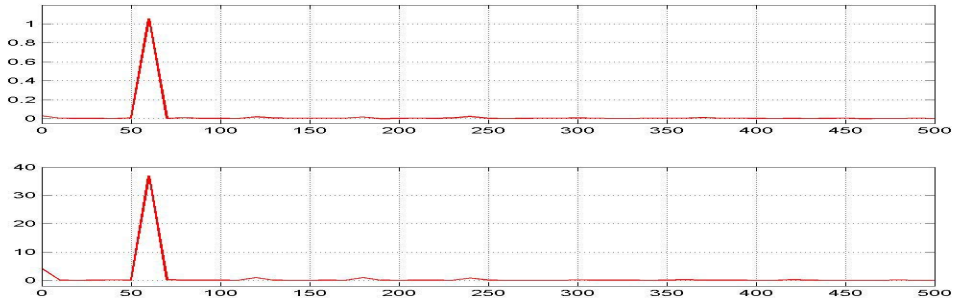
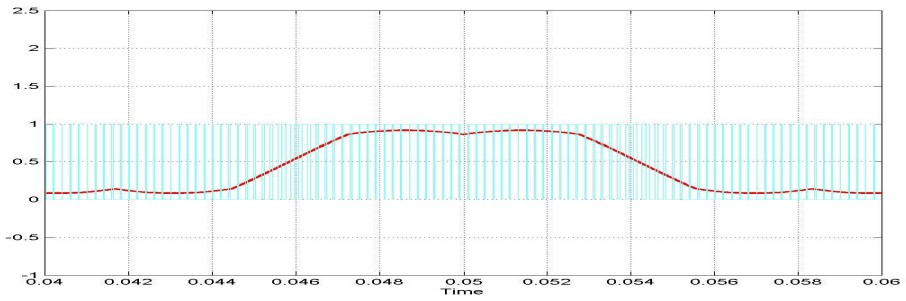
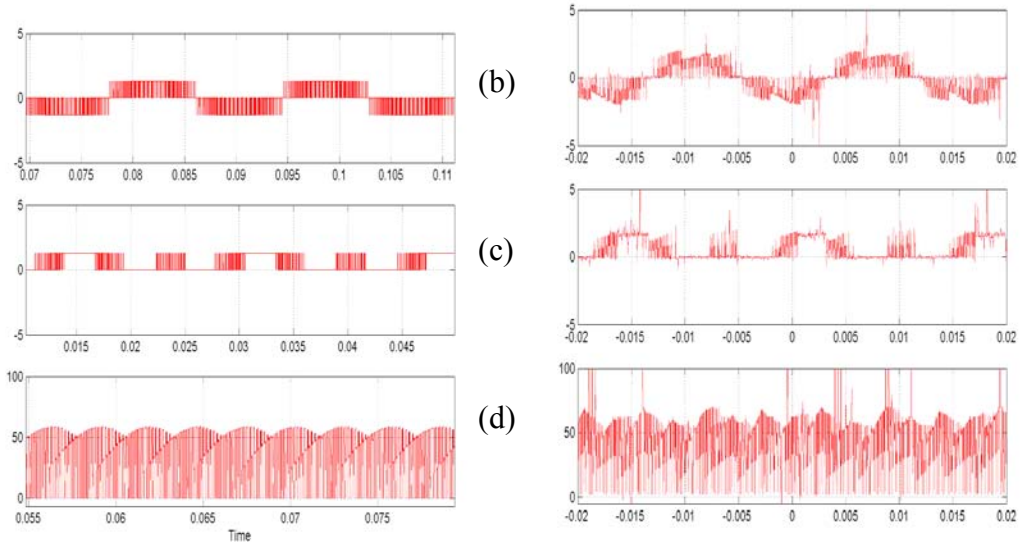


Figure 4.11 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0 and M = 0.96

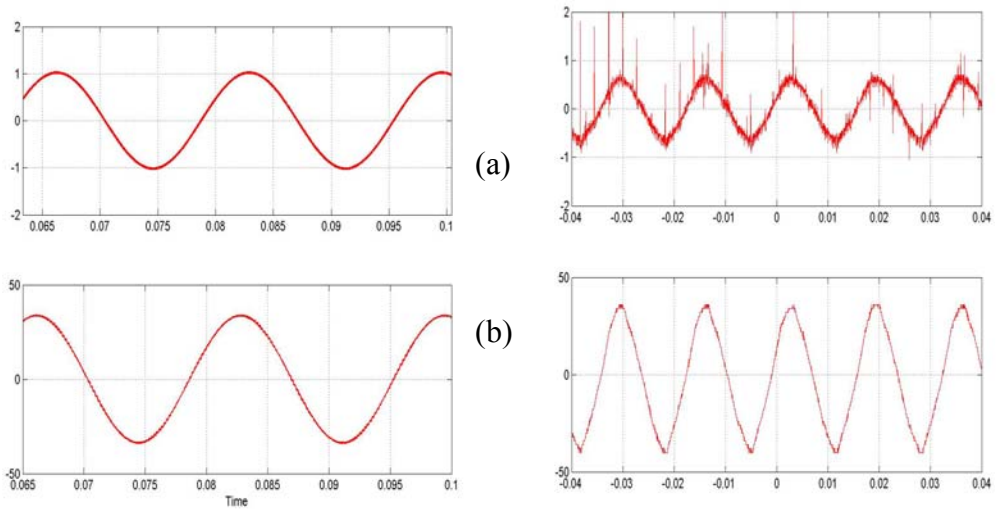


(a)



I Simulation **II. Experiment**

Figure 4.12 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.13 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage

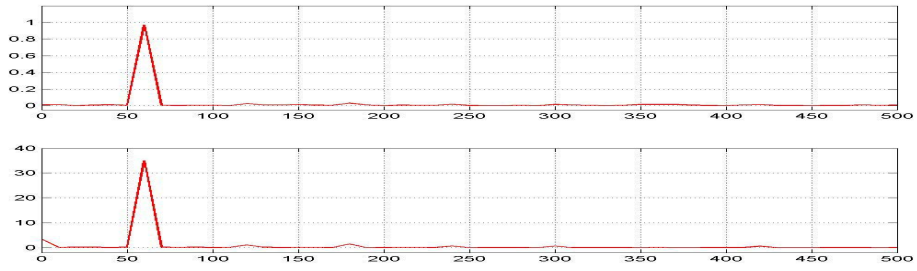
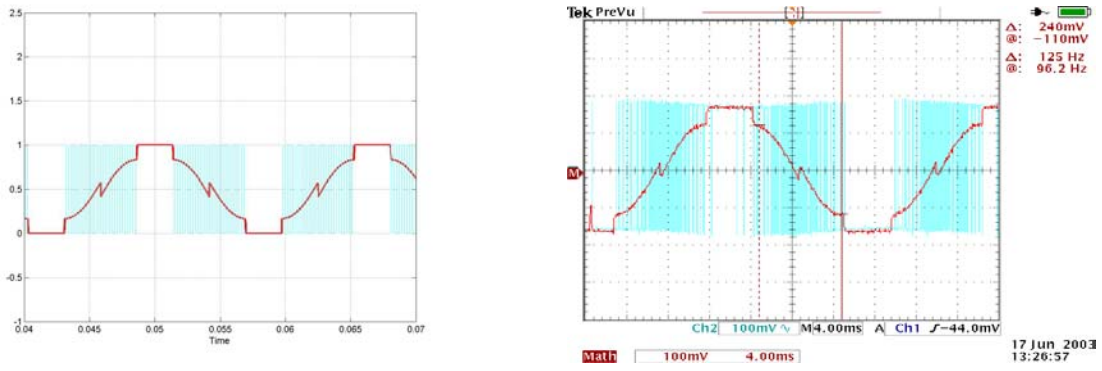
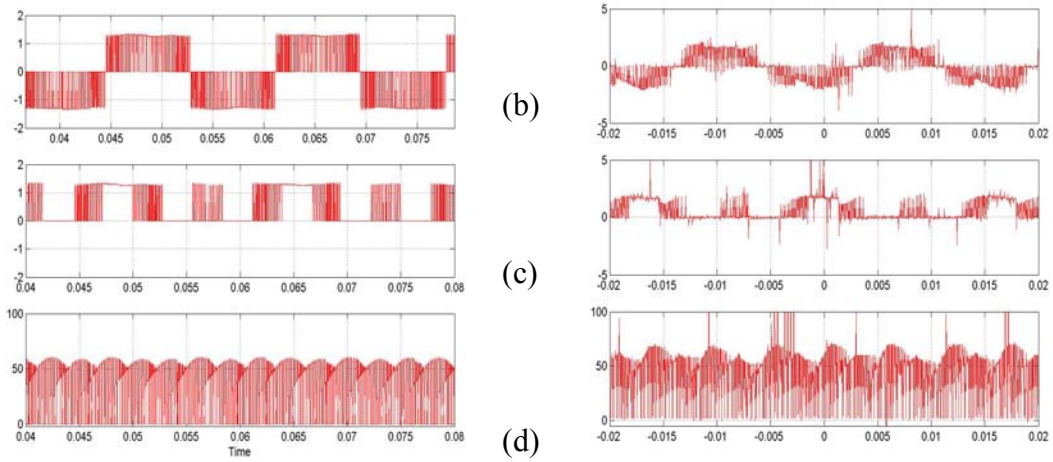


Figure 4.14 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0.5 and M = 0.96



(a)



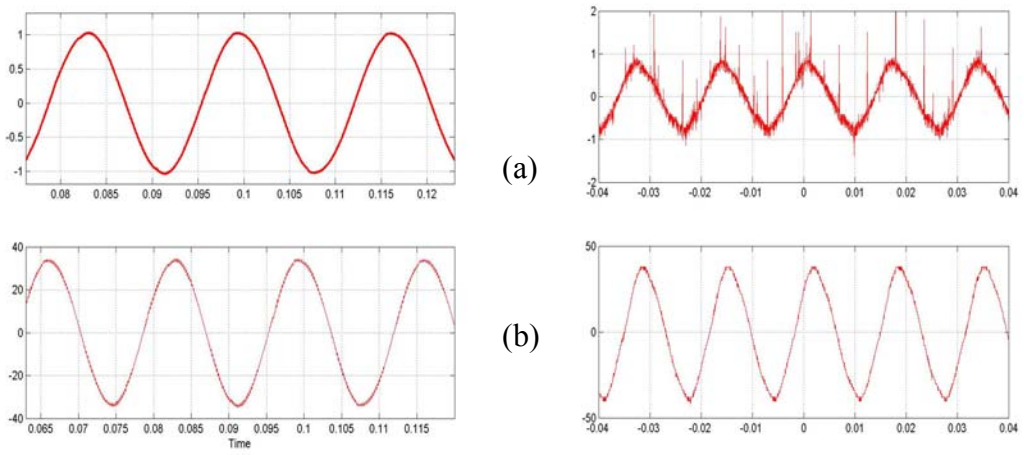
(b)

(c)

(d)

I Simulation **II. Experiment**

Figure 4.15 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM $\beta = 0.5[1 + SgnCos\ 3(\omega t + \delta)]$, $\delta = 0$ modulation feeding an R-L load of ,$R_L = 30\Omega$,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.16 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM $\beta = 0.5[1 + SgnCos\ 3(\omega t + \delta)]$, $\delta = 0$ modulation feeding an R-L load of ,$R_L = 30\Omega$,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage e

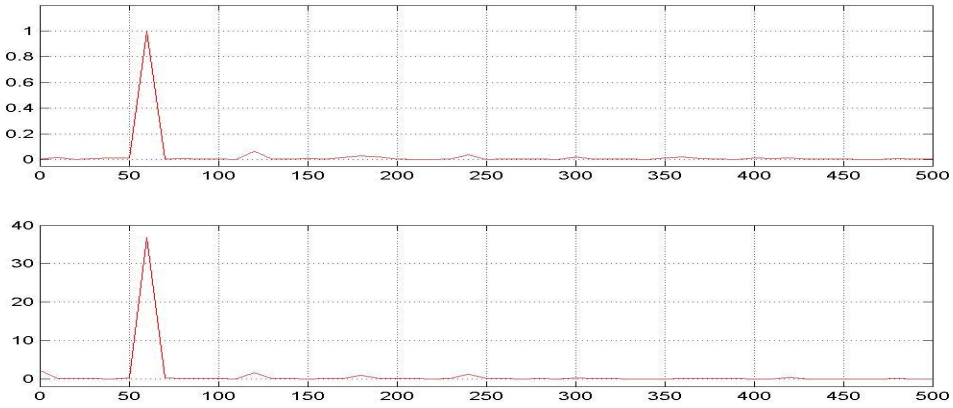
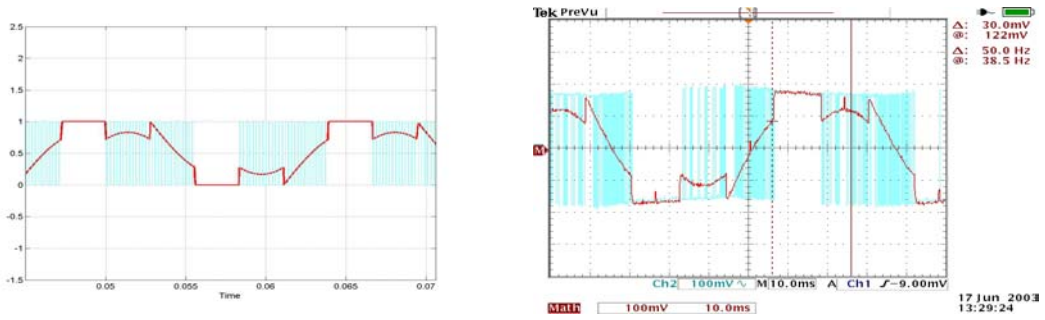
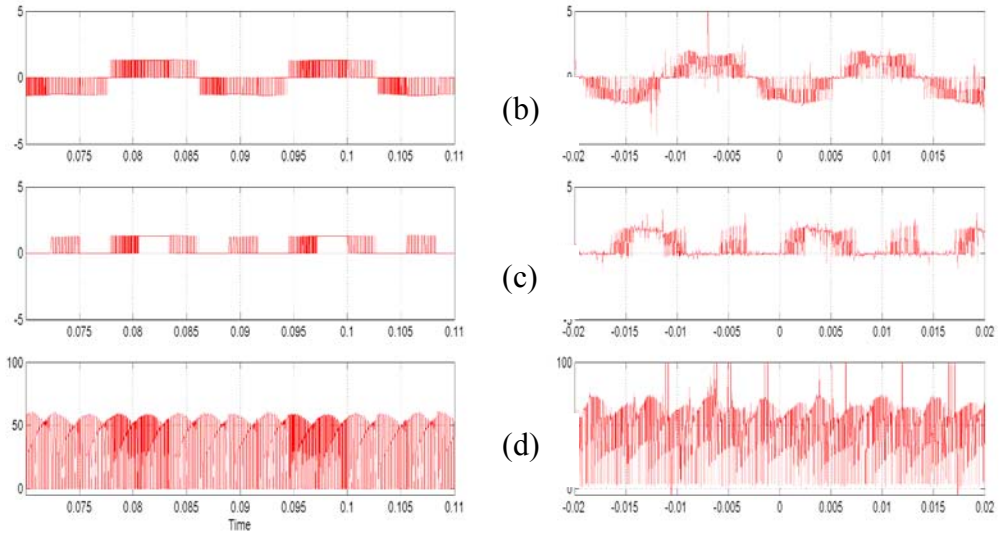


Figure 4.17 FFT of the filtered output voltage and current for the above GDPWM modulating signal $\beta = 0.5[1 + SgnCos\ 3(\omega t + \delta)]$, $\delta=0$ and M = 0.96



(a)



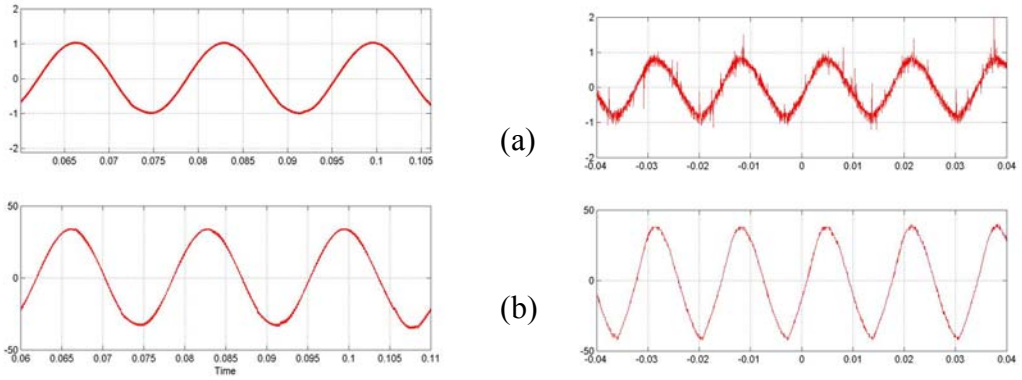
(b)

(c)

(d)

I Simulation **II. Experiment**

Figure 4.18 I&II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ = -30 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.19 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ = -30 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage

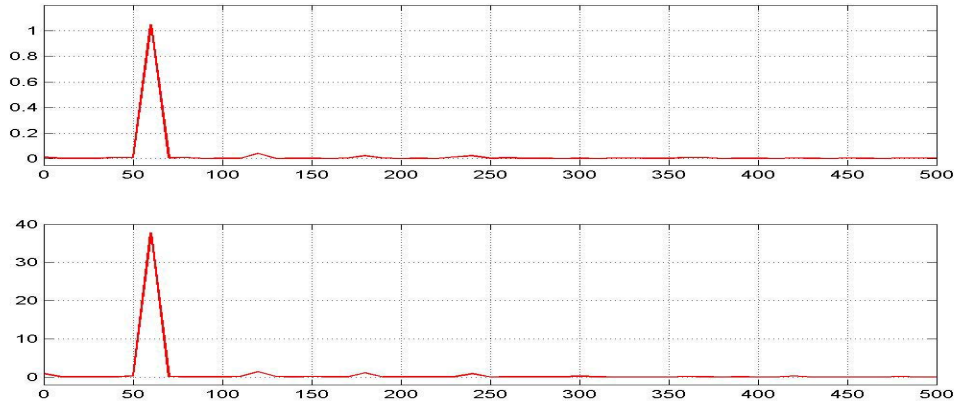


Figure 4.20 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0.5[1 + SgnCos 3(ωt + δ)], δ = -30 and M = 0.96

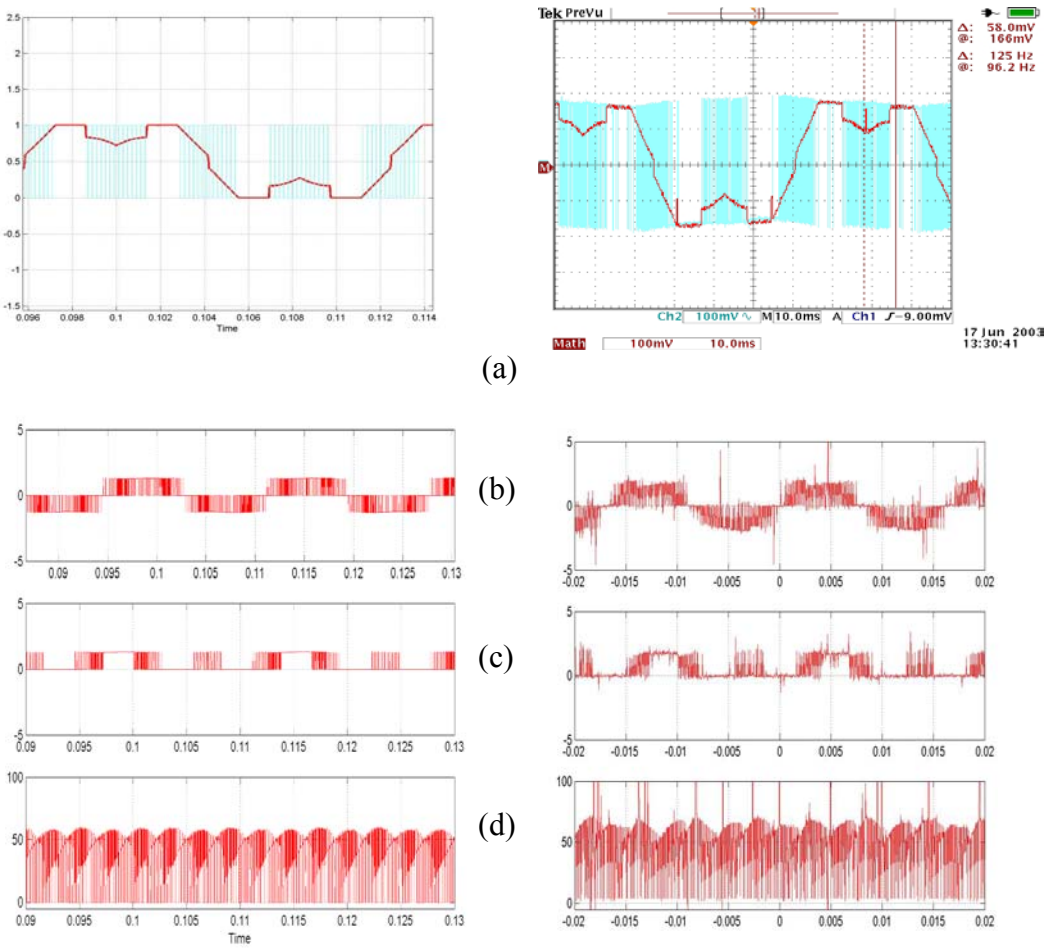
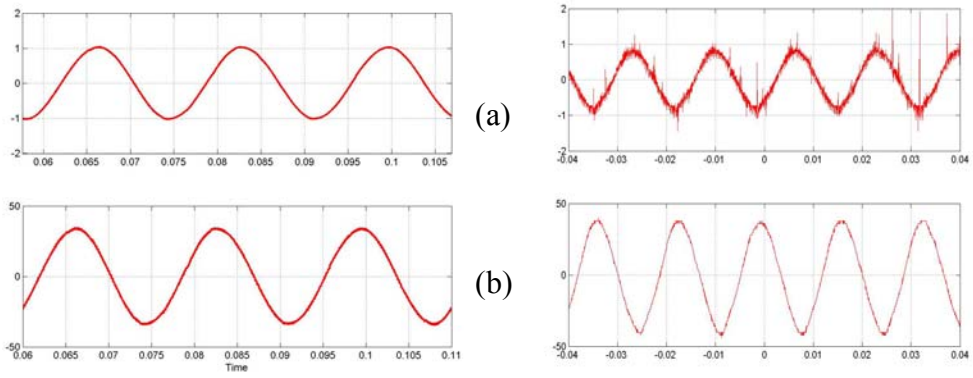


Figure 4.21 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ = -60 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.22 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ=-60 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)Phase 'a' Filtered Out put Current and (b) Voltage

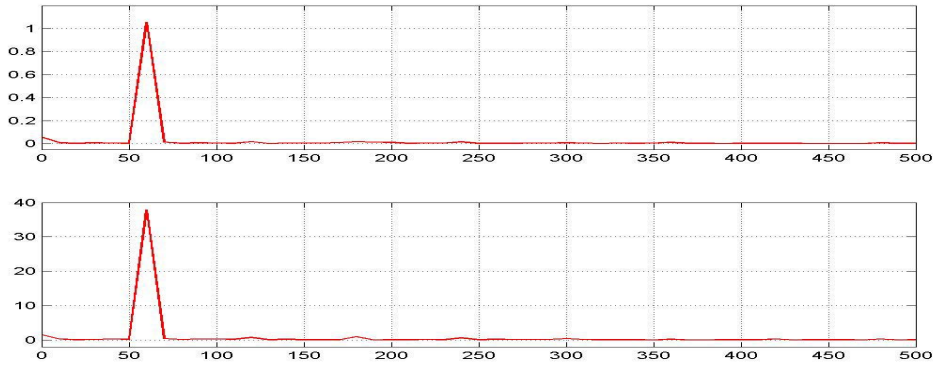


Figure 4.23 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0.5[1 + SgnCos 3(ωt + δ)], δ = -60 and M = 0.96

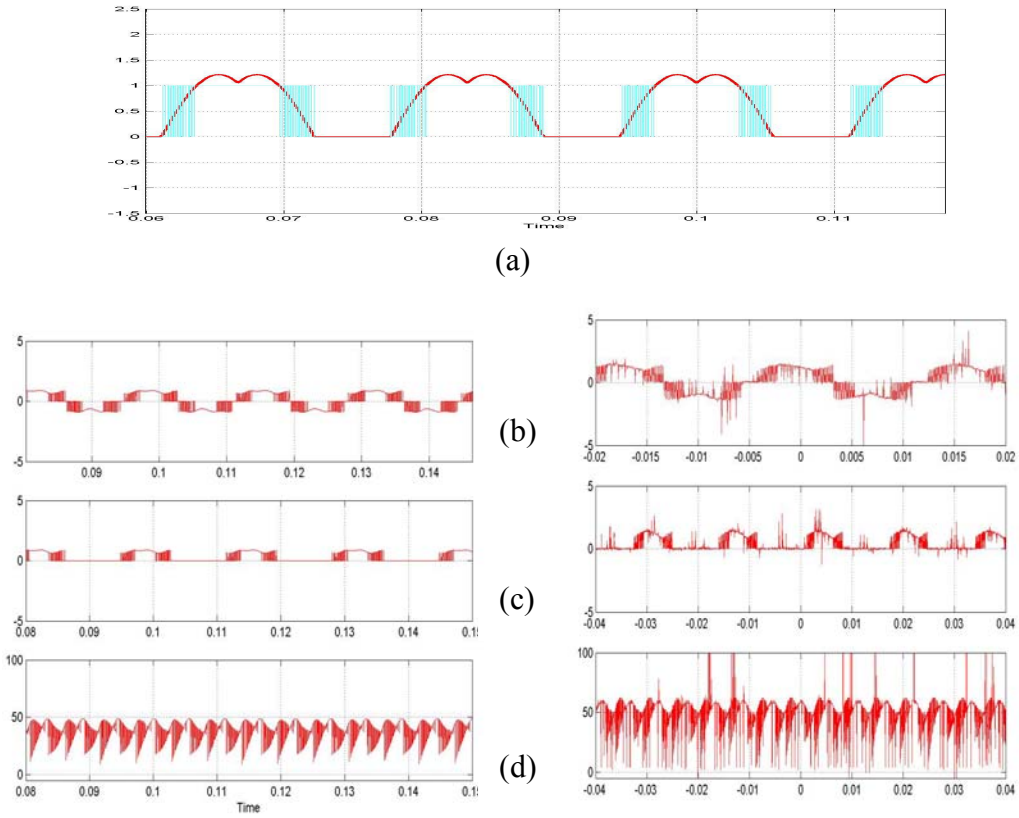
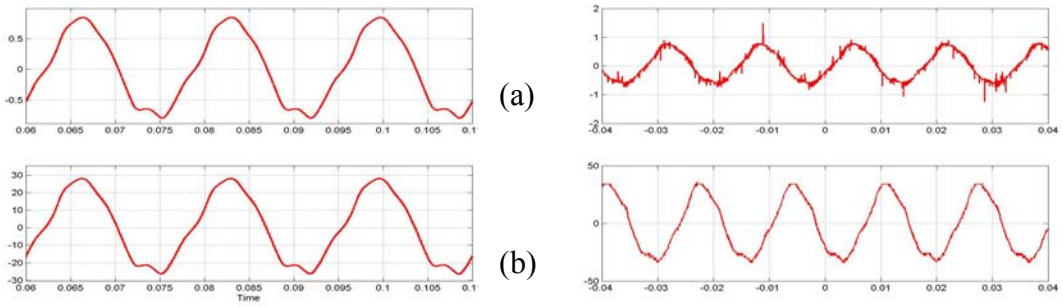


Figure 4.24 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.25 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage

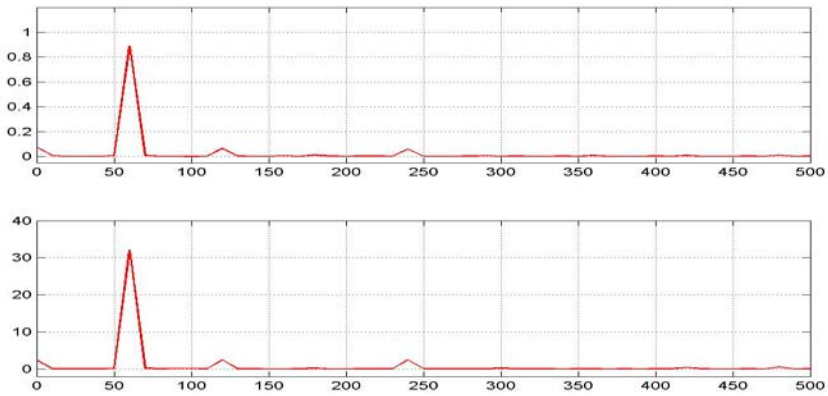


Figure 4.26 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0 and M = 1.5

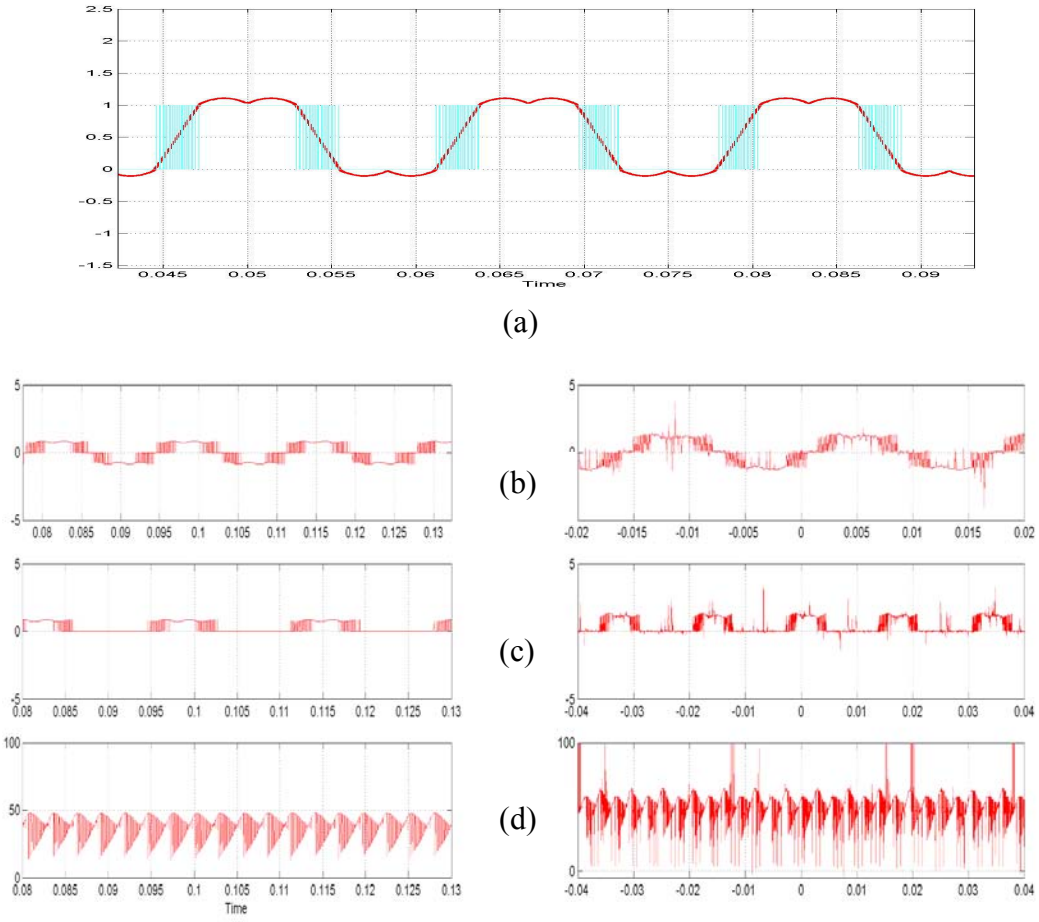


Figure 4.27 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage

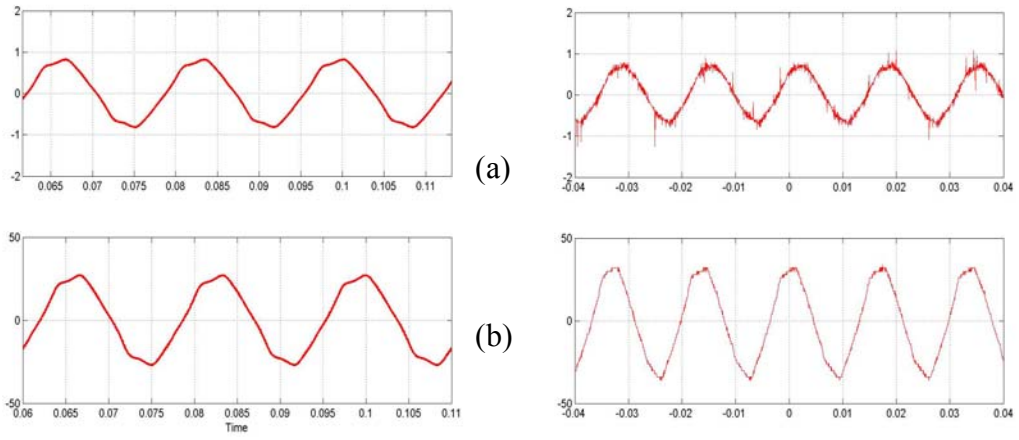


Figure 4.28 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)Phase 'a' Filtered Out put Current and (b) Voltage

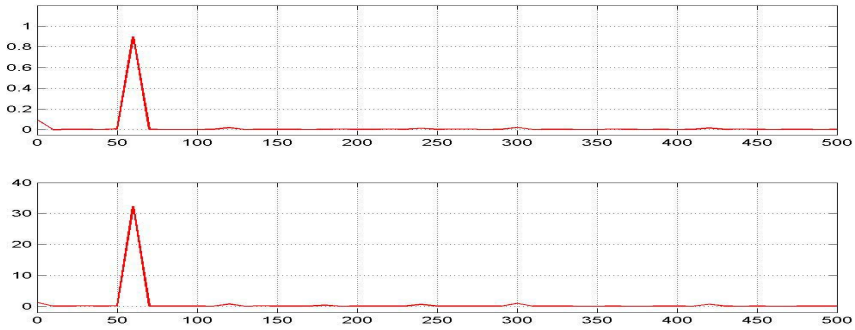
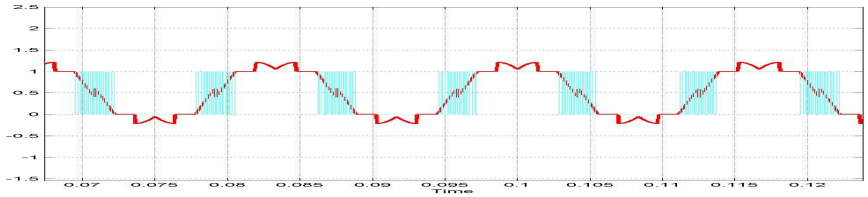
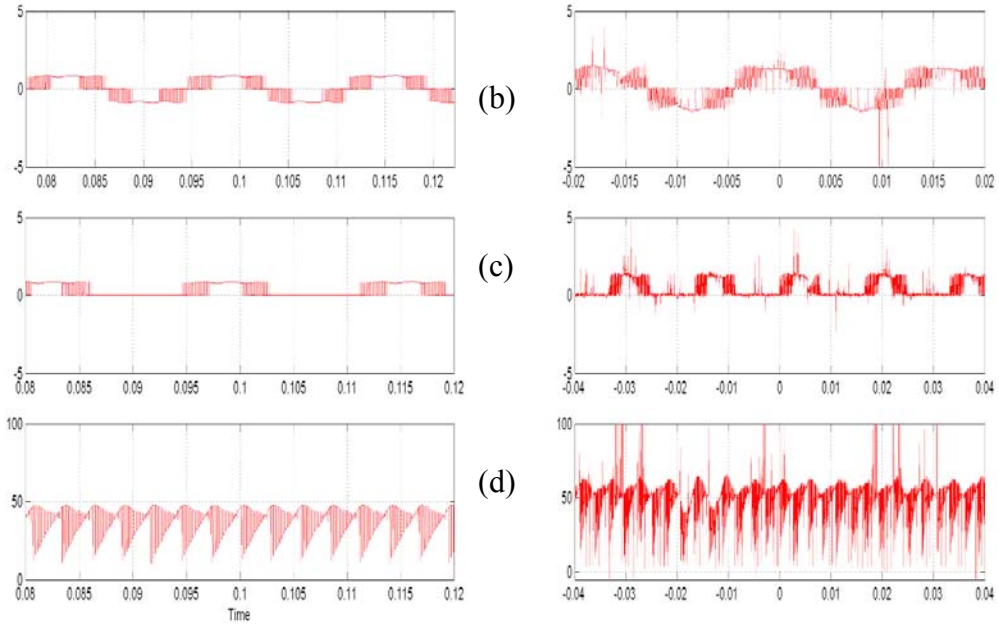


Figure 4.29 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0.5 and M = 1.5

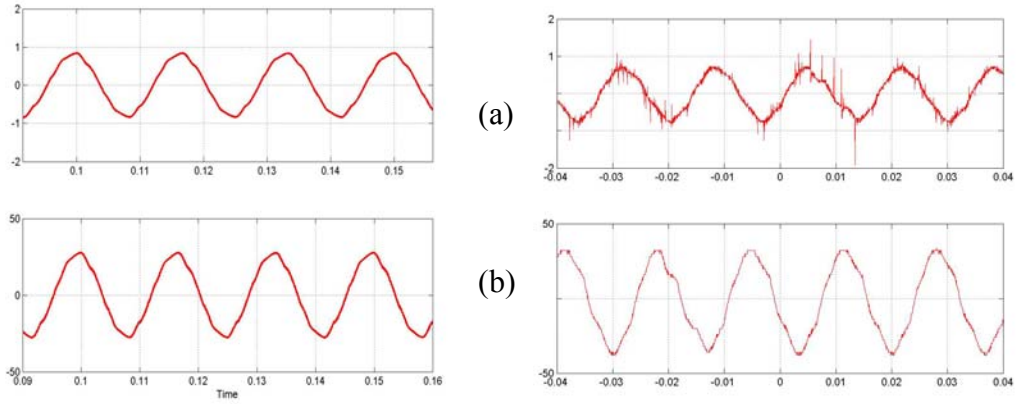


(a)



I Simulation **II. Experiment**

Figure 4.30 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM $\beta = 0.5[1 + SgnCos\ 3(\omega t + \delta)]$, $\delta = 0$ modulation feeding an R-L load of ,$R_L = 30\Omega$,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a)GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.31 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM $\beta = 0.5[1 + SgnCos\ 3(\omega t + \delta)]$, $\delta = 0$ modulation feeding an R-L load of ,$R_L = 30\Omega$,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage

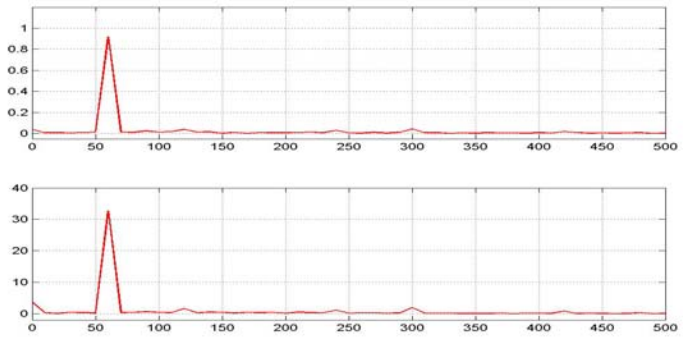
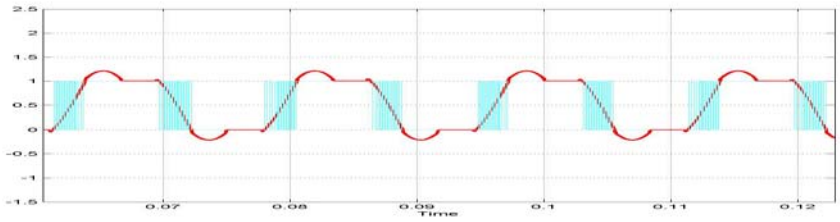
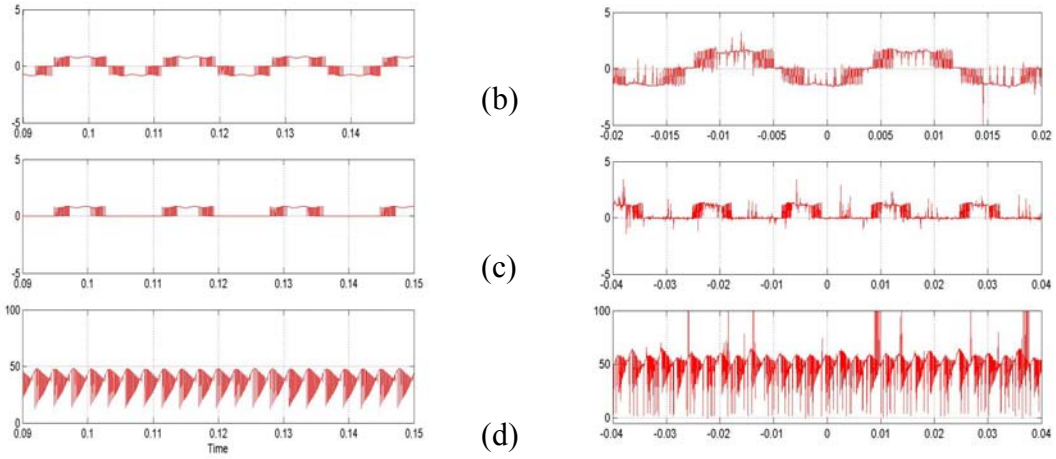


Figure 4.32 FFT of the filtered output voltage and current for the above GDPWM modulating signal $\beta = 0.5$ and M = 1.5



(a)



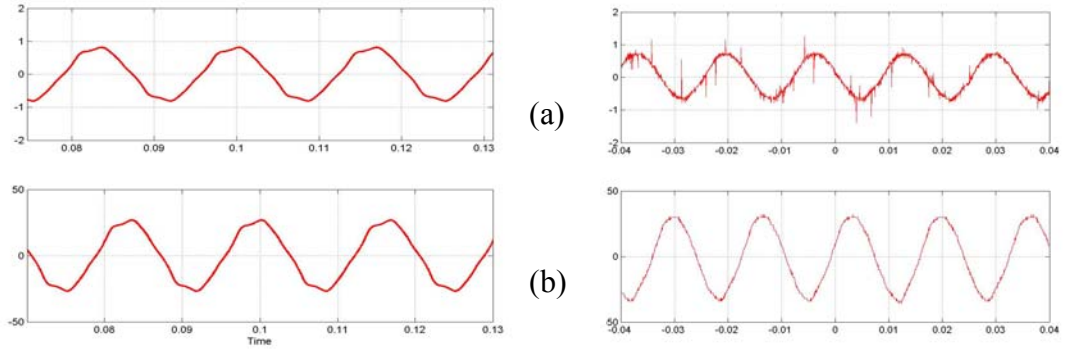
(b)

(c)

(d)

I Simulation **II. Experiment**

Figure 4.33 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ = -30 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.34 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ=-30 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage

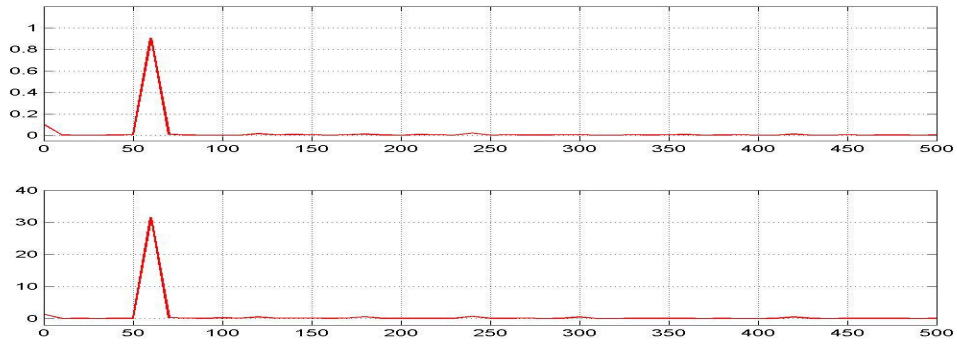
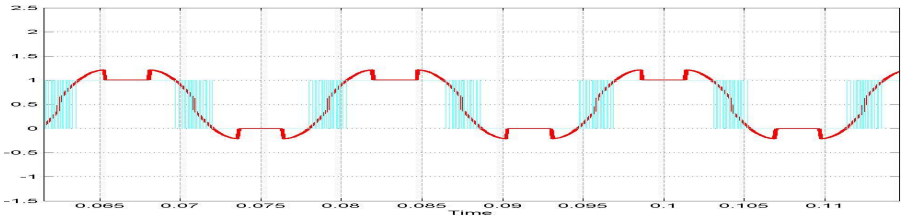
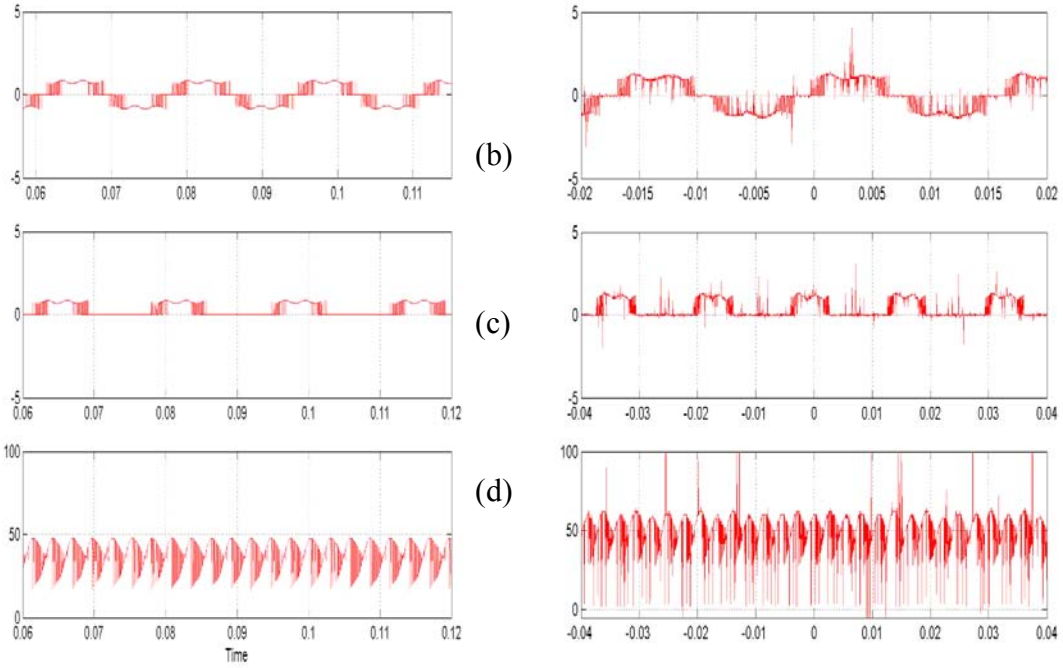


Figure 4.35 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0.5[1 + SgnCos 3(ωt + δ)], δ=-30 and M = 1.5

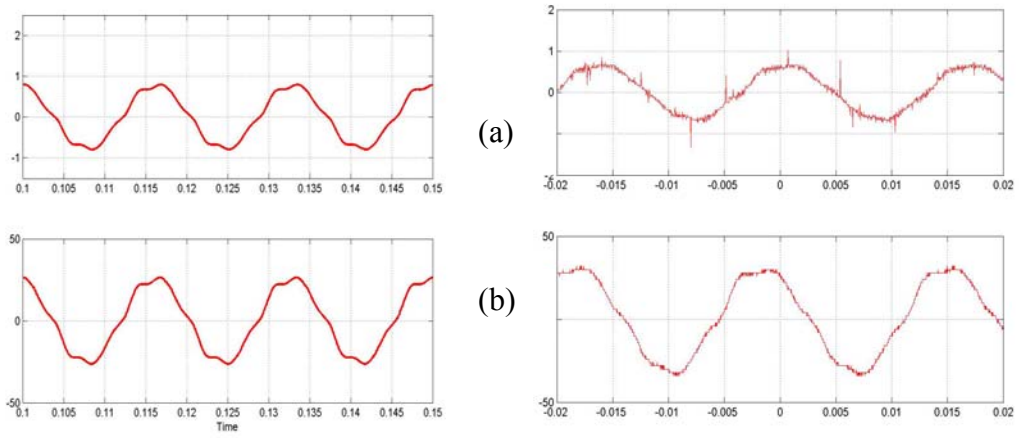


(a)



I Simulation **II. Experiment**

Figure 4.36 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM $\beta = 0.5[1 + SgnCos\ 3(\omega t + \delta)]$, $\delta = -60$ modulation feeding an R-L load of ,$R_L = 30\Omega$,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) GDPWM modulating signal and corresponding VSI switching (b)Unfiltered Phase 'a' Output Current, (c) device switching current and (d) Input voltage



I Simulation **II. Experiment**

Figure 4.37 I & II Simulation and Experimental results respectively for three phase CSI under GDPWM β = 0.5[1 + SgnCos 3(ωt + δ)], δ=-60 modulation feeding an R-L load of ,R_L = 30Ω,L = 4mH at M = 0.96,V_{dc} = 40V, I_{dc} = 1.8A (a) Phase 'a' Filtered Out put Current and (b) Voltage

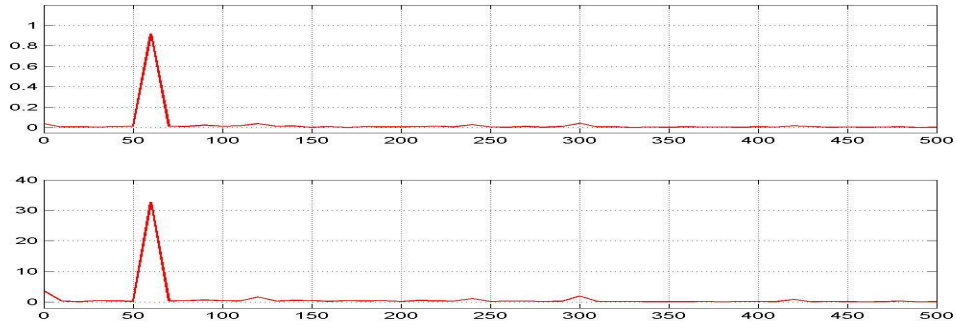


Figure 4.38 FFT of the filtered output voltage and current for the above GDPWM modulating signal β = 0.5[1 + SgnCos 3(ωt + δ)], δ=-60^o and M = 1.5

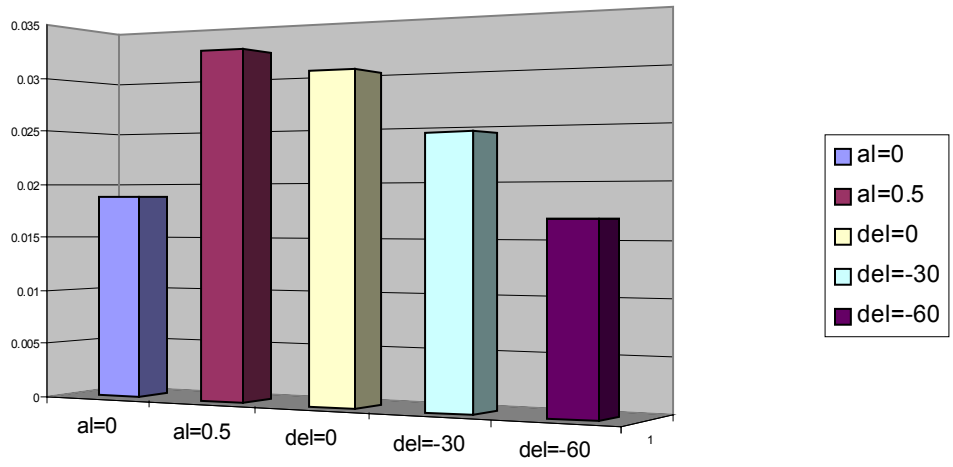


Figure 4.39 (a) Comparison of 3rd harmonic obtained from FFT of output currents for various modulating schemes at 'm'=0.96

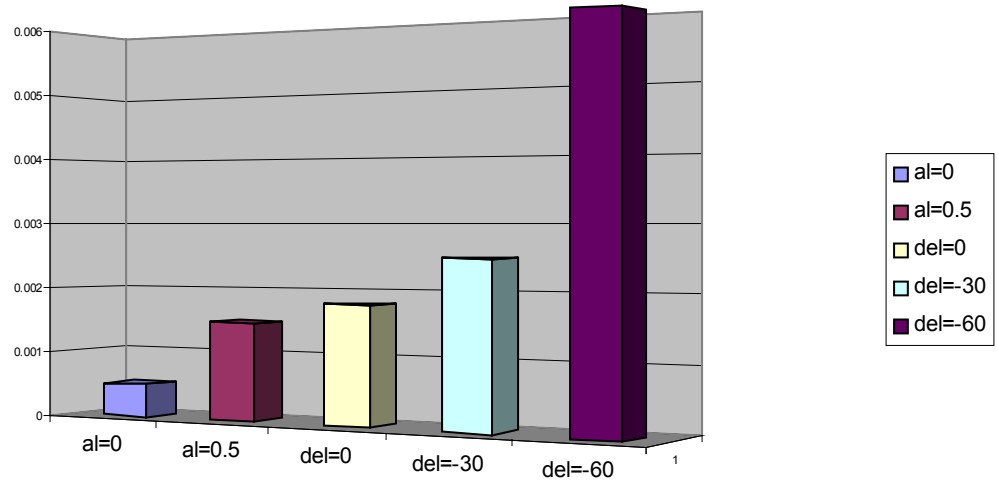


Figure 4.39 (b) Comparison of 5th harmonic obtained from FFT of output currents for various modulating schemes at 'm'=0.96

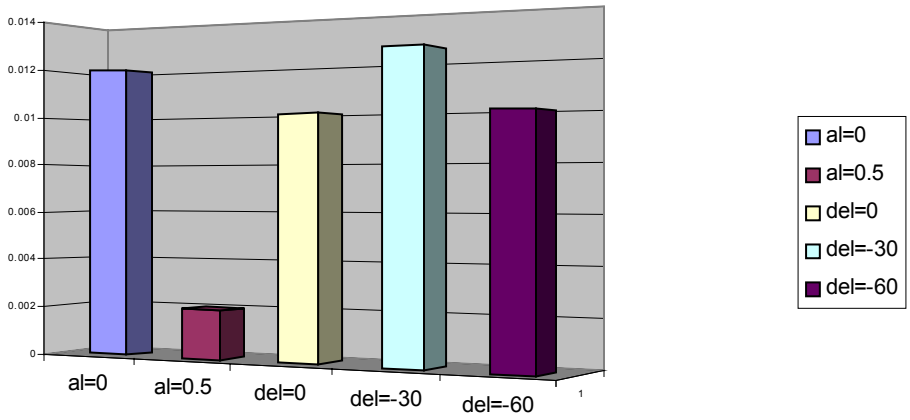


Figure 4.40 (a) Comparison of 3rd harmonic obtained from FFT of output currents for various modulating schemes at over modulation

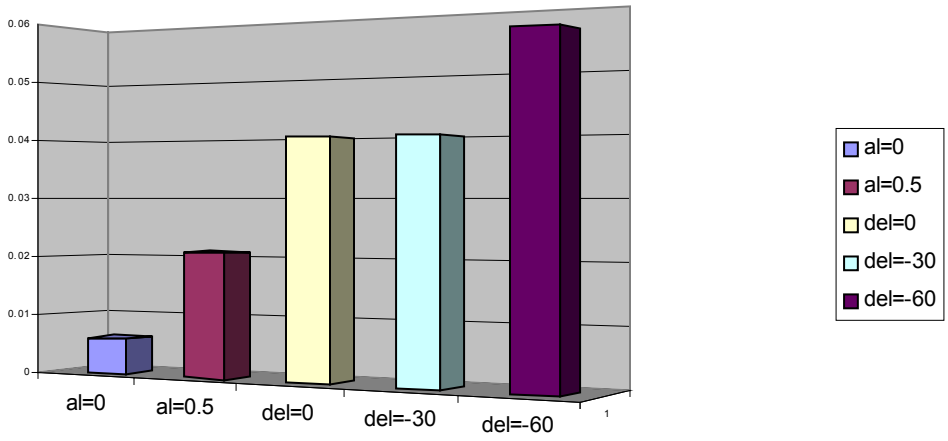


Figure 4.40 (b) Comparison of 5th harmonic obtained from FFT of output currents for various modulating schemes at over modulation

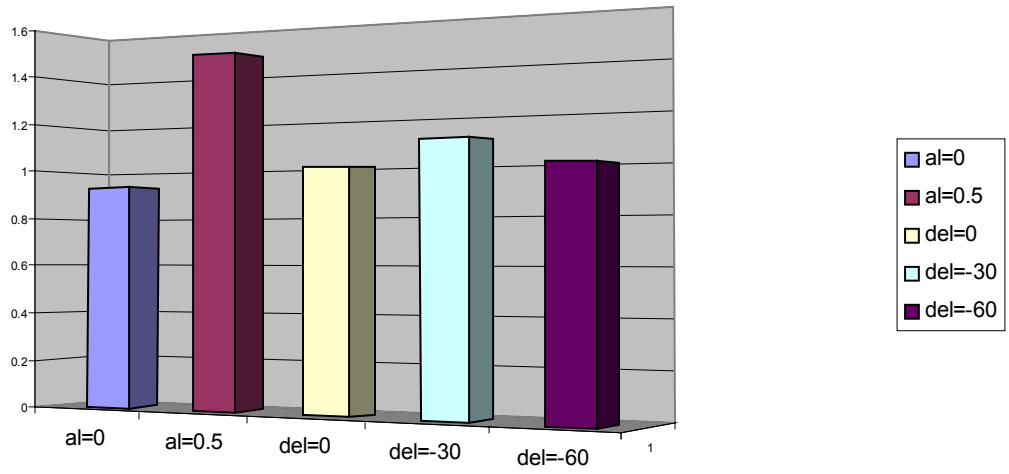


Figure 4.41 (a) Comparison of 3rd harmonic obtained from FFT of output voltages for various modulating schemes at 'm' = 0.96

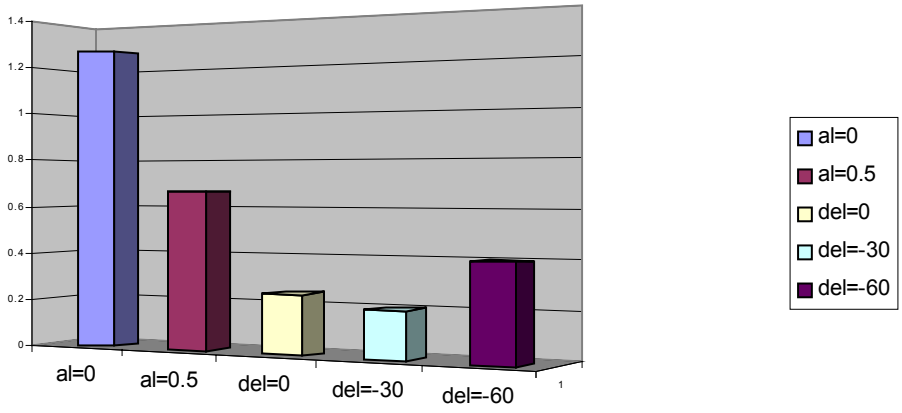


Figure 4.41 (b) Comparison of 5th harmonic obtained from FFT of output voltages for various modulating schemes at 'm' = 0.96

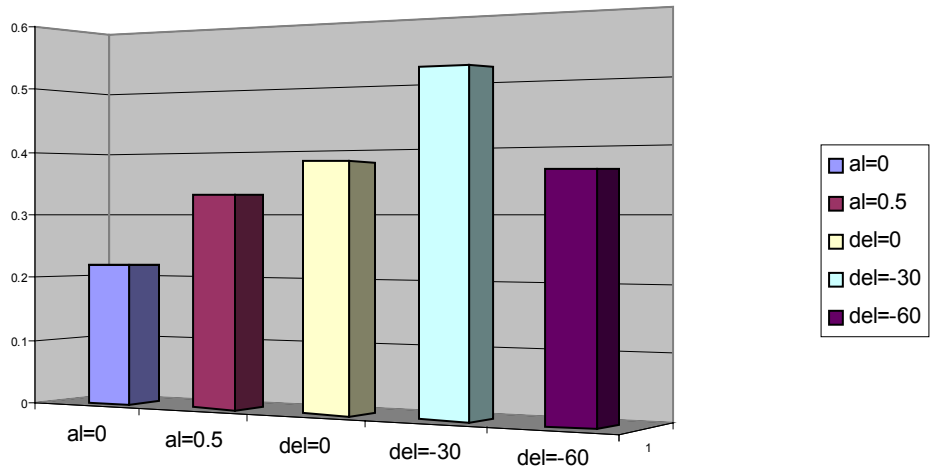


Figure 4.42 (a) Comparison of 3rd harmonic obtained from FFT of output voltages for various modulating schemes at over modulation

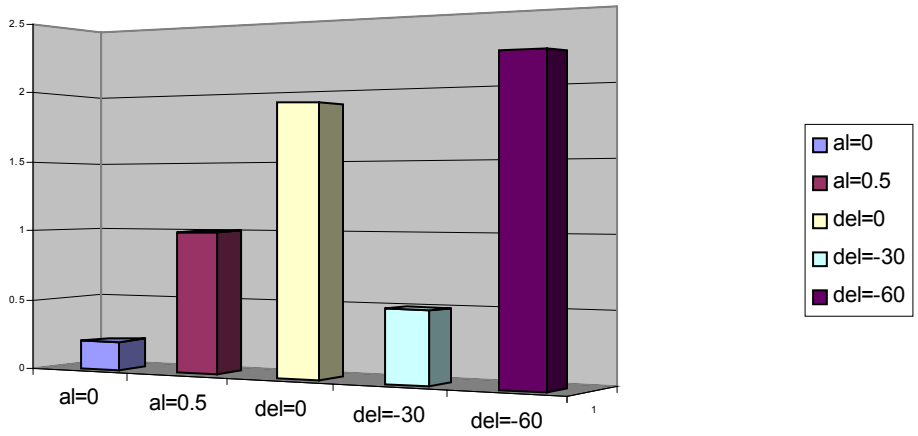


Figure 4.42 (b) Comparison of 5th harmonic obtained from FFT of output voltages for various modulating schemes at over modulation