A NEW CARRIER-BASED DISCONTINUOUS PWM MODULATION METHODOLOGY FOR FOUR-LEG VOLTAGE SOURCE INVERTERS

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ABSTRACT : A new carrier-based discontinuous pulse-width modulation (PWM) scheme anchored on a novel Space Vector modulation methodology is proposed in this paper for four-leg converters. Using a Space Vector definition that includes the zero sequence voltage component and partitioning the feasible sixteen modes into three separate sets, the expressions for the modulation signals for the discontinuous carrier based PWM scheme are set forth. Significantly, the switching devices can be clamped either to the positive or negative rail for 120 degrees under all operating conditions of unbalanced three-phase voltages; ensuring the reduction of switching losses and the effective switching frequency of the inverters. The discontinuous PWM modulation methodology proposed which is shown by experimental results to synthesis desirable balanced or unbalanced three-phase voltage sets complements and further clarifies the results of the 3-dimesional Space Vector Modulation scheme (3-D SVM) for four-leg converters reported in the literature.

I. INTRODUCTION

Stand-alone three-phase power supplies with high waveform quality and performance are increasingly required for critical applications such as military and medical equipment, satellite earth stations, large scale computer systems and for rural electrification schemes in remote locations. In view of the possible imbalances in electrical loads, which are becoming nonlinear, four-leg DC/AC inverters are recommended, especially in applications where the neutrals of the star-connected loads are accessible. Four-leg converters are finding relevance in active power filters and fault-tolerant three-phase rectifiers with capability for load balancing and distortion mitigation. For three phase, four-wire electric distribution systems, four-leg converters are now used in distributed generator systems such as micro-turbines to provide three-phase outputs with neutral connections[1]. Since it is standard procedure to ensure voltage and current regulation or power quality improvement through the use of either carrier-based pulse-width modulation or space vector inverter control schemes, research into the development of the three dimensional space vector modulation (3-D SVM) scheme for four-leg converter structure has made much progress and some experimentally demonstrated algorithms have been reported in pioneering papers [1-4]. This paper makes a novel contribution to the development of the carrier-based generalized discontinuous modulation scheme for the four-leg DC/AC inverters. Through intensive analyses and experimental results, the modulation possibilities opened up are discussed and the relations between the new carrier-based technique and the 3-D space vector modulation scheme in [1] are explicated.

II. CARRIER-BASED DISCONTINUOUS PWM SCHEME

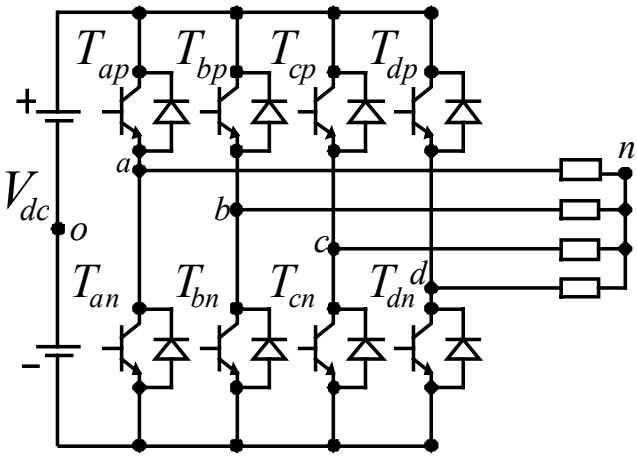


Fig. 1 : Circuit topology of four-leg DC/AC inverter.

The 16 feasible switching modes of the four-leg inverter of Figure 1 are given in Table I [3]. The stationary reference frame qdo voltages of the switching modes are expressed in the complex variable form as ($a = e^{j\beta}$, $\beta = 120°$) :

$$V_{qds} = 2/3(V_{an} + aV_{bn} + a^2V_{cn}), \quad V_o = 1/3(V_{an} + V_{bn} + V_{cn}). \quad (1)$$

Using the phase to reference voltages V_{ao}, V_{bo}, V_{co} and V_{do} for each switching mode, the components of the stationary reference frame V_{qdos} expressed in terms of the switching functions are given as :

$$V_{qs} = 1/6(2S_{ap} - S_{bp} - S_{cp} - 2S_{an} + S_{bn} + S_{cn})V_d,$$
$$V_{ds} = 1/2\sqrt{3}(S_{cp} - S_{bp} - S_{cn} + S_{bn})V_d, \quad (2)$$
$$V_o = 1/6(S_{ap} + S_{bp} + S_{cp} - S_{an} - S_{bn} - S_{cn} - 3S_{dp} + 3S_{dn})V_d + V_{dn}$$

S_{ip} and S_{in} for i =a,b,c,d are the switching functions of top (p) and bottom (n) for the phases. It is evident from Table I that the 16 switching modes can be divided into three broad divisions. A set of modes (1a-6a) in which all the zero sequence voltages are positive and another set (1b-6b) in which all the zero sequence voltages are negative and the third set comprising the null states (7,8,9,10). Modes 7 and 8 are two null states with zero qdo voltages while modes 9 and 10 are modes with zero qd voltages having zero

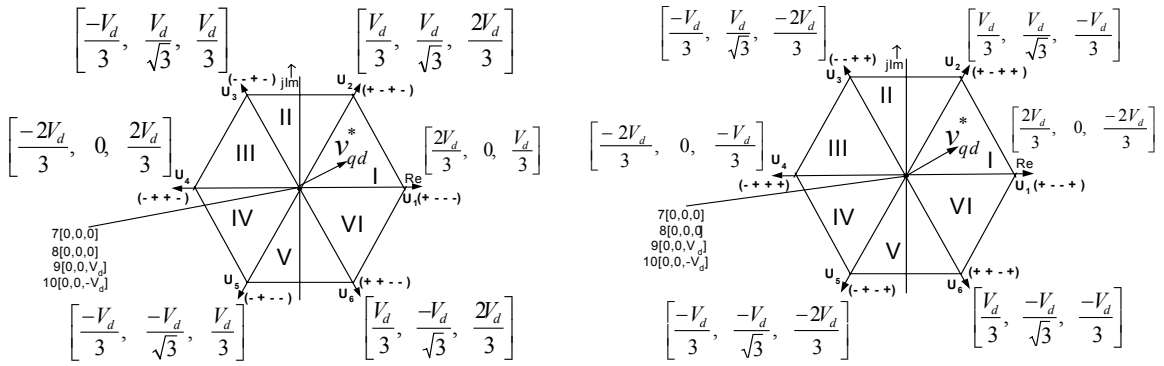


Fig. 2: Space vector of switching modes.(a) Positive zero sequence voltages, (b) negative zero sequence voltages.

sequence voltages of equal but opposite sign. A space vector methodology based on the partitioning of modes as shown in Fig. 2 is set forth in which the null states 7,8,9,10 are common to both. Since the inverters are used in systems with unbalanced and nonlinear loads, the zero sequence voltages for the switching modes must be included in the calculations and are therefore reflected in Fig. 2. In Fig. 2(a), the zero sequence voltages of the active modes are positive while they are negative in Fig. 2(b). In the sequel, Fig. 2(a) will be referred to as the positive (p) sequence space vector set while Fig. 2(b) is the negative (n) space vector set. In classical space vector technique, a reference voltage V_{qd}^* located within the six sectors of the complex space vector in Fig. 2 is approximated instantaneously by time-averaging of four vectors comprising of two adjacent active switching modes and the two null modes 0,7 over the PWM sampling period T_s. However, for the four-leg inverter, the reference voltage is approximated by time-averaging six switching modes comprising of two active modes which are adjacent to the reference V_{qdo}^*, and the four null voltage modes 7,8,9,10. For the synthesis of a voltage reference set, there are four possible two active switching modes which can be used. These are obtained by using (a) two active adjacent states in the positive sequence set, fig. 2(a); (b) two adjacent active states in the negative sequence set, (c) selecting an adjacent active mode from the negative and the other adjacent active set from the positive sequence set and vice visa. The synthesis of a reference voltage in sector I can be explained using Table I and Fig 2. Switching modes 1(a),2(a),7,8,9,10 are required when using the positive sequence set (fig 2(a)) and switching modes 1(b),2(b),7,8,9,10 are used if synthesis is achieved with the negative sequence set (fig 2(b)). The remaining two ways of synthesizing the reference voltage are by using both the positive and negative sequence sets which are the switching modes 1(a),2(b),7,8,9,10 and 1(b),2(a),7,8,9,10. The normalized times the active modes (V_{qdoa} , V_{qdob}) are used are t_a and t_b respectively, t_d is the combined normalized time modes 9 and 10 are applied and the combined times modes 7 and 8 are utilized is t_c . If mode 7 is applied for $(1-\kappa)t_c$, mode 8 for κt_c , mode 9 for γt_d and mode 10 for $(1-\gamma)\, t_d$, then

$t_a + t_b + t_c + t_d = 1$, $0 \le \kappa \le 1$, $0 \le \gamma \le 1$.

Hence, $t_d = (V_o^* - V_{oa}\, t_a - V_{ob}\, t_b)/V_d(2\gamma - 1)$,

$$V_{qdo}^* = V_{qdoa}\, t_a + V_{qdob} t_b + V_{qdo7}(1-\kappa)t_c + V_{qdo8}\kappa t_c + V_{qdo9}\gamma\, t_d + V_{qdo10}(1-\gamma)\, t_d \quad (3)\ .$$

Separating (3) into the three components, the normalized dwell times for the required switching modes in the six sectors are calculated. The resulting equations of the dwell times expressed in terms of line-line reference voltages are given in Table II. Furthermore, the expressions of the normalized time t_d given in (3) are tabulated in Table III.

Table I Switching modes and qdo voltages

S_{ap}	S_{bp}	S_{cp}	S_{dp}	$3V_q^*$	$\sqrt{3}V_d^*$	$3V_o^*$	Mode
0	0	0	0	0	0	0	7
0	0	0	1	0	0	$-3V_d$	10
0	0	1	0	$-V_d$	V_d	V_d	3a
0	0	1	1	$-V_d$	V_d	$-2V_d$	3b
0	1	0	0	$-V_d$	$-V_d$	V_d	5a
0	1	0	1	$-V_d$	$-V_d$	$-2V_d$	5b
0	1	1	0	$-2V_d$	0	$2V_d$	4a
0	1	1	1	$-2V_d$	0	$-V_d$	4b
1	0	0	0	$2V_d$	0	V_d	1a
1	0	0	1	$2V_d$	0	$-2V_d$	1b
1	0	1	0	V_d	V_d	$2V_d$	2a
1	0	1	1	V_d	V_d	$-V_d$	2b
1	1	0	0	V_d	$-V_d$	$2V_d$	6a
1	1	0	1	V_d	$-V_d$	$-V_d$	6b
1	1	1	0	0	0	$3V_d$	9
1	1	1	1	0	0	0	8

Table II : Dwell times of the active devices.

Sect	1	2	3	4	5	6
$\mathbf{V_d t_a}$	V_{ac}	V_{ab}	V_{cb}	V_{ca}	V_{ba}	V_{bc}
$\mathbf{V_d t_b}$	V_{cb}	V_{ca}	V_{ba}	V_{bc}	V_{ac}	V_{ab}

III. SYNTHESIS OF DISCONTINUOUS PWM MODULATION

The expressions for the discontinuous modulation signals for the devices are determined by averaging their existence

Table III : Value of t_d for all four active switching mode combinations

Sector	I	II	III	IV	V	VI
$t_{d(p)}$	$V_{bdd}\chi$	$V_{bdd}\chi$	$V_{add}\chi$	$V_{add}\chi$	$V_{cdd}\chi$	$V_{cdd}\chi$
$t_{d(n)}$	$V_{cdd}\chi$	$V_{cdd}\chi$	$V_{cdd}\chi$	$V_{bdd}\chi$	$V_{bdd}\chi$	$V_{add}\chi$
$t_{d(I)}$	$V_{cdd}\chi$	$(V_{bdn} + V_{cdn} - V_{adn} - V_{ddn})\chi$	$V_{bdd}\chi$	$(V_{adn} + V_{bdn} - V_{cdn} - V_{ddn})\chi$	$V_{add}\chi$	$(V_{cdn} + V_{adn} - V_{bdn} - V_{ddn})\chi$
$t_{d(II)}$	$(V_{adn} + V_{bdn} - V_{cdn} - V_{ddn})\chi$	$V_{add}\chi$	$(V_{cdn} + V_{adn} - V_{bdn} - V_{ddn})\chi$	$V_{cdd}\chi$	$(V_{bdn} + V_{cdn} - V_{adn} - V_{ddn})\chi$	$V_{bdd}\chi$

$V_{idn} = V_{in}/V_d$, i = a,b,c, d, $V_{zdd} = (V_{zd} - V_{dn})/V_d$, z = a,b, c and $\chi = 1/(2\gamma - 1)$

Table IV : Normalized times of top three devices (a,b,c) and t_d of the top device in the fourth leg

Sector	I	II	III	IV	V	VI
Z_{ap}	$t_a + t_b + t_9 + t_8$	$t_a + t_9 + t_8$	$t_9 + t_8$	$t_9 + t_8$	$t_b + t_9 + t_8$	$t_a + t_b + t_9 + t_8$
Z_{bp}	$t_9 + t_8$	$t_9 + t_8$	$t_b + t_9 + t_8$	$t_a + t_b + t_9 + t_8$	$t_a + t_b + t_9 + t_8$	$t_a + t_9 + t_8$
Z_{cp}	$t_b + t_9 + t_8$	$t_a + t_b + t_9 + t_8$	$t_a + t_b + t_9 + t_8$	$t_a + t_9 + t_8$	$t_9 + t_8$	$t_9 + t_8$
$Z_{dp(p)}$	$t_{10} + t_8$	$t_{10} + t_8$	$t_{10} + t_8$	$t_{10} + t_8$	$t_{10} + t_8$	$t_{10} + t_8$
$Z_{dp(n)}$	$t_a + t_b + t_{10} + t_8$	$t_a + t_b + t_{10} + t_8$	$t_a + t_b + t_{10} + t_8$	$t_a + t_b + t_{10} + t_8$	$t_a + t_b + t_{10} + t_8$	$t_a + t_b + t_{10} + t_8$
$Z_{dp(I)}$	$t_b + t_{10} + t_8$	$t_b + t_{10} + t_8$	$t_b + t_{10} + t_8$	$t_b + t_{10} + t_8$	$t_b + t_{10} + t_8$	$t_b + t_{10} + t_8$
$Z_{dp(II)}$	$t_a + t_{10} + t_8$	$t_a + t_{10} + t_8$	$t_a + t_{10} + t_8$	$t_a + t_{10} + t_8$	$t_a + t_{10} + t_8$	$t_a + t_{10} + t_8$

functions (such as those in Fig. 3) in all the sectors in the four possible switching mode combinations. It is seen from Fig. 3 that the average of an existence function is equal to the sum of the normalized times each device is turned on to realize a reference voltage set [5]. Based on Table I, the total time each top device is turned on for the six sectors are given in Table IV. Note that there are four possible expressions for the time t_d reflecting the four combinations of switching modes to synthesize the reference voltage set.

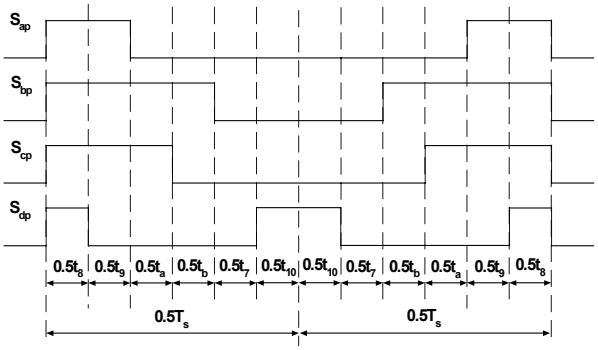


Figure 3 : Existence function of the four leg converter in sector IV

Expressed in terms of the reference phase or line voltages using Tables II and III, the equations for the modulation signals for the top devices are shown in Table V. however, it is noted that the expressions for the modulation signal of the top devices in phases a,b,c are the same for the four switching mode combinations; but the expressions for the modulation signals for phase d and the normalized time t_d are different. In Tables III and V, $M_{dp}(p)$ and $t_d(p)$, respectively, are the expressions for the top device d-phase modulation signal and time for the positive sequence space vector combination set while the corresponding expressions for the negative sequence space vector combination set are $M_{dp}(n)$ and $t_d(n)$, respectively. The corresponding expressions for the modulation signals and times of the other two combinations are $M_{dp}(I)$ and $t_d(I)$, $M_{dp}(II)$ and $t_d(II)$; respectively. These normalized modulation signals for the devices are compared with a high frequency triangular carrier waveform ranging between unity and zero and the intersections define the device switching instants. A study of the switching combinations for all the four switching mode combinations in each sector reveals that the devices connected to phases a, b, c are clamped to the dc rail only when γ and κ take values of unity or zero and $\gamma = \kappa$. In general, the value of γ [1,0] is selected to ensure that t_d and t_c are always positive. When $\kappa = 1 - \gamma$, the d – phase device alone is clamped to the dc rail. Since switching devices connected to phases a, b, c carry most of the load currents; clamping these leads to the highest reduction of switching loss - condition $\gamma = \kappa$ appears to be the optimum selection. It is noted that the selection of γ [1,0], κ[1,0] corresponding to the situation where only two null states are used in the synthesis – one with zero qdo

TABLE V : Modulation signals for the top devices

Sector	M_{ap}	M_{bp}	M_{cp}	$M_{dp}(p)$	$M_{dp}(n)$	$M_{dp(I)}$	$M_{dp\ (II)}$
I	$V_{abn}+\gamma\mathbf{t}_d + \kappa(1-V_{abn}- t_d)$	$\gamma t_d + \kappa(1-V_{abn} - t_d)$	$\kappa(1-V_{abn}-t_d)+ V_{cbn}+\gamma\mathbf{t}_d$	$\kappa(1-V_{abn}- t_d)+(1-\gamma)\mathbf{t}_d$	$V_{abn}+\kappa(1-V_{abn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{cbn}+\kappa(1-V_{abn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{acn}+\kappa(1-V_{abn}- t_d) + (1-\gamma)\mathbf{t}_d$
II	$V_{abn}+\gamma t_d+ \kappa(1-V_{cbn} - t_d)$	$\gamma t_d+ \kappa(1-V_{cbn} - t_d)$	$V_{cbn}+\gamma t_d+\kappa(1- V_{cbn}-t_d)$	$\kappa(1-V_{cbn}- t_d)+(1-\gamma)\mathbf{t}_d$	$V_{cbn}+\kappa(1-V_{cbn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{can}+\kappa(1-V_{cbn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{abn}+\kappa(1-V_{cbn}- t_d) + (1-\gamma)\mathbf{t}_d$
III	$\gamma t_d +\kappa(1-V_{can} - t_d)$	$V_{ban}+\gamma\mathbf{t}_d + \kappa(1-V_{can} - t_d)$	$V_{can}+\gamma\mathbf{t}_d +\kappa(1- V_{can} - t_d)$	$\kappa(1-V_{can} - t_d)+(1-\gamma)\mathbf{t}_d$	$V_{can}+\kappa(1-V_{can}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{ban}+\kappa(1-V_{can}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{cbn}+\kappa(1-V_{can}- t_d) + (1-\gamma)\mathbf{t}_d$
IV	$\gamma t_d +\kappa(1-V_{ban} - t_d)$	$V_{ban}+\gamma t_d+\kappa(1 -V_{ban} - t_d)$	$V_{can}+\gamma t_d +\kappa(1- V_{ban} - t_d)$	$\kappa(1-V_{ban} - t_d)+(1-\gamma)\mathbf{t}_d$	$V_{ban}+\kappa(1-V_{ban}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{bcn}+\kappa(1-V_{ban}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{can}+\kappa(1-V_{ban}- t_d) + (1-\gamma)\mathbf{t}_d$
V	$V_{acn}+\gamma\mathbf{t}_d + \kappa (1-V_{bcn} - t_d)$	$V_{bcn}+\gamma\mathbf{t}_d + \kappa(1-V_{bcn} - t_d)$	$\gamma\mathbf{t}_d +\kappa(1-V_{bcn} - t_d)$	$\kappa(1-V_{bcn} - t_d)+(1-\gamma)\mathbf{t}_d$	$V_{bcn}+\kappa(1-V_{bcn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{acn}+\kappa(1-V_{bcn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{ban}+\kappa(1-V_{bcn}- t_d) + (1-\gamma)\mathbf{t}_d$
VI	$V_{acn}+\gamma\mathbf{t}_d + \kappa(1-V_{acn} - t_d)$	$V_{bcn}+\gamma\mathbf{t}_d+\kappa(1-V_{acn}- t_d)$	$\gamma\mathbf{t}_d +\kappa(1-V_{acn} - t_d)$	$\kappa(1-V_{acn} - t_d)+\mathbf{t}_d (1-\gamma)$	$V_{acn}+\kappa(1-V_{acn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{abn}+\kappa(1-V_{acn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{bcn}+\kappa(1-V_{acn}- t_d) + (1-\gamma)\mathbf{t}_d$

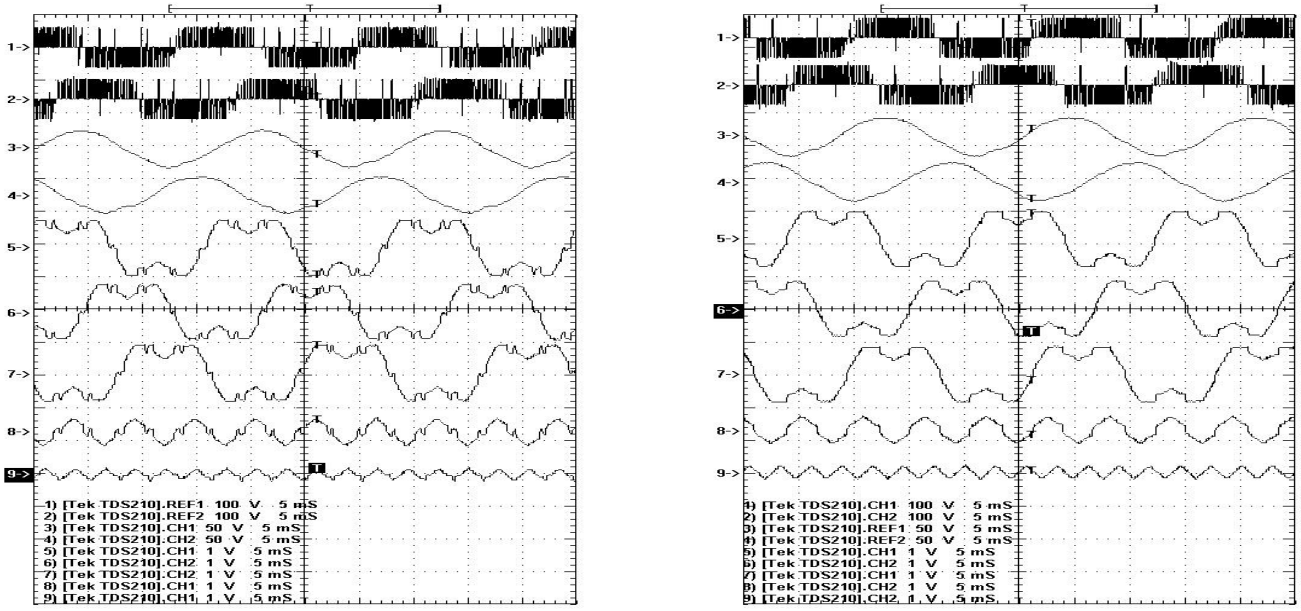
$\chi = 1/(2\gamma -1)$, $V_{ijn} = V_{ij}/V_d$, $V_{in} = V_{in}/ V_d$, i, j = a, b,c and $i \neq j$

value and another with zero qd but non-zero negative sequence voltage values is akin to the Class II sequencing 3-D SVM scheme set forth in [1]; which is shown to be the best compromise choice between switching losses and harmonic contents. An infinite number of possibilities results if γ , κ take fractional values – in which more than two of the members of the set of null states are utilized in the voltage synthesis – with loss of switching device clamping to either the positive of negative rails.

The synthesis of any reference voltage is now set forth: Given the instantaneous unbalanced three phase reference voltage set (equivalently, the qdo voltages in the stationary reference frame) the sector in Fig. 2 where it resides is determined. From table III, and for a given value of γ (to assure positive value of t_d – positivity of time) the times t_d for the four combinations are calculated and an appropriate switching combination that ensures that $t_c \geq 0$ is selected. Since there may be more than one combination that meet the time positivity requirement, other constraints can be used to decide which switching combination is selected such as the combination with the minimum or maximum time t_c. Then Table V is used to determine the modulation signals for the top devices (equivalently those of the lower devices as they are complementary to the top devices).

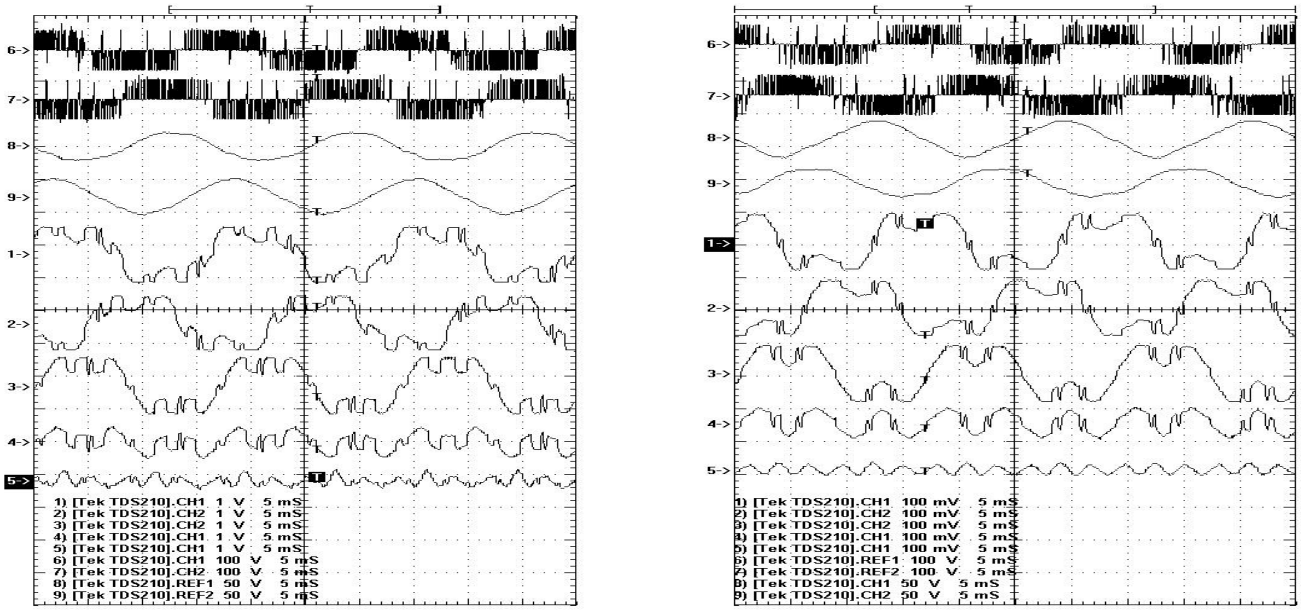
IV. EXPERIMENTAL RESULTS

The new carrier-based discontinuous PWM modulation scheme is implemented by means of a floating-point 40-MHz DSP TMS320LF2407 board to synthesize three-phase balanced and unbalanced phase voltages to a wye-connected three-phase load. While the maximum current and voltage of the four-leg converter used is 14A and 350V respectively, the DC voltage applied for the experiment is 60V and the phase of each of the three-phase load is comprised of a resistance of 40 Ohms shunted with a filter with an inductance of 14 mH and a capacitor of 30 μF. Figure 4 shows the generated balanced three-phase voltage waveforms and the corresponding discontinuous modulation signals for the four top devices required for the synthesis using the switching combinations that have either the instantaneous minimum or maximum value of time t_d respectively. In Figures 5-6 a mild and a severe unbalanced voltages are synthesized. These figures show types of modulation signals needed for the synthesis of unbalanced voltages and the unevenness in the clamping of the devices to the dc rails. It would appear from these figures that at lower (higher) modulation index, voltage synthesis based on the selection of switching mode combinations that give maximum (minimum) t_d yield the smoother modulation signals and hence less distortion in the synthesized voltage waveforms. Finally, Fig. 7 shows the discontinuous modulation signals for generating the three-phase balanced voltages with a modulation index that is less than one. Figure 7(a) corresponds to the Class II(c) symmetrically aligned sequencing scheme of the proposed 3-D SVM in [1]. It is salutary to observe that 7(a) and 7(b) are respectively similar to the discontinuous modulation waveforms DPWM1 and DPWM3 of the three leg voltage source converters [6]. The generalized discontinuous PWM modulation (GDPWM) for the two level converters (DPWM1 and DPWM3 are members) by virtue of the injection of zero sequence signals to the sinusoidal PWM signals extends the PWM linearity range. So it is that the proposed modulation, especially for the switching mode combination satisfying the condition of minimum time t_d will improve the linearity range of the four-leg converter by increasing the voltage gain in the over-modulation region. For the case in which the three load voltages are balanced, the periods for which the devices in the four-leg converter are clamped in each load phase are the same (120 degrees



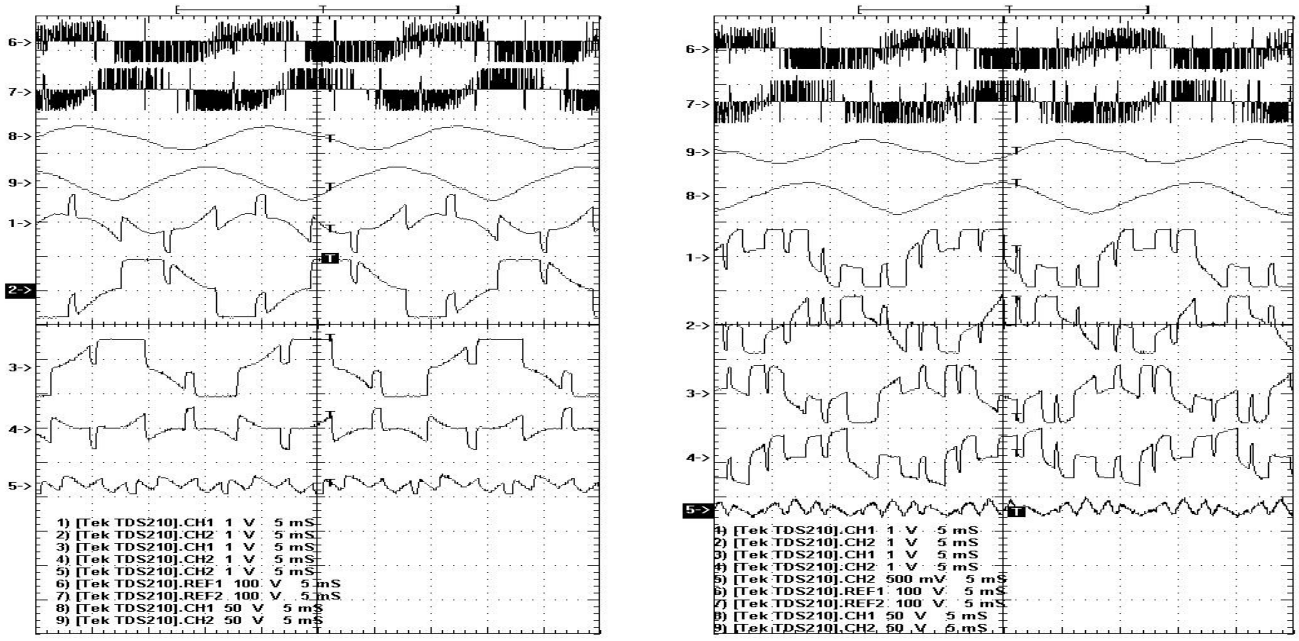
(a) $t_d = t_{dmax}$ (b) $t_d = t_{dmin}$

Figure 4: Experimental results : Generation of balanced three-phase voltages using discontinuous modulation scheme. V_{an} = 30 cos (377t), V_{bn} =30 cos (377t - 2π/3), V_{cn} =30 cos (377t + 2π/3) V_d = 60V. (1-2) Line voltages V_{ad}, V_{cd} , (3-4) Filtered line voltages V_{ad}, V_{cd} , (5-8) Modulating signals of the top four devices, S_{ap} , S_{bp} , S_{cp}, S_{dp} , (9) t_d



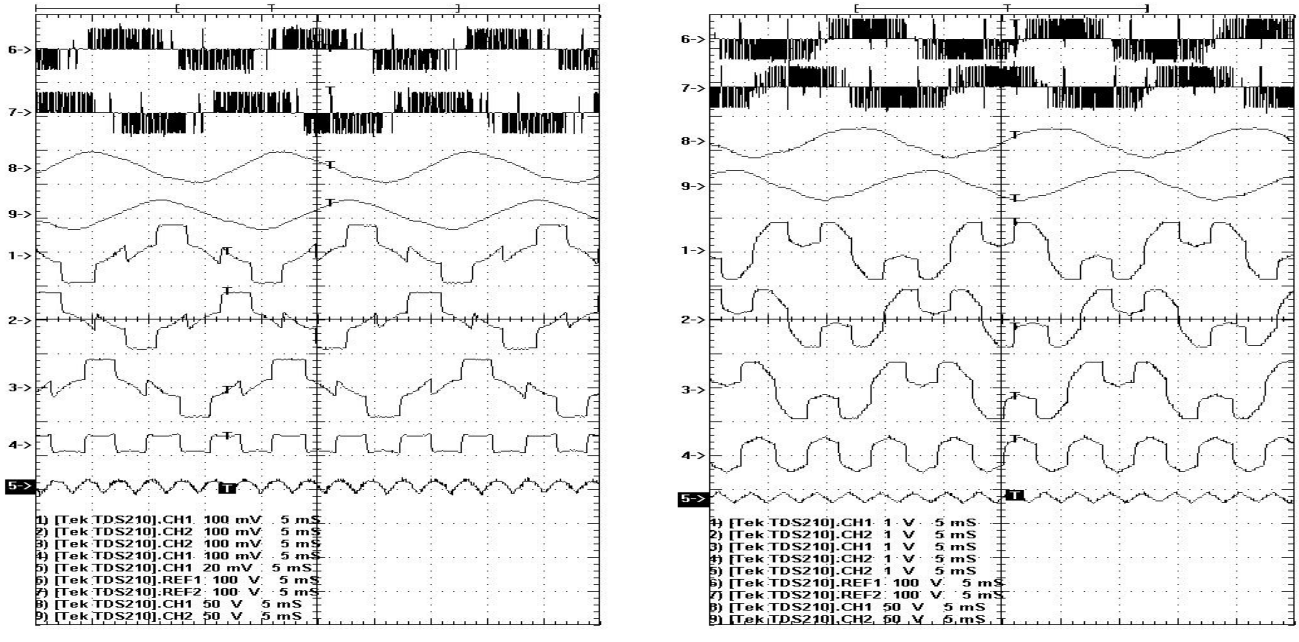
(a) $t_d = t_{dmax}$ (b) $t_d = t_{dmin}$

Figure 5: Experimental results : Generation of unbalanced three-phase voltages using discontinuous modulation scheme. V_{an} = 30 cos (377t), V_{bn} =30cos (377t - 2π/3), V_{cn} = 22.5 cos (377t + 2π/3) V_d = 60V. (6-7) Line voltages V_{ad}, V_{cd} , (3-4) Filtered line voltages V_{ad}, V_{cd} , (1-4) Modulating signals of the top four devices, S_{ap} , S_{bp} , S_{cp}, S_{dp} , (5) t_d



(a) $t_d = t_{dmax}$ (b) $t_d = t_{dmin}$

Figure 6: Experimental results : Generation of unbalanced three-phase voltages using discontinuous modulation scheme. V_{an} = 10 cos (377t), V_{bn} =30cos (377t - 2π/3), V_{cn} = 30 cos (377t + π) V_d = 60V. (6-7) Line voltages V_{ad}, V_{cd} , (3-4) Filtered line voltages V_{ad}, V_{cd} , (1-4) Modulating signals of the top four devices, S_{ap}, S_{bp} , S_{cp}, S_{dp} , (5) t_d



(a) $t_d = t_{dmax}$ (b) $t_d = t_{dmin}$

Figure 7: Experimental results : Generation of balanced three-phase voltages using discontinuous modulation scheme. V_{an} = 22.5 cos (377t), V_{bn} =22.5cos (377t - 2π/3), V_{cn} = 22.5 cos (377t + 2π/3) V_d = 60V. (6-7) Line voltages V_{ad}, V_{cd} , (3-4) Filtered line voltages V_{ad}, V_{cd} , (1-4) Modulating signals of the top four devices, S_{ap}, S_{bp} , S_{cp} , S_{dp} , (5) t_d

cycle); however for the situation in which the load phase voltages are unbalanced, there is a total of 360 degree clamping for the three-phases which are unevenly distributed in the load phases.

VI. CONCLUSIONS

The carrier-based discontinuous modulation scheme for the four-leg converter has been proposed in this paper for the first time using an expanded definition of the space vector methodology that includes the zero sequence voltages of the switching converter modes. The twelve active modes are portioned into two sets - those with the positive zero sequence voltages constituting what is the called the positive sequence set and the second one comprising of the switching modes with negative zero sequence voltages. The remaining set of four modes with zero qd voltages constitute the null states. Using the positive and negative sequence sets and their combinations, the timings for the adjacent switching modes required to synthesize a reference voltage in all the six sectors are calculated from which the expressions for the modulation functions for the top switching devices are determined. It is shown that the devices connected to phases a, b, c are clamped to the dc rail only when γ and κ take values of unity or zero and $\gamma = \kappa$. In general, the value of γ [1,0] is selected to ensure that t_d is always positive. When $\kappa = 1 - \gamma$, the d – phase device alone is clamped to the dc rail. For the case in which the three load voltages are balanced, the period for which the devices are clamped in each load phase are seen to be the same (120 degrees per cycle) ; however; for the situation in which the load phase voltages are unbalanced, there is a total of 360 degrees clamping for the three-phase but are unevenly distributed in the load phases. Since switching devices connected to phases a, b, c carry most of the load currents, clamping these phases leads to the highest reduction of switching loss : hence the condition $\gamma = \kappa$ appears to be the optimum selection [1].

In general, there are four possible expressions for the modulation signals for each device; however it is shown in the body of the paper that for any reference phase voltages, only few of them are tenable at every instant since the positivity condition of the switching times may not always be satisfied. It would appear that the switching mode combination that yields the minimum instantaneous time t_d gives the highest linearity range when converter operates in the over-modulation region.

The carrier-based discontinuous modulation methodology set forth in this paper overcomes some of the difficulties in the understanding and use of the 3-D SVM modulation for the four-leg converters such as the need for exhaustive search for switching combinations, selection of the switching vectors and the sequencing of the switching vectors [1]. The possibility of generating an infinite number of discontinuous modulation signals is revealed in the analysis presented in this paper in a rather transparent and mathematically provable fashion, showing limitations and possible exploratory parameters [γ , κ] to meet application measures such as harmonic content, switching loss requirements. Over-modulation voltage gain is enhanced; thanks to the selection of appropriate switching mode combinations to synthesize the desired reference balanced or unbalanced voltages.

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