CONCISE MODULATION STRATEGIES FOR FOUR-LEG VOLTAGE SOURCE INVERTERS

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ABSTRACT : The continuous and discontinuous pulse-width modulation (PWM) schemes and a novel Space Vector modulation methodology are proposed in this paper for four-leg DC-AC inverters. Using a Space Vector definition that includes the zero sequence voltage component and partitioning the feasible sixteen modes into two separate sets – one set having zero sequence voltages with positive magnitudes and the other set with the zero sequence voltages with negative magnitudes – the novel Space vector implementation technique is determined as also the discontinuous carrier based PWM scheme. For the continuous carrier based PWM scheme, the indeterminate defining output voltage equations expressed in terms of the existence functions of the switching devices are solved using an optimization technique. The modulation schemes determined are shown by experimental results to synthesis any desirable balanced or unbalanced three-phase voltage sets when operating in the linear modulation region.

I. INTRODUCTION

Stand-alone three-phase power supplies with high waveform quality and performance are increasingly required for critical applications such as military and medical equipment, satellite earth station, large scale computer systems, distributed power systems, and for rural electrification schemes in remote locations. In view of the possible imbalances in the loads which are becoming nonlinear, four-leg DC/AC inverters are recommended, especially in applications where the neutrals of the loads are accessible. In certain applications, front-end three-phase diode rectifiers fed from a generator or alternative energy sources, such as solar systems, fuel-cells or battery banks provides the input DC source to the four-legged inverter. It is now standard procedure to ensure voltage, current regulation or power quality improvement (mitigation of harmonics, etc.) through either pulse-width modulation or space vector inverter control schemes. A space vector modulation scheme fashioned after the classical

qdo stationary reference frame space vector methodology has been proposed and shown by computer simulations to be capable of balancing load voltages and improve current quality [1-3,6]. In view of the alleged inability of the well- known 3x3 abc-qdo stationary reference transformation to reflect the fourth degree of freedom that the four inverter legs provide in the modeling of the four-leg inverters, a rather complicated 4x4 or quad stationary reference frame transformation has been proposed for inverter modeling which, with synchronous reference frame controllers, is used to experimentally showcase the possibility of voltage regulation under nonlinear or unbalanced three-phase load conditions [4-5].

The paper contributes to the development of both the space vector and carrier-based modulation schemes for the four-leg DC/AC inverters. The definition of the problem permits the use of the classical qdo transformations; however, unlike the classical space vector where the zero sequence voltages are ignored, they are used here for calculating the turn-on times of the devices. With the expressions for the times the devices are turned on for a desired voltage set, the expressions for the discontinuous modulation signals for the devices are determined. Various discontinuous modulation schemes for three-phase inverters have been investigated [7-10]. Furthermore, using the inverter voltage equations expressed in terms of the existence functions of the devices and an optimization methodology based on Moore-Penrose inverse, the expressions for the modulating signals constituting the carrier-based continuous PWM for all the eight switching devices are explicitly determined. The methodologies proposed for determining the carrier-based and space vector modulation set forth are considered to be novel and are extendable for the determination of modulation schemes for other current or voltage source converters including the multi-level and converters with reduced component counts (minimalist converters).

II. CONTINUOUS PWM MODULATION

Fig. 1 shows the circuit topology of the four-leg voltage source DC/AC inverter in which the fourth leg, in general is connected through an impedance to the neutral of the three-phase load which could be unbalanced or/and nonlinear. The turn-on and turn-off sequences of a switching transistor are represented by an existence function which has a value of unity when it is turned on and becomes zero when it is off. In general, an existence function of a two-level converter is represented by $\mathbf{S_{ij}}$, i = a,b,c, and j = p, n where i represents the load phase to which the device is connected, and j signifies top (p) and bottom (n) device of the inverter leg. Hence, $\mathbf{S_{ap}}$, $\mathbf{S_{an}}$ which take values of zero or unity, are respectively the existence functions of the top device ($\mathbf{T_{ap}}$) and bottom device ($\mathbf{T_{an}}$) of the inverter leg which is connected to phase 'a' load [11,13]. The load voltage equations expressed in terms of the existence functions and input DC voltage V_d are given as :

$$0.5V_d\ (S_{ap} - S_{an}) = V_{an} + V_{no}\ ,\ 0.5V_d\ (S_{bp} - S_{bn}) = V_{bn} + V_{no}$$

$$0.5V_d\ (S_{cp} - S_{cn}) = V_{cn} + V_{no}\ ,\ 0.5V_d\ (S_{dp} - S_{dn}) = V_{dn} + V_{no} \qquad (1)$$

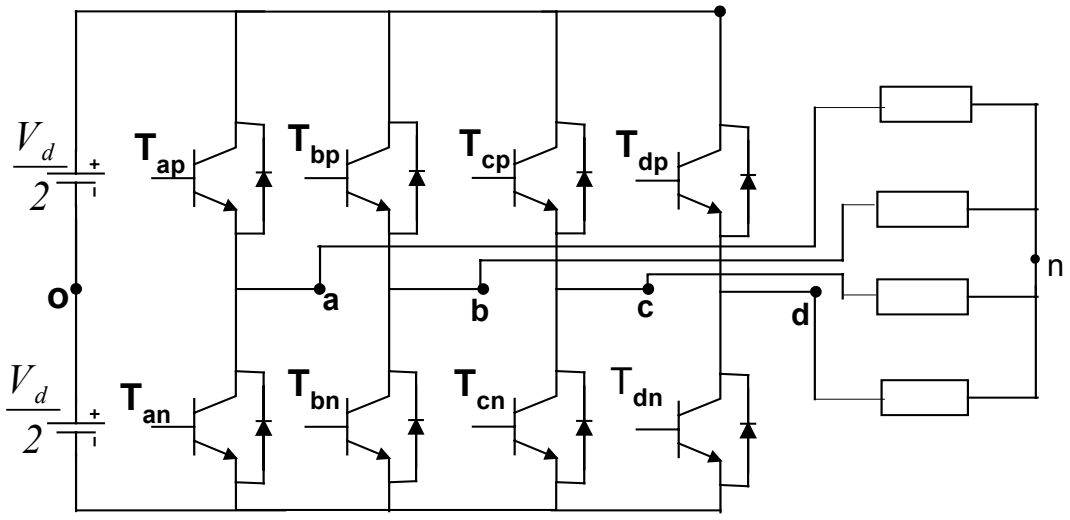

Fig. 1 : Circuit topology of four-leg DC/AC inverter.

In equations in (1), V_{an}, V_{bn}, V_{cn} are the desired phase voltages of the load and the phase voltage of the neutral impedance connected to the fourth leg is V_{dn}. The voltage between a reference 'o' of the inverter and the neutral of the load is denoted by V_{no}. In order to prevent short-circuiting the DC source and thereby not violate the Kichoff's voltage law, $\mathbf{S_{ip}}$ and $\mathbf{S_{in}}$ cannot be turned on at the same time. Hence, Kirchoff's law constraints the existence function such that $\mathbf{S_{ip}} + \mathbf{S_{in}}=1$. After an algebraic manipulation, with due considerations given to the constraints imposed by the voltage Kirchoff's law, equations in (1) reduce to :

$$V_d\ (S_{ap} - S_{dp}) = V_{an} - V_{dn}\ ,\quad V_d\ (S_{bp} - S_{dp}) = V_{bn} - V_{dn}$$
$$V_d\ (S_{cp} - S_{dp}) = V_{cn} - V_{dn} \qquad (2)$$

It is desired to determine the expressions for the four $\mathbf{S_{ij}}$ from equations in (2) given the phase voltages V_{an} , V_{bn}, V_{cn}, V_{dn}. Since there are three linear independent equations to be solved to determine expressions for four unknown existence functions, these equations are under-determined. In view of this indeterminacy, there is an infinite number of solutions which are obtained by various optimizing performance functions defined in terms of the existence functions. For a set of linear indeterminate equations expressed as $\mathbf{AX} = \mathbf{Y}$, a solution which minimizes the sum of squares of the variable $\mathbf{X}$ is obtained using the Moore-Penrose inverse [12]. The solution is given as $\mathbf{X} = \mathbf{A^T[AA^T]^{-1}Y}$. The solutions for the minimization of the sum of the squares of the four existence functions (equivalently, this is the maximization of the inverter output-input voltage gain), i.e. $S_{ap}^{\ 2} + S_{bp}^{\ 2} + S_{cp}^{\ 2} + S_{dp}^{\ 2}$ subject to the constraints in equations in (2) are given as [12] :

$$M_{ap} = 1/2\,(3V_{ann} - V_{bnn} - V_{cnn} - V_{dnn}),\ V_{ann} = V_{an}/V_d$$

$$M_{bp} = 1/2\,(-V_{ann} + 3V_{bnn} - V_{cnn} - V_{dnn}),\ V_{bnn} = V_{bn}/V_d$$

$$M_{cp} = 1/2\,(-V_{ann} - V_{bnn} + 3V_{cnn} - V_{dnn}),\ V_{cnn} = V_{cn}/V_d$$

$$M_{dp} = 1/2\,(-V_{ann} - V_{bnn} - V_{cnn} + 3V_{dnn}),\ V_{dnn} = V_{dn}/V_d \qquad (3)$$

M_{ip} are the continuous PWM modulation signals for the top devices of the four inverter legs. These signals are compared with a high frequency triangle carrier waveform (ranging from + 1 to –1) to generate the PWM switching pulses for the base drives of the switching devices represented by the existence functions S_{ip}.

III. SPACE VECTOR PWM

Respecting the Kirchoff's voltage law, which implies that the top and bottom switching devices of an inverter leg cannot be turned on at the same time, there are 16 feasible switching modes of the four-leg inverter which are enumerated in Table I [2]. The stationary reference frame qdo voltages of the switching modes are expressed in the complex variable form as ($a = e^{j\beta}$, $\beta = 120°$)

$$V_{qds} = 2/3(V_{an} + aV_{bn} + a^2V_{cn}),\ V_o = 1/3(V_{an} + V_{bn} + V_{cn}) \qquad (4)$$

Using the phase to reference voltages V_{ao}, V_{bo}, V_{co} and V_{do} for each switching mode and equations in (2), the components of the stationary reference frame V_{qdo} given in (5) are also shown in Table I.

$$V_{qs} = 1/6(2S_{ap} - S_{bp} - S_{cp} - 2S_{an} + S_{bn} + S_{cn})V_d,$$

$$V_{ds} = 1/2\sqrt{3}(S_{cp} - S_{bp} - S_{cn} + S_{bn})V_d$$

$$V_o - V_{dn} = 1/6(S_{ap} + S_{bp} + S_{cp} - S_{an} - S_{bn} - S_{cn} - 3S_{dp} + 3S_{dn})V_d \qquad (5)$$

It is evident from Table I that the 16 switching modes can be divided into three broad divisions. Modes ka and kb (k =1,2,3,4,5,6) have the same q and d axis voltages; however the values of the zero sequence voltages for modes ka are negative and those of kb are positive. Modes 7 and 8 are two null states while modes 9 and 10 are states with zero qd components having zero sequence voltages of opposite magnitude signs. We propose a space vector methodology based on the partitioning of modes a and b as shown in Fig. 2 where null states 7,8,9,10 are common to both. Since the inverters are used in systems with unbalanced and nonlinear loads, the zero sequence voltages for the switching modes must be included in the calculations and are therefore reflected in Fig. 2. In Fig. 2(a), the zero sequence voltages of the active modes are positive while they are negative in Fig. 2(b). In the sequel, Fig. 2(a) will be referred to as the positive (p) sequence space vector while Fig. 2(b) is the negative (n) space vector.

In classical space vector technique, a reference voltage V_{qd}^{*} located within the six sectors of the complex space vector in Fig. 2 is approximated instantaneously by time-averaging of six vectors comprising of two adjacent active switching modes and the two null modes 0,7 over the PWM sampling period T_s, which is much greater than the period of the reference signal. However, for the four-leg inverter, the reference voltage is approximated by time-averaging six switching modes comprising of the two active modes which are adjacent to the reference V_{qd}^{*}, and the four null voltage modes 7,8,9,10.

To realize a reference in sector I, switching 1,2,7,8,9,10 with voltages V_{qdo1}, V_{qdo2}, V_{qdo7}, V_{qdo8}, V_{qdo9}, V_{qdo10} are time-averaged while for another reference voltage in Sector V, switching modes 5,6,7,8,9,10 with voltages V_{qdo5}, V_{qdo6}, V_{qdo7}, V_{qdo8}, V_{qdo9}, V_{qdo10} are used. The normalized times the active modes (V_{qdoa} and V_{qdob}) are used are t_a and t_b respectively, t_d is the combined normalized time modes 9 and 10 are applied and the combined normalized time modes 7 and 8 are utilized is t_c. If mode 7 is applied

for $(1-\kappa)t_c$, mode 8 for κt_c , mode 9 for γt_d and mode 10 for $(1-\gamma)\, t_d$, then $t_a + t_b + t_c + t_d = 1$, $0 \le \kappa \le 1$, $0 \le \gamma \le 1$.

$$V_{qdo}^* = V_{qdoa}\, t_a + V_{qdob} t_b + V_{qdo7}(1-\kappa) t_c + V_{qdo8} \kappa t_c + V_{qdo9} \gamma\, t_d + V_{qdo10}(1-\gamma)\, t_d \qquad (6)$$

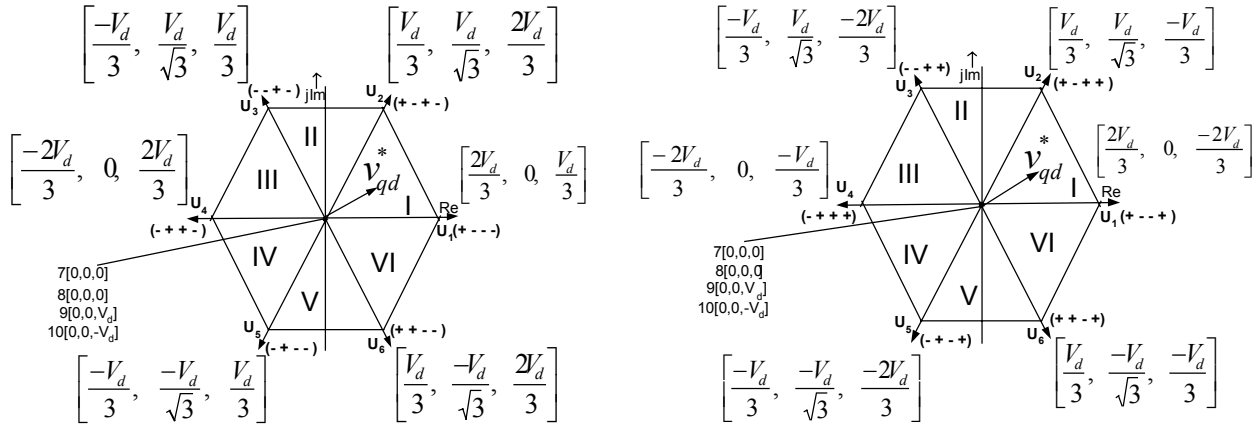

Fig. 2: Space vector of switching modes.(a) Positive zero sequence voltages, (b) negative zero sequence voltages.

Separating (6) into the three components, the normalized dwell times for reference voltages in the six sectors are calculated. The resulting equations expressed in terms of line-line reference voltages are given in Table II. The expressions for the normalized dwell times in Table II can also be generalized as $t_a = 1.5V(\cos\xi - 1/\sqrt{3} \sin\xi)$, $t_b = \sqrt{3}\sin\xi$, $V = \text{abs}(V_{qd}^*)/V_d$, $\psi = \text{angle}\,(V_{qd}^*) = 60(n-1) + \xi$, where he sector number is n (n=1,2,3,4,5,6).

Furthermore, the time normalized time t_d is given as:

$$t_d = (V_o^* - V_{oa}\, t_a - V_{ob}\, t_b)/V_d(2\gamma - 1) \qquad (7)$$

where $V_o^* = V_o - V_{dn}$

Table I Switching modes and qdo voltages

S_{ap}	S_{bp}	S_{cp}	S_{dp}	$3V_q^*$	$\sqrt{3}V_d^*$	$3V_o^*$	Mode
0	0	0	0	0	0	0	7
0	0	0	1	0	0	$-3V_d$	10
0	0	1	0	$-V_d$	V_d	V_d	3a
0	0	1	1	$-V_d$	V_d	$-2V_d$	3b
0	1	0	0	$-V_d$	$-V_d$	V_d	5a
0	1	0	1	$-V_d$	$-V_d$	$-2V_d$	5b
0	1	1	0	$-2V_d$	0	$2V_d$	4a
0	1	1	1	$-2V_d$	0	$-V_d$	4b
1	0	0	0	$2V_d$	0	V_d	1a
1	0	0	1	$2V_d$	0	$-2V_d$	1b
1	0	1	0	V_d	V_d	$2V_d$	2a
1	0	1	1	V_d	V_d	$-V_d$	2b
1	1	0	0	V_d	$-V_d$	$2V_d$	6a
1	1	0	1	V_d	$-V_d$	$-V_d$	6b
1	1	1	0	0	0	$3V_d$	9
1	1	1	1	0	0	0	8

Table II : Dwell times of the active devices.

Sector	1	2	3	4	5	6
$\mathbf{V_d t_a}$	V_{ac}	V_{ab}	V_{cb}	V_{ca}	V_{ba}	V_{bc}
$\mathbf{V_d t_b}$	V_{cb}	V_{ca}	V_{ba}	V_{bc}	V_{ac}	V_{ab}

The symmetric switching sequence is adopted which is presumed to have low THD in view of the symmetry of the waveforms. For a reference voltage in sector IV in Fig. 2(a), a period switching sequence is 1111→1110→ 0110→0100→0000→0001→0001→0000→0100→0110→1110→1111. For a reference voltage in sector IV in Fig. 2(b), 1110→1111→0111→0101→0001→0000→0000→ 0001→0101→0111→1111→ 1110 results. The existence functions of the four top devices for realizing a reference voltage in sector IV in Fig. 2(a) are shown in Fig. 3.

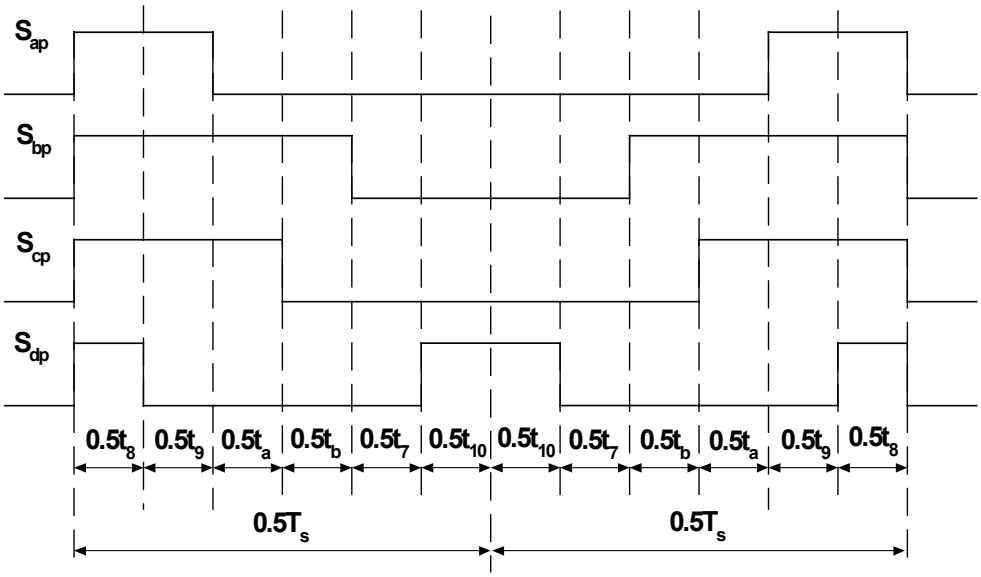

Figure 3 : Existence functions of top devices for operation in sector IV in Figure 2(a).

The operation of the modulator is as follows: the qdo quantities of the reference voltages are calculated at every sampling time with which the sector of operation is determined. From (6), t_a and t_b are determined which are the same for sectors in Figs. 2(a) and 2(b). Assume operation in the modes in the negative sequence space vector and determine t_d from (7) which is ensured to be positive by making the quantity γ to be either zero or unity. If $t_c > 0$, then select appropriate κ and determine the times the null states are applied. If $t_c < 0$,then, the positive sequence space vector is used and the new t_d is calculated. If $t_c > 0$, then the sequencing in Fig. 2(a) is adopted. If $t_c < 0$ for the two sequences, then the modulator cannot synthesize the unbalanced voltage set.

IV. DISCONTINUOUS PWM MODULATION

The expressions for the discontinuous modulation signals for the devices are determined by averaging their existence functions (such as those in Fig. 3) in each sector of Fig. 2. It is seen from Fig. 3 that the average of an existence function is equal to the sum of the normalized times each device is turned on to realize a reference voltage. Based on Tables I and II and (7), the total time each top device

is turned on for the six sectors are determined and given in Table III. Note that the expressions for the modulation signals for the top devices in phases a,b,c are the same for the two sequence space vectors; however the expressions for the modulation signals for phase d and the normalized time t_d are different In Table III, $M_{dp}(p)$ and $t_d(p)$, respectively, are the expressions for the top device d-phase modulation signal and time t_d for the positive sequence space vector while the corresponding expressions for the negative sequence space vector are $M_{dp}(n)$ and $t_d(n)$, respectively. These expressions are equivalent to the normalized modulation signals for the devices. Note that $0 \leq \kappa \leq 1$, which when varied, introduces different weights to the null states 7 and 8. The quantity γ is either zero or unity to ensure that t_d is always positive.

Given the instantaneous q and d voltages (equivalently, the qd magnitude and phase angle, ψ) of the unbalanced three-phase voltage set, the sector in Fig. 2 where it resides is determined. Then the times t_a , t_b with the aid of Table II are calculated. Assume operation in the negative sequence space vector. If $t_c > 0$, then the expressions for the modulation signals corresponding to the negative sequence space vector are used. If $t_c < 0$, then a new t_c is determined using equations corresponding to the positive sequence space vector, which if greater than zero, the expressions corresponding to the positive sequence space vector in the selected sector are adopted for the generation of the modulation signals. If $t_c < 0$ in the two cases, then the modulator cannot generate the waveforms. Again, an appropriate value of κ is selected to achieve further objective apart from synthesizing the waveforms. When κ is unity, we have a proper discontinuous modulation scheme since the modulation signal of a phase has at least one segment which clamped to either the positive or negative rail for at most a total of 120 degrees. Defining κ and γ appropriately, a generalized discontinuous PWM modulation results – a subject which will be explored in another publication.

V. EXPERIMENTAL RESULTS

The proposed modulation schemes are practically implemented by means of a floating-point 26-MHz DSP (ADSP2100) and the ADMC401 motion control board to synthesize three-phase unbalanced phase voltages. Fig. 4 shows the experimentally generated balanced reference three-phase voltages using the continuous modulation signals set forth in (3). The modulation signals for the top four devices are also displayed showing that for balanced phase voltages, the modulation signal for the fourth leg is zero. Fig. 5 gives the experimental waveforms when a three-phase unbalanced voltage set with the magnitude of phase 'a' voltage reduced by 20% is synthesized. Figs. 4-5 largely confirm the correctness of the proposed continuous modulation scheme.

Fig. 6 shows the synthesized three-phase balanced voltage set and the corresponding modulation signals using the discontinuous modulation scheme while Fig. 7 displays similar waveforms when the reference voltage set is unbalanced. These voltage waveforms are similar to those in Figs. 4 and 5. Fundamental components of the generated voltages are the same for various values of κ.

Fig. 8(1-3) displays the modulation signals for phase 'a' top device when the reference voltage set is balanced and κ is set to be 1.0, 0.5, 0.0 while in Fig. 8(4-6) the voltage set is no longer balanced. It is observed that for 120 degrees within a period, the modulation signals are unity ensuring that the top devices in a phase are turned on which results in lower switching loss and lower effective converter switching frequency.

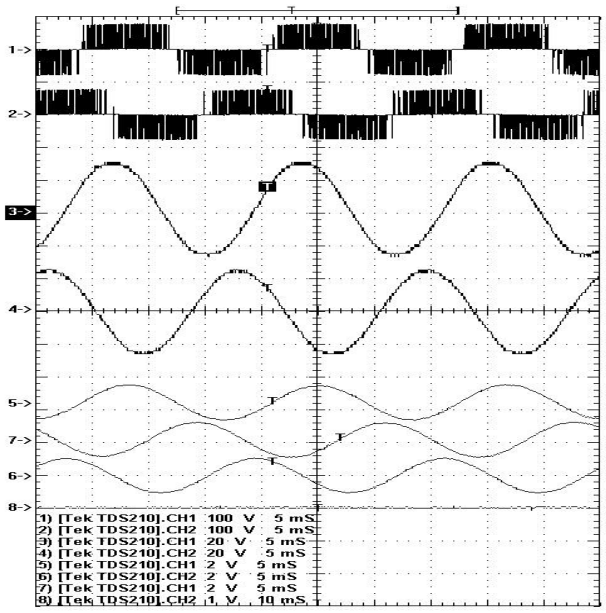

Figure 4 : Experimental results : Generation of balanced three-phase voltages using continuous modulation scheme. V_{an} = 25 cos (377t), V_{bn} =25 cos (377t - 2π/3), V_{cn} = 25 cos (377t + 2π/3), V_d = 80V. (1-2) phase 'a' and 'b' voltages, (3-4) filtered phase 'a' and 'b' voltages, (5-8) phase modulating signals.

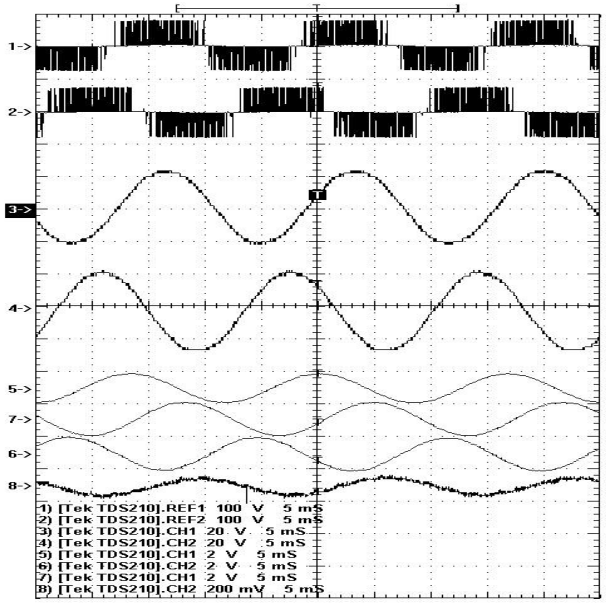

Figure 5: Experimental results : Generation of unbalanced three-phase voltages. Unbalanced voltages are V_{an} = 20 cos (377t), V_{bn} =25 cos (377t - 2π/3), V_{cn} = 25 cos (377t + 2π/3) V_d = 80V. (1-2) phase 'a' and 'b' voltages, (3-4) filtered phase 'a' and 'b' voltages, (5-8) phase modulating signals.

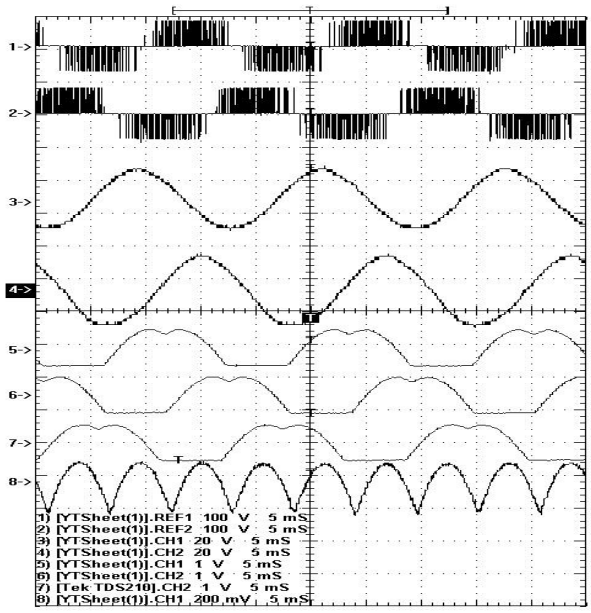

Figure 6 : Experimental results : Generation of balanced three-phase voltages using discontinuous modulation scheme. V_{an} = 25 cos (377t), V_{bn} =25 cos (377t - 2π/3), V_{cn} = 25 cos (377t + 2π/3) V_d = 80V. (1-2) phase 'a' and 'b' voltages, (3-4) filtered phase 'a' and 'b' voltages, (5-8) phase modulating signals.

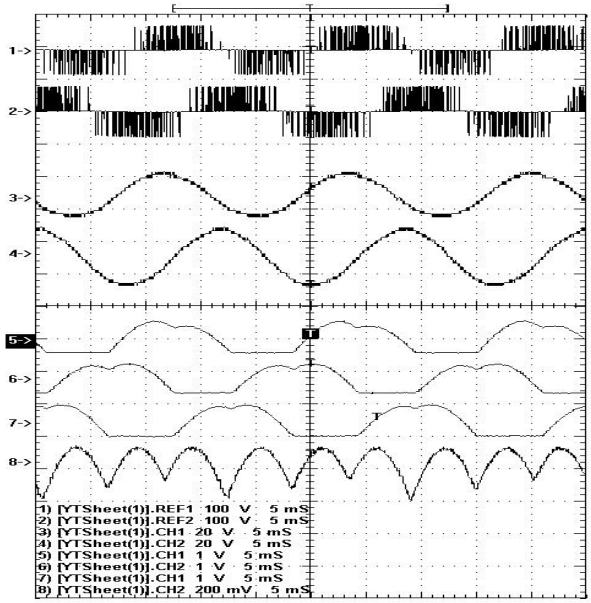

Figure 7 : Experimental results : Generation of unbalanced three-phase voltages using discontinuous modulation scheme. V_{an} = 25 cos (377t + π/12), V_{bn} =25 cos (377t - 2π/3), V_{cn} = 25 cos (377t + 2π/3) V_d = 80V. (1-2) phase 'a' and 'b' voltages, (3-4) filtered phase 'a' and 'b' voltages, (5-8) phase modulating signals.

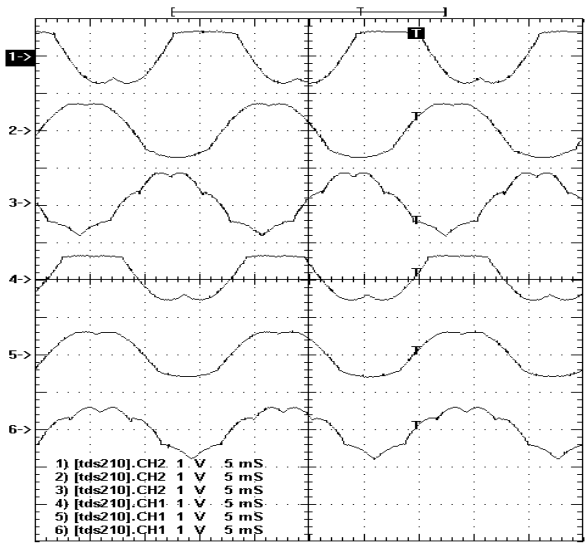

Figure 8: Generation of discontinuous modulation signals for phase 'a' top device. For balanced voltage set : (1) $\kappa = 1$, (2) $\kappa = 0.5$, (3) $\kappa = 0$ unbalanced voltage set : (4) $\kappa = 1$, (5) $\kappa = 0.5$, (6) $\kappa = 0$

TABLE III : Modulation signals for the top devices

Sector	M_{ap}	M_{bp}	M_{cp}	$M_{dp}(p)$	$M_{dp}(n)$	$t_d(p)$	$t_d(n)$
$0 \geq \psi \geq 60$	$V_{abn}+\gamma \mathbf{t}_d + \kappa(1-V_{abn}- t_d)$	$\gamma t_d + \kappa(1-V_{abn} - t_d)$	$\kappa(1-V_{abn}- t_d)+ V_{cbn}+\gamma \mathbf{t}_d$	$\kappa(1-V_{abn}- t_d)+(1-\gamma)\mathbf{t}_d$	$V_{abn}+\kappa(1-V_{abn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{bdd}\chi$	$V_{add}\chi$
$60 \geq \psi \geq 120$	$V_{abn}+\gamma t_d+ \kappa(1-V_{cbn} - t_d)$	$\gamma t_d+ \kappa(1-V_{cbn} - t_d)$	$V_{cbn}+\gamma t_d+ \kappa(1-V_{cbn}- t_d)$	$\kappa(1-V_{cbn}- t_d)+(1-\gamma)\mathbf{t}_d$	$V_{cbn}+\kappa(1-V_{cbn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{bdd}\chi$	$V_{cdd}\chi$
$120 \geq \psi \geq \pi$	$\gamma t_d +\kappa(1-V_{can} - t_d)$	$V_{ban}+\gamma \mathbf{t}_d +\kappa(1-V_{can} - t_d)$	$V_{can}+\gamma \mathbf{t}_d +\kappa(1-V_{can} - t_d)$	$\kappa(1-V_{can} - t_d)+(1-\gamma)\mathbf{t}_d$	$V_{can}+\kappa(1-V_{can}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{add}\chi$	$V_{cdd}\chi$
$-\pi \geq \psi \geq -120$	$\gamma t_d +\kappa(1-V_{ban} - t_d)$	$V_{ban}+\gamma t_d+\kappa(1-V_{ban} - t_d)$	$V_{can}+\gamma t_d +\kappa(1-V_{ban} - t_d)$	$\kappa(1-V_{ban} - t_d)+(1-\gamma)\mathbf{t}_d$	$V_{ban}+\kappa(1-V_{ban}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{add}\chi$	$V_{bdd}\chi$
$-120 \geq \psi \geq -60$	$V_{acn}+\gamma \mathbf{t}_d +\kappa(1-V_{bcn} - t_d)$	$V_{bcn}+\gamma \mathbf{t}_d +\kappa(1-V_{bcn} - t_d)$	$\gamma \mathbf{t}_d +\kappa(1-V_{bcn} - t_d)$	$\kappa(1-V_{bcn} - t_d)+(1-\gamma)\mathbf{t}_d$	$V_{bcn}+\kappa(1-V_{bcn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{cdd}\chi$	$V_{bdd}\chi$
$-60 \geq \psi \geq 0$	$V_{acn}+\gamma \mathbf{t}_d +\kappa(1-V_{acn} - t_d)$	$V_{bcn}+\gamma \mathbf{t}_d +\kappa(1-V_{acn} - t_d)$	$\gamma \mathbf{t}_d +\kappa(1-V_{acn} - t_d)$	$+\kappa(1-V_{acn} - t_d)+ (1-\gamma)\mathbf{t}_d$	$V_{acn}+\kappa(1-V_{acn}- t_d) + (1-\gamma)\mathbf{t}_d$	$V_{cdd}\chi$	$V_{add}\chi$

$\chi = 1/(2\gamma -1)$, $V_{ijn} = V_{ij}/V_d$, $V_{in} = V_{in}/ V_d$, i, j = a, b,c and $I \neq j$, $V_{kdd} = (V_{kn} - V_{dn})/ V_d$, k = a,b,c

VI. CONCLUSIONS

Three modulation schemes – space vector and two carrier-based which are the continuous and discontinuous carrier-based modulation schemes – have been proposed for the four-leg DC/AC inverter for the generation of three-phase voltages which may be balanced or unbalanced. The space vector scheme proposed partitions the 16 modes of operation into two sets: the positive sequence space vector where the zero sequence voltage is positive while in the negative sequence space vector, the zero sequence voltages are negative. A reference three-phase voltage set expressed in terms of the three components of the qdo stationary reference frame is synthesized by time-averaging two active modes and four null states. This schemes permits the partitioning of the total times spent in the null modes which influences the performance of the modulator. The continuous modulation scheme on the other hand is derived using an optimization methodology while the averaging of the existence functions for each of the inverter sectors yields expressions for the discontinuous modulation signals. A variable in the expressions for the modulation signals in the discontinuous modulation scheme permits the partitioning of the timing of the zero sequence voltages achieved by defining the value of κ which must instantaneously lie between unity and zero.

Some confirmatory experimental results showing both the voltage waveforms and modulation signals have been provided to verify the modulation methodologies proposed. Unbalanced and balanced three-phase voltages were experimentally synthesized by both the new space vector and discontinuous modulation schemes.

The techniques set forth for determining the proposed modulation schemes have wider potential applications in the definition of modulation strategies of other converters. Our future publications will extend the above methodologies for operation in the over-modulation region, address the applicability of the variables κ and γ for improving the performance of the modulator, and the dynamic control of

the four-leg converters in several applications such as in power quality improvement and stand-alone power supply.

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